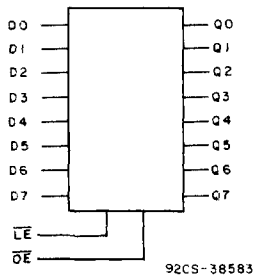


# CD54/74HC373, CD54/74HCT373 CD54/74HC573, CD54/74HCT573

## High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

## Octal Transparent Latch, 3-State Output

**Type Features:**

- Common latch enable control
- Common 3-state output enable control
- Buffered inputs
- 3-State outputs
- Bus line driving capacity
- Typical propagation delay = 12 ns @  $V_{CC} = 5V, C_L = 15 pF, T_A = 25^\circ C$  (Data to Output for HC373)

The RCA CD54/74HC373/573 and CD54/74HCT373/573 are high speed Octal Transparent Latches manufactured with silicon gate CMOS technology. They possess the low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LSTTL devices. The CD54/74HCT373/573 are functionally as well as pin compatible with the standard 54/74LS373 and 573.

The outputs are transparent to the inputs when the latch enable ( $\overline{LE}$ ) is high. When the latch enable ( $\overline{LE}$ ) goes low the data is latched. The output enable ( $\overline{OE}$ ) controls the 3-state outputs. When the output enable ( $\overline{OE}$ ) is high the outputs are in the high impedance state. The latch operation is independent to the state of the output enable. The 373 and 573 are identical in function and differ only in their pinout arrangements.

The CD54HC/HCT373/573 are supplied in 20 lead ceramic dual-in-line packages (F suffix). The CD74HC/HCT373/573 are supplied in a 20-lead plastic dual-in-line plastic package (E suffix) and in 20-lead surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

**Family Features:**

- Fanout (Over Temperature Range):  
Standard Outputs - 10 LSTTL Loads  
Bus Driver Outputs - 15 LSTTL Loads
- Wide Operating Temperature Range:  
CD74HC/HCT: -40 to +85° C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips/Signetics
- CD54HC/CD74HC Types:  
2 to 6 V Operation  
High Noise Immunity:  $N_{IL} = 30\%, N_{IH} = 30\%$  of  $V_{CC}$ ; @  $V_{CC} = 5 V$
- CD54HCT/CD74HCT Types:  
4.5 to 5.5 V Operation  
Direct LSTTL Input Logic Compatibility  
 $V_{IL} = 0.8 V$  Max.,  $V_{IH} = 2 V$  Min.  
CMOS Input Compatibility  
 $I_i \leq 1 \mu A$  @  $V_{OL}, V_{OH}$

**TRUTH TABLE**

Output Enable	Latch Enable	Data	Output
L	H	H	H
L	H	L	L
L	L	l	L
L	L	h	H
H	X	X	Z

Note:  
 L = Low voltage level  
 H = High voltage level  
 l = Low voltage level one set-up time prior to the high to low latch enable transition  
 h = High voltage level one set-up time prior to the high to low latch enable transition  
 X = Don't Care  
 Z = High Impedance State

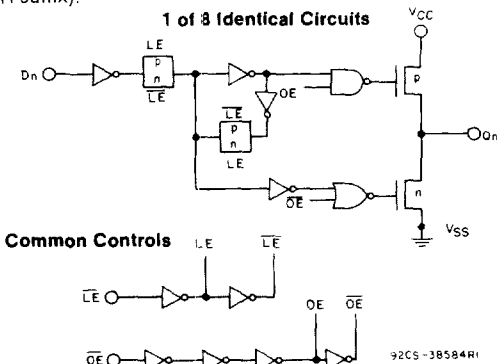


Fig. 1 - Logic diagram.

# CD54/74HC373, CD54/74HCT373 CD54/74HC573, CD54/74HCT573

**MAXIMUM RATINGS, Absolute-Maximum Values:**

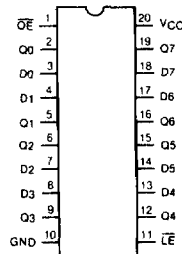
DC SUPPLY-VOLTAGE, (V <sub>CC</sub> ): (Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I <sub>IK</sub> (FOR V <sub>I</sub> < -0.5 V OR V <sub>I</sub> > V <sub>CC</sub> + 0.5 V)	±20 mA
DC OUTPUT DIODE CURRENT, I <sub>OK</sub> (FOR V <sub>O</sub> < -0.5 V OR V <sub>O</sub> > V <sub>CC</sub> + 0.5 V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I <sub>O</sub> ) (FOR -0.5 V < V <sub>O</sub> < V <sub>CC</sub> + 0.5 V)	±35 mA
DC V <sub>CC</sub> OR GROUND CURRENT, (I <sub>CC</sub> ):	±70 mA
<b>POWER DISSIPATION PER PACKAGE (P<sub>D</sub>):</b>	
For T <sub>A</sub> = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T <sub>A</sub> = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T <sub>A</sub> = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T <sub>A</sub> = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T <sub>A</sub> = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T <sub>A</sub> = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
<b>OPERATING-TEMPERATURE RANGE (T<sub>A</sub>):</b>	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
<b>STORAGE TEMPERATURE (T<sub>STG</sub>)</b>	
	-65 to +150°C
<b>LEAD TEMPERATURE (DURING SOLDERING):</b>	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

**RECOMMENDED OPERATING CONDITIONS:**

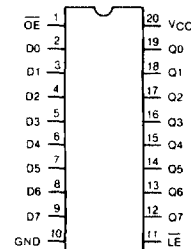
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T <sub>A</sub> = Full Package-Temperature Range) V <sub>CC</sub> .* CD54/74HC Types CD54/74HCT Types	2 4.5	6 5.5	V V
DC Input or Output Voltage V <sub>I</sub> , V <sub>O</sub>	0	V <sub>CC</sub>	V
Operating Temperature T <sub>A</sub> : CD74 Types CD54 Types	-40 -55	+85 +125	°C °C
Input Rise and Fall Times, t <sub>r</sub> , t <sub>f</sub> at 2 V at 4.5 V at 6 V	0 0 0	1000 500 400	ns ns ns

\*Unless otherwise specified, all voltages are referenced to Ground.



92CS 36819  
**CD54/74HC373, CD54/74HCT373  
TERMINAL ASSIGNMENT**



92CS 36715  
**CD54/74HC573, CD54/74HCT573  
TERMINAL ASSIGNMENT**

# CD54/74HC373, CD54/74HCT373 CD54/74HC573, CD54/74HCT573

## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CD74HC373/CD54HC373 CD74HC573/CD54HC573									CD74HCT373/CD54HCT373 CD74HCT573/CD54HCT573									UNITS					
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE			54HC TYPE			TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE			54HCT TYPE			
	V <sub>i</sub> V	I <sub>o</sub> mA	V <sub>cc</sub> V	+25°C			-40/ +85°C			-55/ +125°C			V <sub>i</sub> V	V <sub>cc</sub> V	+25°C			-40/ +85°C			-55/ +125°C			
				Min	Typ	Max	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max		Min	Max			
High-Level Input Voltage V <sub>IH</sub>			2	1.5	—	—	1.5	—	1.5	—	—	—	4.5			2	—	—	2	—	2	—	—	V
			4.5	3.15	—	—	3.15	—	3.15	—	—	—	I <sub>o</sub>			—	—	0.8	—	0.8	—	—	—	V
			6	4.2	—	—	4.2	—	4.2	—	—	—	5.5			—	—	—	—	—	—	—	—	V
Low-Level Input Voltage V <sub>IL</sub>			2	—	—	0.5	—	0.5	—	0.5	—	—	4.5			—	—	0.8	—	0.8	—	—	—	V
			4.5	—	—	1.35	—	1.35	—	1.35	—	—	I <sub>o</sub>			—	—	—	—	—	—	—	—	V
			6	—	—	1.8	—	1.8	—	1.8	—	—	5.5			—	—	—	—	—	—	—	—	V
High-Level Output Voltage V <sub>OH</sub>	V <sub>IL</sub> or V <sub>IH</sub>	-0.02	2	1.9	—	—	1.9	—	1.9	—	—	V <sub>IL</sub> or V <sub>IH</sub>	4.5	4.4	—	—	4.4	—	4.4	—	4.4	—	—	V
CMOS Loads	V <sub>IL</sub> or V <sub>IH</sub>		4.5	4.4	—	—	4.4	—	4.4	—	—	V <sub>IL</sub> or V <sub>IH</sub>	4.5	3.98	—	—	3.84	—	3.84	—	3.7	—	—	V
TTL Loads (Bus Driver)	V <sub>IL</sub> or V <sub>IH</sub>	-6 -7.8	4.5	3.98	—	—	3.84	—	3.7	—	—	V <sub>IL</sub> or V <sub>IH</sub>	4.5	3.98	—	—	3.84	—	3.84	—	3.7	—	—	V
Low-Level Output Voltage V <sub>OL</sub>	V <sub>IL</sub> or V <sub>IH</sub>	0.02	2	—	—	0.1	—	0.1	—	0.1	—	V <sub>IL</sub> or V <sub>IH</sub>	4.5	—	—	0.1	—	0.1	—	0.1	—	—	—	V
CMOS Loads	V <sub>IL</sub> or V <sub>IH</sub>		4.5	—	—	0.1	—	0.1	—	0.1	—	V <sub>IL</sub> or V <sub>IH</sub>	4.5	—	—	0.1	—	0.1	—	0.1	—	—	—	V
TTL Loads (Bus Driver)	V <sub>IL</sub> or V <sub>IH</sub>	6 7.8	4.5	—	—	0.26	—	0.33	—	0.4	—	V <sub>IL</sub> or V <sub>IH</sub>	4.5	—	—	0.26	—	0.33	—	0.33	—	—	—	V
Input Leakage Current I <sub>i</sub>	V <sub>cc</sub> or Gnd		6	—	—	±0.1	—	±1	—	±1	—	Any Voltage Between V <sub>cc</sub> and Gnd	5.5	—	—	±0.1	—	±1	—	±1	—	—	—	μA
Quiescent Device Current I <sub>cc</sub>	V <sub>cc</sub> or Gnd	0	6	—	—	8	—	80	—	160	—	V <sub>cc</sub> or Gnd	5.5	—	—	8	—	80	—	80	—	—	—	μA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI <sub>cc</sub> *												V <sub>cc</sub> -2.1	4.5 to 5.5	—	100	360	—	450	—	490	—	—	—	μA
3-State Leakage Current	V <sub>IL</sub> or V <sub>IH</sub>	V <sub>o</sub> =V <sub>cc</sub> or Gnd	6	—	—	±0.5	—	±5	—	±10	—	V <sub>IL</sub> or V <sub>IH</sub>	5.5	—	—	±0.5	—	±5	—	±10	—	—	—	μA

\*For dual-supply systems theoretical worst case (V<sub>i</sub> = 2.4 V, V<sub>cc</sub> = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS*	
	HCT373	HCT573
$\overline{OE}$	1.5	1.25
$\overline{Dn}$	0.4	0.3
$\overline{LE}$	0.6	0.65

\* Unit Load is ΔI<sub>cc</sub> limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

# CD54/74HC373, CD54/74HCT373 CD54/74HC573, CD54/74HCT573

SWITCHING CHARACTERISTICS ( $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , Input  $t_r, t_f = 6\text{ ns}$ )

CHARACTERISTIC	$C_L$ (pF)	TYPICAL VALUES		UNITS
		HC	HCT	
Propagation Delay				
Data to Qn Output (HC/HCT373) (Fig. 3)	$t_{PLH}$ $t_{PHL}$	15	13	ns
Data to Qn Output (HC/HCT573) (Fig. 3)	$t_{PLH}$ $t_{PHL}$	15	17	ns
$\overline{LE}$ to Qn Output (Fig. 4)	$t_{PLH}$ $t_{PHL}$	15	14	ns
Output Enabling Time (Fig. 6, 7)	$t_{PZL}$ $t_{PZH}$	15	14	ns
Output Disabling Time (Fig. 6, 7)	$t_{PLZ}$ $t_{PHZ}$	15	14	ns
Power Dissipation Capacitance (HC/HCT573, 373)	$C_{PD}^*$	—	51	pF

\* $C_{PD}$  determines the no-load dynamic power consumption per latch. It is obtained by the following relationship;

$P_D$  (total power per latch) =  $V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = input frequency,

$C_L$  = output load capacitance,  $V_{CC}$  = supply voltage

## PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	TEST CONDITIONS	LIMITS												UNITS
		25°C				-40°C to +85°C				-55°C to +125°C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$\overline{LE}$ Pulse Width $t_w$ (Fig. 3)	$V_{CC} = 2$	80	—	—	—	100	—	—	—	120	—	—	—	ns
	$V_{CC} = 4.5$	16	—	16	—	20	—	20	—	24	—	24	—	
	$V_{CC} = 6$	14	—	—	—	17	—	—	—	20	—	—	—	
Set-up Time $t_{SU}$ Data to $\overline{LE}$ 573 (Fig. 4)	$V_{CC} = 2$	50	—	—	—	65	—	—	—	75	—	—	—	ns
	$V_{CC} = 4.5$	10	—	13	—	13	—	16	—	15	—	20	—	
	$V_{CC} = 6$	9	—	—	—	11	—	—	—	13	—	—	—	
Set-up Time $t_{SU}$ Data to $\overline{LE}$ 373 (Fig. 4)	$V_{CC} = 2$	50	—	—	—	65	—	—	—	75	—	—	—	ns
	$V_{CC} = 4.5$	10	—	13	—	13	—	16	—	15	—	20	—	
	$V_{CC} = 6$	9	—	—	—	11	—	—	—	13	—	—	—	
Hold Time $t_H$ Data to $\overline{LE}$ 573 (Fig. 4)	$V_{CC} = 2$	40	—	—	—	50	—	—	—	60	—	—	—	ns
	$V_{CC} = 4.5$	8	—	10	—	10	—	13	—	12	—	15	—	
	$V_{CC} = 6$	7	—	—	—	9	—	—	—	10	—	—	—	
Hold Time $t_H$ Data to $\overline{LE}$ 373 (Fig. 4)	$V_{CC} = 2$	5	—	—	—	5	—	—	—	5	—	—	—	ns
	$V_{CC} = 4.5$	5	—	10	—	5	—	13	—	5	—	15	—	
	$V_{CC} = 6$	5	—	—	—	5	—	—	—	5	—	—	—	

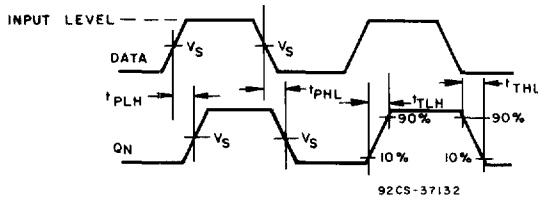
# CD54/74HC373, CD54/74HCT373

# CD54/74HC573, CD54/74HCT573

 SWITCHING CHARACTERISTICS (Input  $t_r, t_f = 6$  ns,  $C_L = 50$  pF)

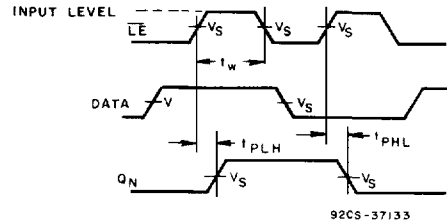
CHARACTERISTIC	TEST CONDITIONS	LIMITS												UNITS	
		25° C				-40° C to +85° C				-55° C to +125° C					
		HC		HCT		74HC		74HCT		54HC		54HCT			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Propagation Delay Data to Qn (Fig. 2) HC/HCT373	$t_{PLH}$	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
	$t_{PHL}$	4.5	—	30	—	32	—	38	—	40	—	45	—	48	
		6	—	26	—	—	—	33	—	—	—	38	—	—	
Data to Qn (Fig. 2) HC/HCT573	$t_{PLH}$	2	—	175	—	—	—	220	—	—	—	265	—	—	ns
	$t_{PHL}$	4.5	—	35	—	35	—	44	—	44	—	53	—	53	
		6	—	30	—	—	—	37	—	—	—	45	—	—	
$\overline{LE}$ to Qn (Fig. 3)	$t_{PLH}$	2	—	175	—	—	—	220	—	—	—	265	—	—	ns
	$t_{PHL}$	4.5	—	35	—	35	—	44	—	44	—	53	—	53	
		6	—	30	—	—	—	37	—	—	—	45	—	—	
Output Enabling Time (Figs. 5 & 6)	$t_{PZL}$	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
	$t_{PZH}$	4.5	—	30	—	35	—	38	—	44	—	45	—	53	
		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Disabling Time (Figs. 5 & 6)	$t_{PLZ}$	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
	$t_{PHZ}$	4.5	—	30	—	35	—	38	—	44	—	45	—	53	
		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Transition Time (Fig. 2)	$t_{T-H}$	2	—	60	—	—	—	75	—	—	—	90	—	—	ns
	$t_{T-HL}$	4.5	—	12	—	12	—	15	—	15	—	18	—	18	
		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	$C_i$	—	—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	$C_o$	—	—	20	—	20	—	20	—	20	—	20	—	20	pF

# CD54/74HC373, CD54/74HCT373 CD54/74HC573, CD54/74HCT573



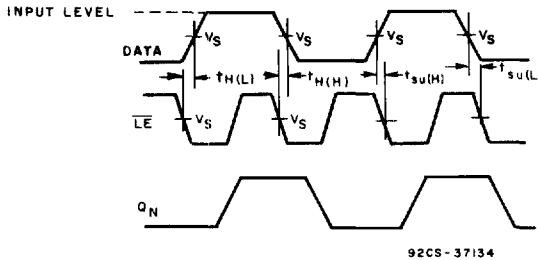
	54/74HC	54/74HCT
Input Level	$V_{CC}$	3 V
$V_S$	50% $V_{CC}$	1.3 V

Fig. 2 - Data to  $Q_n$  output propagation delays and output transition times.



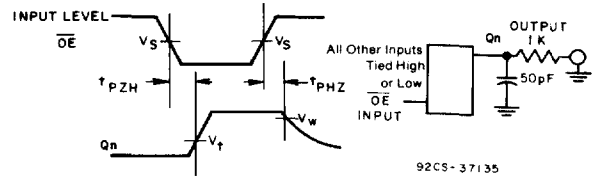
	54/74HC	54/74HCT
Input Level	$V_{CC}$	3 V
$V_S$	50% $V_{CC}$	1.3 V

Fig. 3 - Latch enable propagation delays.



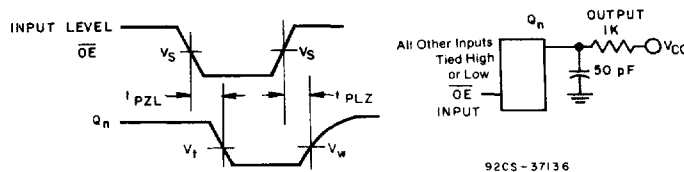
	54/74HC	54/74HCT
Input Level	$V_{CC}$	3 V
$V_S$	50% $V_{CC}$	1.3 V

Fig. 4 - Latch enable prerequisite times.



	54/74HC	54/74HCT
Input Level	$V_{CC}$	3 V
$V_S$	50% $V_{CC}$	1.3 V
$V_t$	50% $V_{CC}$	1.3 V
$V_w$	90% $V_{CC}$	90% $V_{CC}$

Fig. 5 - Three-state propagation delays.



	54/74HC	54/74HCT
Input Level	$V_{CC}$	3 V
$V_S$	50% $V_{CC}$	1.3 V
$V_t$	50% $V_{CC}$	1.3 V
$V_w$	10% $V_{CC}$	10% $V_{CC}$

Fig. 6 - Three-state propagation delays.