DPS32M8A

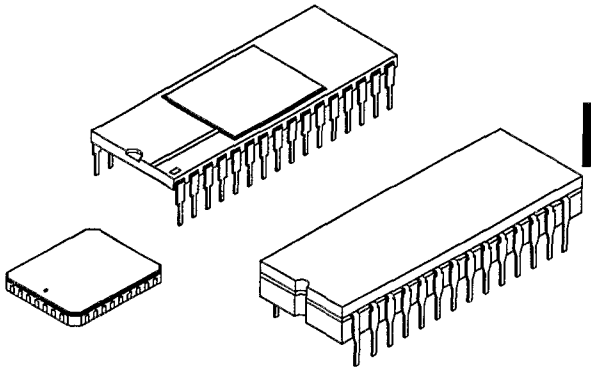
HIGH SPEED 32K X 8 CMOS SRAM MONOLITHIC

ADVANCED INFORMATION

DESCRIPTION:

The DPS32M8A is a 32K X 8 CMOS Static Random Access Memory (SRAM). The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single +5V power supply is required.

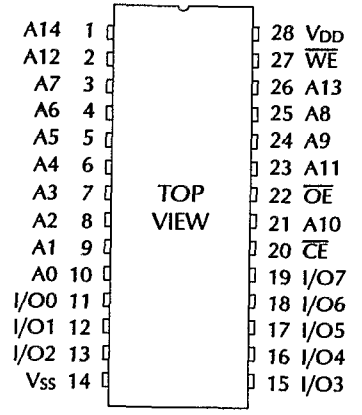
The DPS32M8A is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost and high performance.



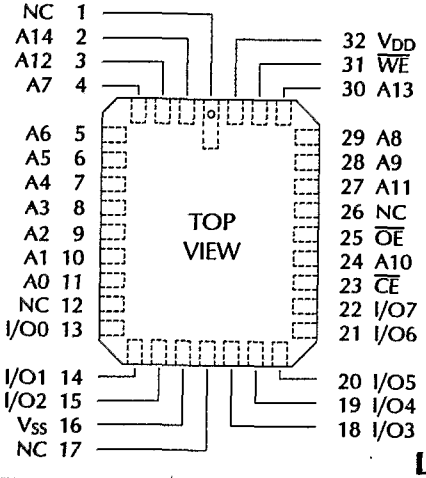
FEATURES:

- 32,768 by 8-Bits Organization
- Access Times: 25, 35, 45, 55, 70, 85ns (max.)
- Low Power: 110mW (max.) Full Standby
- Fully Static Operation; No Clock or Refresh Required
- TTL Compatible Input and Output
- Common Data Input and Output
- Single +5V Power Supply, ±10% Tolerance
- Three State Output
- Standard 28-Pin DIP or 32-Pad LCC Packages

PIN-OUT DIAGRAMS

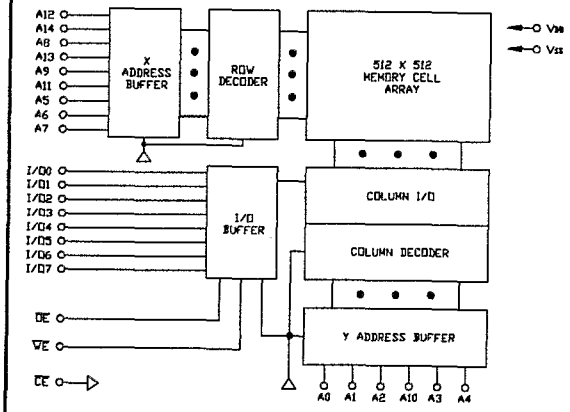


DIP



LCC

FUNCTIONAL BLOCK DIAGRAM



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TRUTH TABLE

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O Pin	Supply Current
Not Selected	H	X	X	HIGH-Z	Standby
D_{OUT} Disable	L	H	H	HIGH-Z	Active
Read	L	L	H	D_{OUT}	Active
Write	L	X	L	D_{IN}	Active

L = LOW H = HIGH X = Don't Care

PIN NAMES

A0-A14	Address Inputs
I/O0-I/O7	Data In/Out
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{DD}	Power (+5V)
V_{SS}	Ground

RECOMMENDED OPERATING RANGE[1]

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		V_{DD}+0.3	V
V_{IL}	Input LOW Voltage	-0.5[2]		0.8	V

ABSOLUTE MAXIMUM RATINGS[3]

Symbol	Parameter	Value	Unit
T_{STC}	Storage Temperature	-65 to +150	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
V_{DD}	Supply Voltage[1]	-0.5 to +7.0	V
$V_{I/O}$	Input/Output Voltage[1]	-0.5 to +7.0	V

CAPACITANCE[4]: T_A = 25°C, F = 1.0MHz

Symbol	Parameter	Max.	Unit	Condition
C_{IN}	Input Capacitance	11	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	11		

DC OPERATING CHARACTERISTICS: Over operating ranges

Symbol	Characteristics	Test Conditions		C Min.	C Max.	I Min.	I Max.	M/B Min.	M/B Max.	Unit
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}		-10	10	-10	10	-10	10	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{CE}$ or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}		-10	10	-10	10	-10	10	µA
I_{CC1}	Active Supply Current	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA			100		115		120	mA
I_{CC2}	Operating Supply Current	Cycle = min., Duty = 100% I_{OUT} = 0mA			140		160		160	mA
I_{SB1}	Full Standby Supply Current (CMOS)	f = 0, Outputs Open $\overline{CE}$ ≥ V_{DD} -0.2V	S		10		15		20	mA
		V_{IN}≥V_{DD} -0.2V or V_{IN}≥V_{DD} -0.2V	L		2		2		2	
I_{SB2}	Standby Supply (TTL)	$\overline{CE}$ = V_{IH}, f = 0, Outputs Open			30		35		35	mA
V_{OL}	Output Low Voltage	I_{OUT} = 8.0mA			0.4		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -4mA		2.4		2.4		2.4		V

DATA RETENTION DC CHARACTERISTICS: (L Versions only)

Symbol	Characteristics	Test Conditions	C Min.	C Max.	I Min.	I Max.	M/B Min.	M/B Max.	Unit
I_{CCDR3}	Data Retention Supply Current	V_{DR} = 3V, $\overline{CE}$ ≥ V_{DR} -0.2V		350		400		800	µA
I_{CCDR2}	Data Retention Supply Current	V_{DR} = 2V, $\overline{CE}$ ≥V_{DR} -0.2V		300		350		600	µA

DATA RETENTION CHARACTERISTICS (L Versions only)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DR}	Data Retention Voltage	$\overline{CE}$ ≥ V_{DD} -0.2V	2.0	5.0	5.5	V
t_{CDR}	Chip Disable to Data Retention Time		0			ns
t_R	Recovery Time	t_{RC} = Read Cycle Timing	t_{RC}			ns

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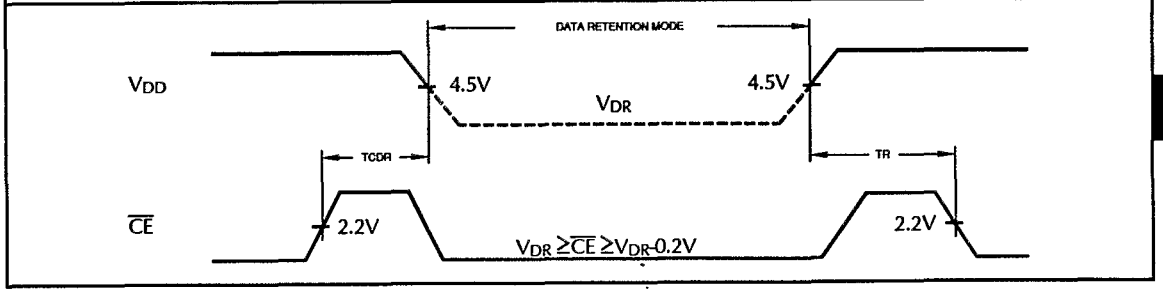
DATA RETENTION WAVEFORM



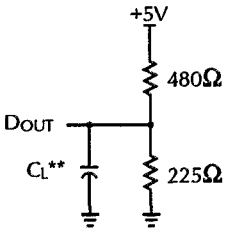
AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns*
Input and Output Timing Reference Levels	1.5V

* Transition between 0.8V and 2.2V.

OUTPUT LOAD		
Load	C_L	Parameters Measured
1	100pF	except t_{CLZ}, t_{CHZ}, t_{OHZ}, t_{OLZ}, t_{WLZ} and t_{WHZ}
2	5pF	t_{CLZ}, t_{CHZ}, t_{OHZ}, t_{OLZ}, t_{WLZ} and t_{WHZ}

Figure 1. Output Load

** Including Probe and Jig Capacitance.



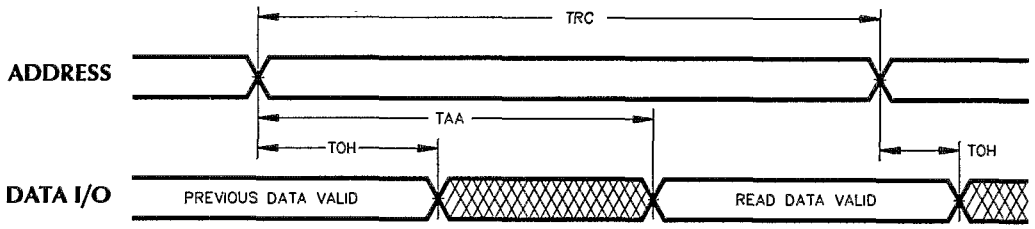
AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges														
No.	Symbol	Parameter	-25		-35-		45		-55		-70		-85		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	25		35		45		55		70		85		ns
2	t_{AA}	Address Access Time		25		35		45		55		70		85	ns
3	t_{CO}	Chip Enable to Output Valid		25		35		45		55		70		85	ns
4	t_{OV}	Output Enable to Output Valid		15		20		20		25		30		35	ns
5	t_{OH}	Output Hold from Address Change	5		5		5		5		5		5		ns
6	t_{CLZ}	Chip Enable to Output in LOW-Z [4, 5]	5		5		5		5		5		5		ns
7	t_{OLZ}	Output Enable to Output in LOW-Z [4, 5]	3		3		3		3		3		3		ns
8	t_{CHZ}	Chip Enable to Output in HIGH-Z [4, 5]		15		20		20		25		30		35	ns
9	t_{OHZ}	Output Enable to Output in HIGH-Z [4, 5]		15		20		20		25		30		35	ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE [6,7]: Over operating ranges														
No.	Symbol	Parameter	-25		-35-		45		-55		-70		-85		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
10	t_{WC}	Write Cycle Time	25		35		45		55		70		85		ns
11	t_{AW}	Address Valid to End of Write	20		30		40		50		60		70		ns
12	t_{CW}	Chip Enable to End of Write	20		30		40		50		60		70		ns
13	t_{DW}	Data Valid to End of Write	15		18		20		25		30		35		ns
14	t_{DH}	Data Hold Time	3		3		3		3		3		3		ns
15	t_{WP}	Write Pulse Width	20		30		35		40		45		50		ns
16	t_{AS}	Address Set-up Time ***	0		0		0		0		0		0		ns
17	t_{AH}	Address Hold Time	0		0		0		0		0		0		ns
18	t_{WHZ}	Write Enable to Output in HIGH-Z [4, 5]		15		15		20		25		30		35	ns
19	t_{WLZ}	Write Enable to Output in LOW-Z [4, 5]	5		5		5		5		5		5		ns

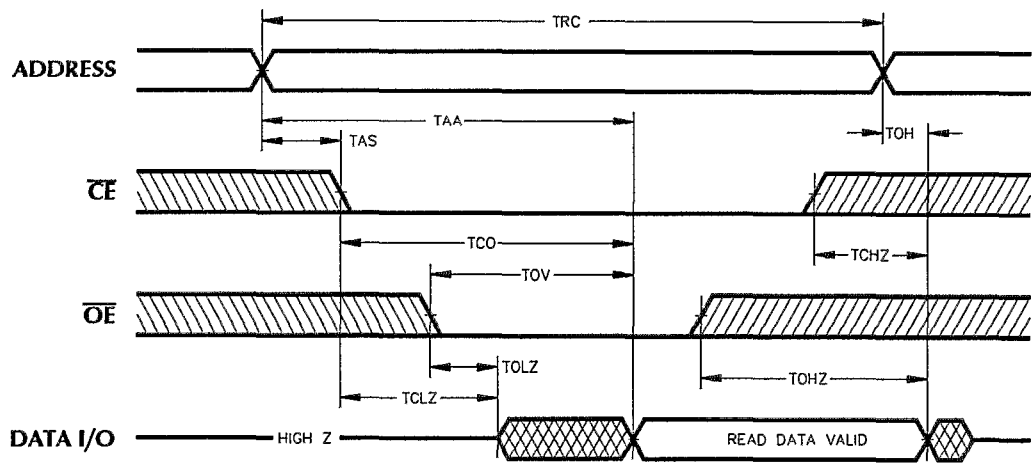
*** Valid for both Read and Write Cycles.

ADVANCED INFORMATION

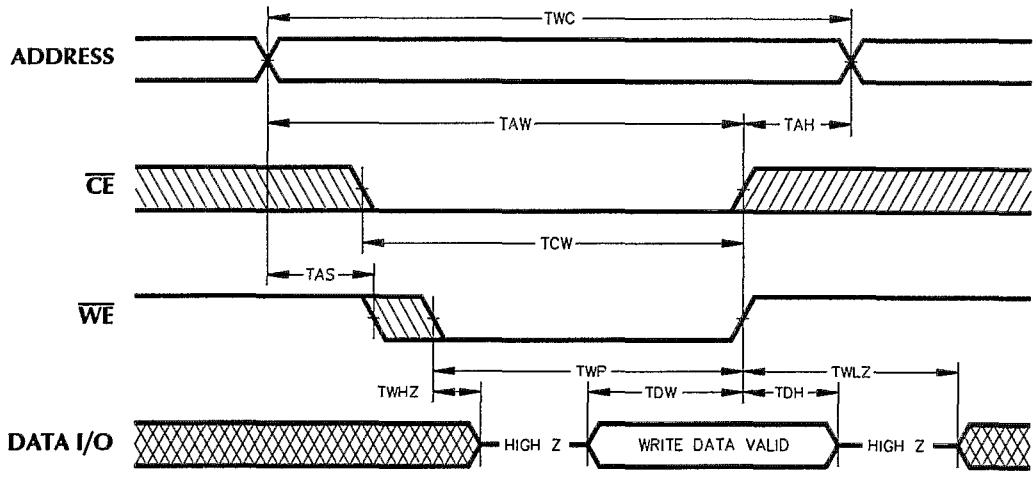
READ CYCLE 1: Address Controlled. $\overline{WE}$ is HIGH. $\overline{CE}$ and $\overline{OE}$ are LOW.



READ CYCLE 2: $\overline{CE}$ Controlled. $\overline{WE}$ is HIGH.

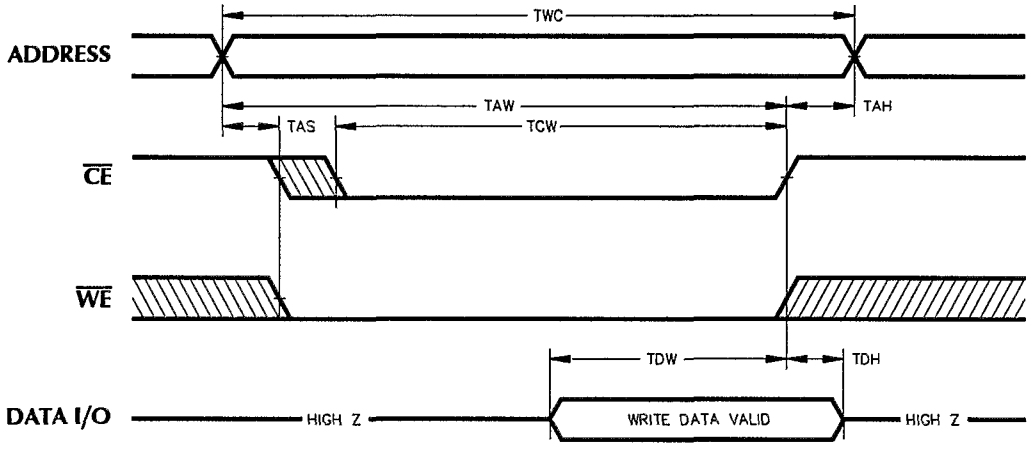


WRITE CYCLE 1: $\overline{WE}$ Controlled. $\overline{OE}$ is LOW.



ADVANCED INFORMATION

WRITE CYCLE 2: $\overline{CE}$ Controlled. $\overline{OE}$ is HIGH.



WAVEFORM KEY

NOTES:

1. All voltages are with respect to V_{SS}.
2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guarenteed and not 100% tested.
5. Transition is measured at the point of ±500mV from steady state voltage.
6. When $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state; and, input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.

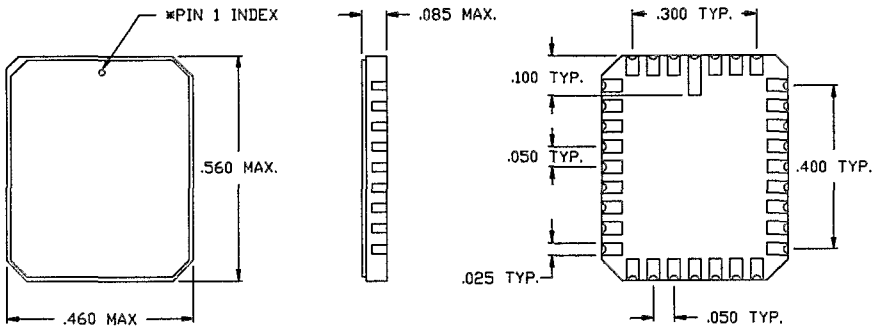
ORDERING INFORMATION

DP	S32M8A	X	X	– XX	X
PREFIX	DEVICE TYPE	PACKAGE	POWER	SPEED	GRADE

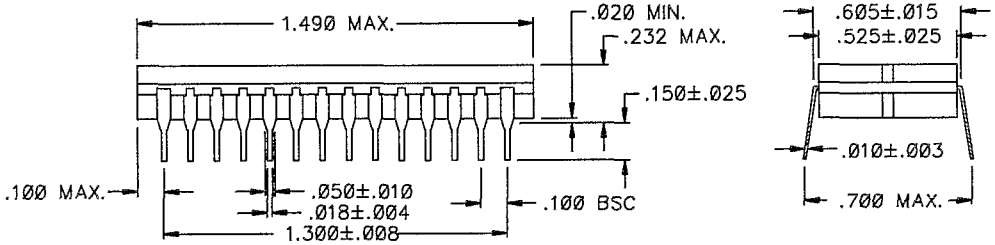
C	COMMERCIAL	0°C to +70°C
I	INDUSTRIAL	-40°C to +85°C
M	MILITARY	-55°C to +125°C
B	MIL-PROCESSED	-55°C to +125°C
25	25ns	
35	35ns	
45	45ns	
55	55ns	
70	70ns	
85	85ns	
S	STANDARD POWER	
L	LOW POWER	
G	32 PAD LCC	
N	28 LEAD SIDE BRAZED DIP	
NONE	28 LEAD CERDIP	
	HIGH SPEED 32K X 8 CMOS SRAM	

ADVANCED INFORMATION

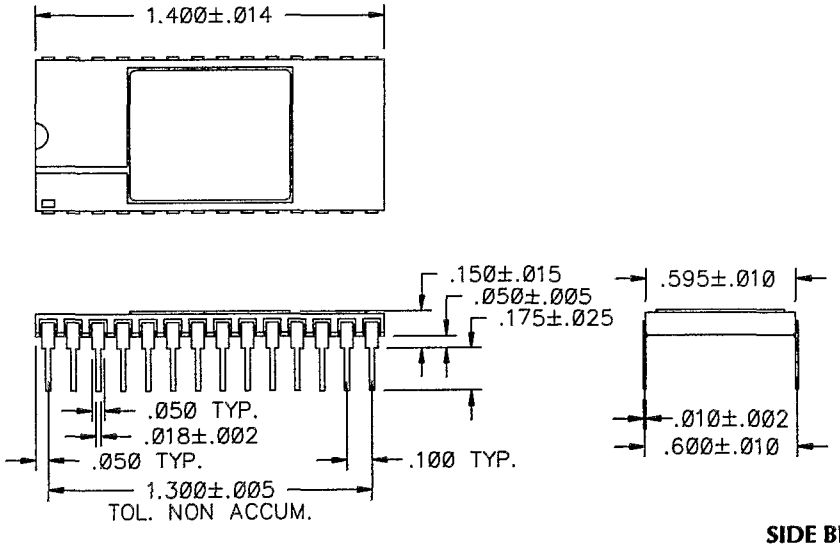
MECHANICAL DIAGRAMS



LCC



CERDIP



SIDE BRAZED DIP

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