HY628400 Series

512K x 8-bit CMOS SRAM

PRELIMINARY

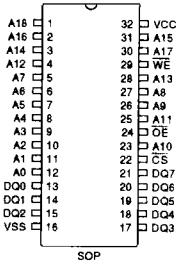
DESCRIPTION

The HY628400 is a high speed, low power and 524,288 x 8-bit CMOS static RAM fabricated using Hyundai's high performance twin tub CMOS process. This high reliability process coupled with innovative circuit design techniques, yields maximum access time of 55ns. The HY628400 has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 2.0 volt. Using CMOS technology, supply voltages from 2.0 to 5.5 volt have little effect on supply current in data retention mode. Reducing the supply voltage to minimize current drain is unnecessary with the HY628400 series.

FEATURES

- **High speed - 55 / 70 / 85 / 100ns**
- **Low power consumption**
  - **Active 275mW (Typ.)**
  - **Stand-by 10μW (Typ.)**
- **Battery back up (L/LL-part)**
  - **2.0V data retention**
- **Fully static operation**
  - **No clock or refresh required**
- **TTL compatible inputs and outputs**
- **Tri-state output**
- **High reliability 600 mil 32 pin PDIP, 440 mil 32 pin SOP and 400 mil TSOP-II**

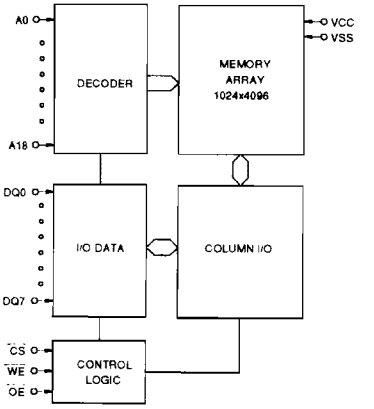
PIN CONNECTION



PIN DESCRIPTION

$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
A0-A18	Address Input
DQ0-DQ7	Data Input/Output
VCC	Power(+ 5V)
VSS	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS NOTE 1

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}, V_{IN}, V_{OUT}	Power Supply, Input/Output Voltage	– 0.5 to 7.0	V
T_{BIAS}	Temperature under Bias	– 10 to 125	°C
T_{STG}	Storage Temperature	– 55 to 125	°C
P_D	Power Dissipation	1.0	W
I_{OUT}	Data Output Current	50	mA
T_{SOLDER}	Lead Soldering Temperature & Time	260•10	°C•sec

NOTE :

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating range of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	–0.3(1)	-	0.8	V

NOTE :

1. V_{IL}= –3.0V for pulse width less than 30ns.

TRUTH TABLE

MODE	DQ OPERATION	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$
Standby	High-Z	H	X	X
Output Disabled	High-Z	L	H	H
Read	Data Out	L	H	L
Write	Data In	L	L	X

NOTE : H= V_{IH}, L= V_{IL}, X= Don't Care.

DC CHARACTERISTICS

(T_A= 0°C to 70°C, V_{CC}= 5V± 10%)

SYMBOL	PARAMETER	TEST CONDITIONS	POWER	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{SS} \leq V_{IN} \leq V_{CC}$		-2	-	2	μA
I_{LO}	Output Leakage Current	$V_{SS} \leq V_{OUT} \leq V_{CC}$ Output Disabled		-2	-	2	μA
I_{CC}	Static Operating Current	V_{CC}= MAX., $I_{I/O}$= 0mA f= 0, $\overline{CS}$= V_{IL}		-	-	40	mA
I_{CC1}	Dynamic Operating Current	Min. Duty Cycle= 100% $\overline{CS}$= V_{IL} V_{IN}= V_{IH} or V_{IL}, $I_{I/O}$= 0mA		-	55	90	mA
I_{SB}	TTL Standby Current (TTL Inputs)	V_{CC}= MAX., V_{IN}= V_{IH} or V_{IL}, $\overline{CS}$= V_{IH}, f= 0		-	-	3	mA
I_{SB1}	CMOS Standby Current (CMOS Inputs)	V_{CC}= MAX., f= 0		-	-	2	mA
		$\overline{CS} \geq V_{CC}$- 0.2V, $V_{IN} \geq V_{CC}$- 0.2V or $V_{IN} \leq$ 0.2V	L	-	2	100	μA
			LL	-	2	50	
V_{OL}	Output Low Voltage	I_{OL}= 2.1mA		-	-	0.4	V
V_{OH}	Output High Voltage	I_{OH}= -1.0mA		2.4	-	-	V

AC CHARACTERISTICS

(TA= 0°C to 70°C)

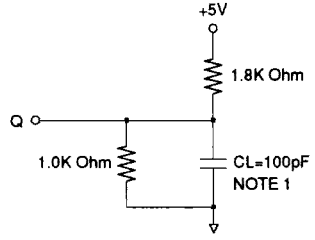
#	SYMBOL	PARAMETER	HY628400								UNIT
			-55		-70		-85		-10		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
	READ CYCLE										
1	tRC	Read Cycle Time	55	-	70	-	85	-	100	-	ns
2	tAA	Address Access Time	-	55	-	70	-	85	-	100	ns
3	tACS	Chip Select Access Time	-	55	-	70	-	85	-	100	ns
4	tOE	Output Enable to Output Valid	-	25	-	35	-	45	-	50	ns
5	tCLZ	Chip Select to Low-Z Output	5	-	10	-	10	-	10	-	ns
6	tOLZ	Output Enable to Low-Z Output	5	-	5	-	5	-	5	-	ns
7	tCHZ	Chip Disable to High-Z Output	-	20	-	25	-	30	-	35	ns
8	tOHZ	Output Disable to High-Z Output	-	20	-	25	-	30	-	35	ns
9	tOH	Output Hold from Address Change	5	-	10	-	10	-	10	-	ns
	WRITE CYCLE										
10	tWC	Write Cycle Time	55	-	70	-	85	-	100	-	ns
11	tCW	Chip Select to Write End	50	-	60	-	75	-	80	-	ns
12	tAW	Address Valid to Write End	50	-	60	-	75	-	80	-	ns
13	tAS	Address Set-up Time	0	-	0	-	0	-	0	-	ns
14	tWP	Write Pulse Width	40	-	50	-	55	-	60	-	ns
15	tWR	Write Recovery Time	5	-	5	-	5	-	5	-	ns
16	tWHZ	Write to High-Z Output	-	20	-	25	-	30	-	35	ns
17	tDW	Data to Write Time Overlap	25	-	30	-	35	-	40	-	ns
18	tDH	Data Hold from Write End	0	-	0	-	0	-	0	-	ns
19	tOW	Output Active from Write End	5	-	5	-	5	-	5	-	ns

AC TEST CONDITIONS

(TA= 0°C to 70°C)

Parameter	Value
Input Pulse Level	0.8V to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	1.5V

AC TEST LOADS



NOTE:
1. Including jig and scope capacitance.

CAPACITANCE

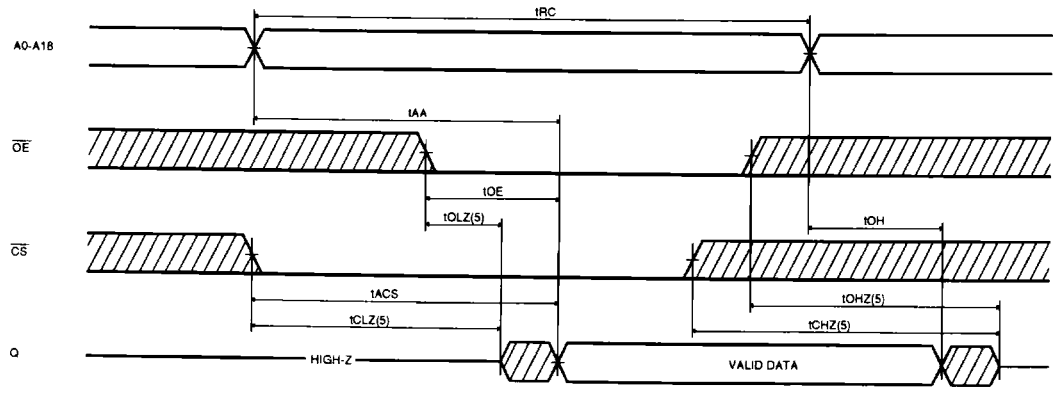
(TA= 25°C, f= 1MHz).

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
CIN	Input Capacitance	VIN= 0V	8	pF
CI/O	Input/Output Capacitance	VI/O= 0V	10	pF

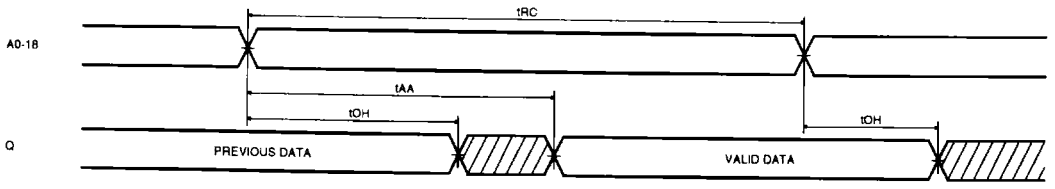
NOTE: This parameter is determined by device characterization but is not production tested.

TIMING DIAGRAM

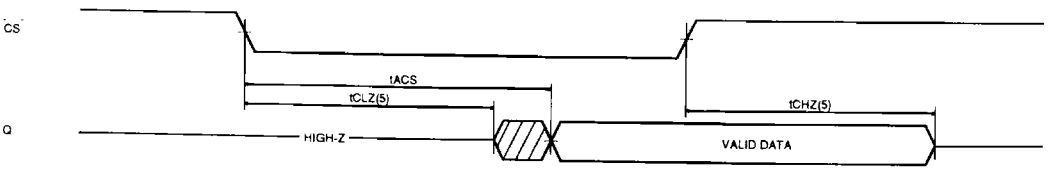
READ CYCLE 1 NOTE 1



READ CYCLE 2 NOTE 1, 2, 4

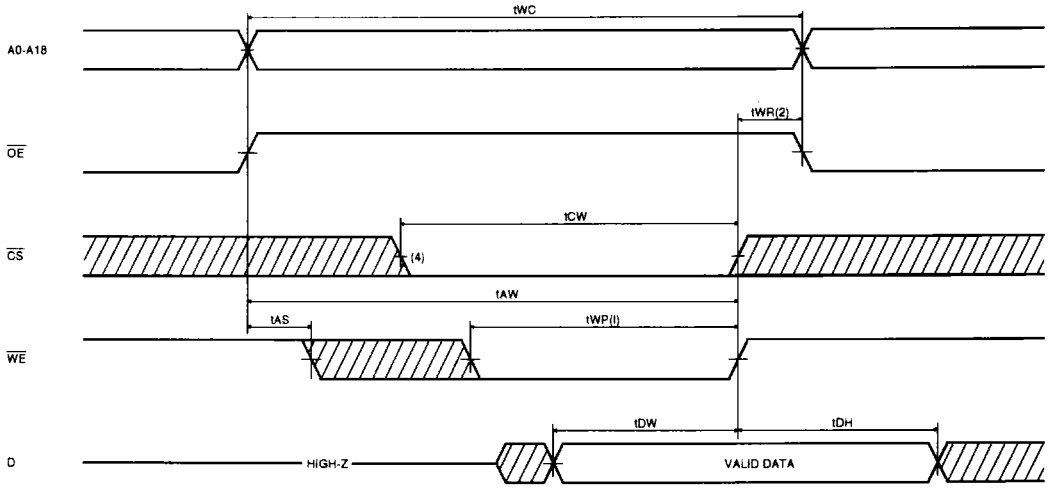


READ CYCLE 3 NOTE 1, 3, 4

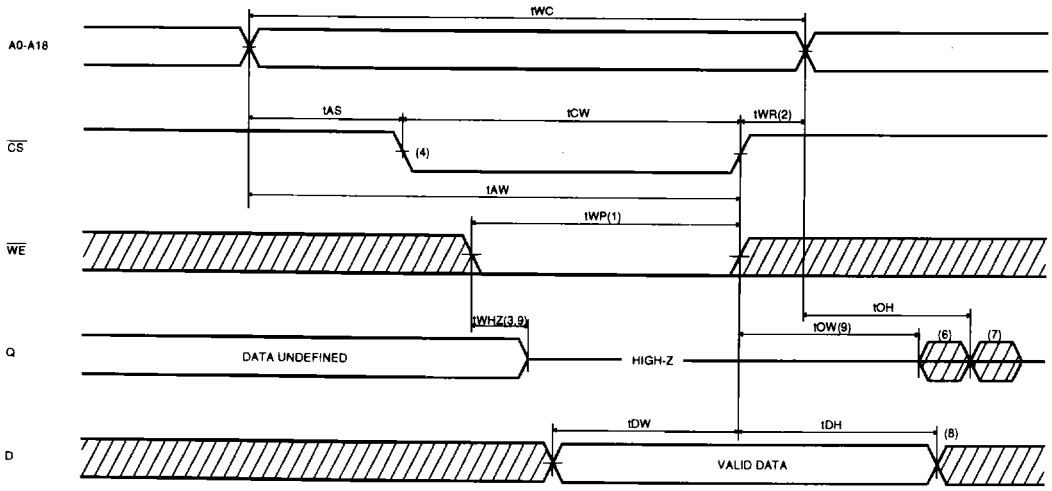


NOTES :
1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected $\overline{CS}$= VIL.
3. Addresses are valid prior to coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$= VIL.
5. Transition is measured ± 500mV from steady state.
   This parameter is sampled and not 100% tested.

WRITE CYCLE 1



WRITE CYCLE 2



NOTES :

1. A write occurs during the overlap (tWP) of low $\overline{CS}$ and low $\overline{WE}$.
2. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high at the end of write cycle.
3. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low Transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
5. $\overline{OE}$ is continuously low ($\overline{OE}$= VIL).
6. Q is the same phase of write data of this write cycle.
7. Q is the read data of next address.
8. If $\overline{CS}$ is low during this period, DQ pins are in the output state.
   Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ± 500mV from steady state.
   This parameter is sampled and not 100% tested.

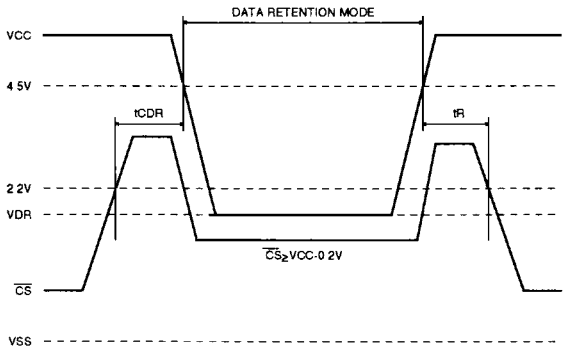
DATA RETENTIOSN CHARACTERISTICS NOTE 1

(TA= 0°C to 70°C)

SYMBOL	PARAMETER	TEST CONDITION	POWER	MIN.	TYP.[2]	MAX.	UNIT
VDR	Vcc for retention of data	$\overline{CS}$ ≥ Vcc-0.2V, Vss≤ Vin≤ Vcc		2.0	-	-	V
Iccdr	Data Retention Current	Vcc= 3.0V, $\overline{CS}$ ≥ Vcc-0.2V, Vss≤ Vin≤ Vcc	L	-	2	50	µA
			LL	-	2	30	µA
tcdr	Chip Disable to Data Retention Time	See Data Retention Timing Diagram		0	-	-	ns
tR	Operating Recovery Time	See Timing Diagram		tRC[3]	-	-	ns

NOTES :
1. These characteristics are only applied to L/LL-parts.
2. Typical values are at the condition of TA= 25°C.
3. tRC is Read Cycle Time.

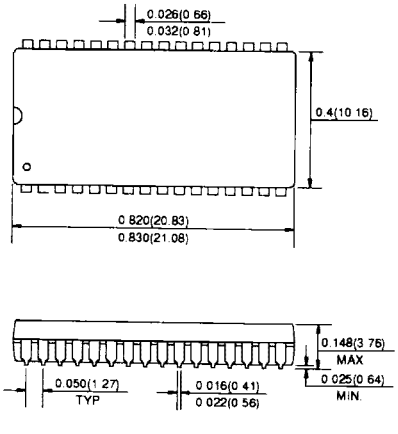
DATA RETENTION TIMING DIAGRAM



PACKAGE INFORMATION

400 mil 32 pin Small Outline Package

UNIT : INCH(mm)



ORDERING INFORMATION

PART NO	SPEED	POWER	PACKAGE	PART NO	SPEED	POWER	PACKAGE
HY628400P	55/70/85/100		PDIP	HY628400GC	55/70/85/100		SOP
HY628100LP	55/70/85/100	L-part	PDIP	HY628400LGC	55/70/85/100	L-part	SOP
HY628400LLP	55/70/85/100	LL-part	PDIP	HY628400LLGC	55/70/85/100	LL-part	SOP
HY628400TC	55/70/85/100		TSOP-II	HY628400RC	55/70/85/100		TSOP-II(R)
HY628400LTC	55/70/85/100	L-part	TSOP-II	HY628400LRC	55/70/85/100	L-part	TSOP-II(R)
HY628400LLJC	55/70/85/100	LL-part	TSOP-II	HY628400LLRC	55/70/85/100	LL-part	TSOP-II(R)