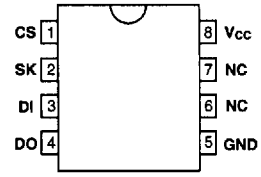
1,024-Bit Serial Electrically Erasable PROM
with 2V Read Capability

FEATURES

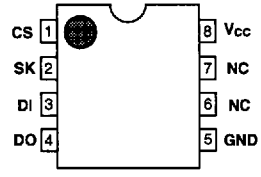
- 2.7 to 5.5V Operation (XL93LC46)
  4.5 to 5.5V Operation (XL93LC46A)
- Extended Temperature Range: -40°C to +85°C
- State-of-the-Art Architecture
  - Nonvolatile data storage
  - Fully TTL compatible inputs and outputs
  - Auto increment for efficient data dump
- Hardware and Software Write Protection
  - Defaults to write-disabled state at power up
  - Software instructions for write-enable/disable
  - Vcc lockout inadvertent write protection (XL93LC46A)
- Low Power Consumption
  - 1mA active (typical)
  - 1µA standby (typical)
- Low Voltage Read Operations
  - Reliable read operations down to 2.0 volts
- Advanced Low Voltage CMOS E^2PROM Technology
- Versatile, Easy-to-Use Interface
  - Self-timed programming cycle
  - Automatic erase-before-write
  - Programming Status Indicator
  - Word and chip erasable
- Durable and Reliable
  - 10-year data retention after 100K write cycles
  - Minimum of 100,000 write cycles per word
  - Unlimited read cycles
  - ESD protection (EIAJ and JEDEC standard)

PIN CONFIGURATIONS

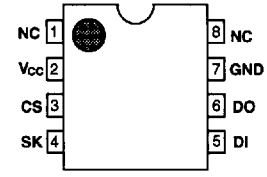
Plastic Dual-in-line "P" Package



EIAJ Small Outline "RF" Package



EIAJ Small Outline "F" Package



PIN NAMES

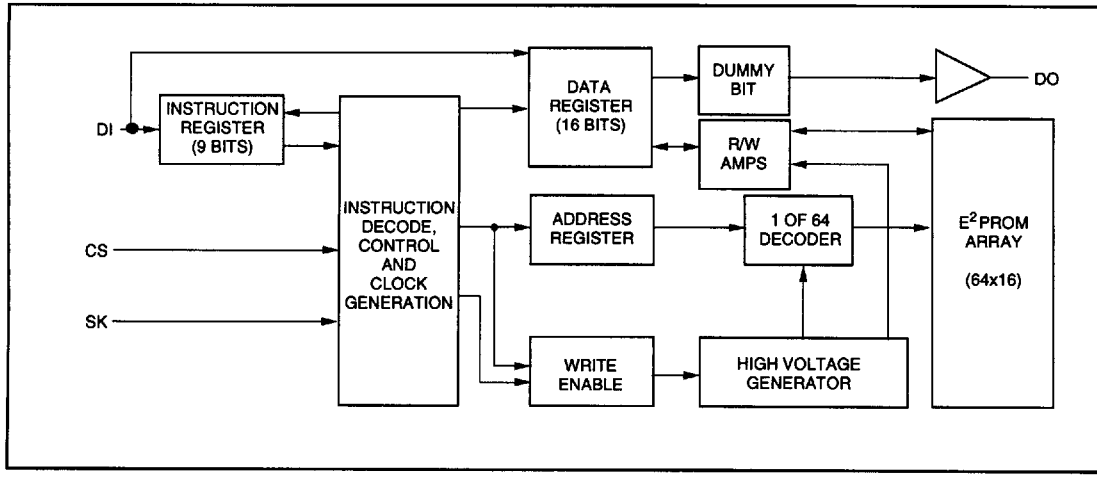
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
Vcc	Power Supply
NC	Not Connected

OVERVIEW

The XL93LC46/46A is a cost effective 1,024-bit, nonvolatile, serial E^2PROM. It is fabricated using EXEL's advanced CMOS E^2PROM technology. The XL93LC46/46A provides efficient nonvolatile read/write memory arranged as 64 registers of 16 bits each. Seven 9-bit instructions control the operation of the device, which include read, write, and mode enable functions. The data output pin (DO) indicates the status of the device during the self-timed nonvolatile programming cycle.

The self-timed write cycle includes an automatic erase-before-write capability. To protect against inadvertent writes, the WRITE instruction is accepted only while the chip is in the write enabled state. Data is written in 16 bits per write instruction into the selected register. If Chip Select (CS) is brought HIGH after initiation of the write cycle, the Data Output (DO) pin will indicate the READY/BUSY status of the chip.

BLOCK DIAGRAM



APPLICATIONS

The XL93LC46/46A is ideal for high volume applications requiring low power and low density storage. This device uses a cost effective, space saving 8-pin package. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation settings.

ENDURANCE AND DATA RETENTION

The XL93LC46/46A is designed for applications requiring up to 100,000 write cycles per bit. It provides 10 years of secure data retention without power after the execution of 100,000 write cycles for each location.

DEVICE OPERATION

The XL93LC46/46A is controlled by seven 9-bit instructions. Instructions are clocked in (serially) on the DI pin. Each instruction begins with a logical "1" (the start bit). This is followed by the opcode (2 bits), the address field (6 bits), and data, if appropriate. The clock signal (SK) may be halted at any time and the XL93LC46/46A will remain in its last state. This allows full static flexibility and maximum power conservation.

Read (READ)

The READ instruction is the only instruction that results in serial data on the DO pin. After the read instruction and address have been decoded, data is transferred from the selected memory register into a 16-bit serial shift register. (Please note that one logical "0" bit precedes the actual 16-bit output data string.) The output on DO changes during the LOW-TO-HIGH transitions of SK. (See Figure 2.)

Low Voltage Read

The XL93LC46/46A has been designed to ensure that data read operations are reliable in low voltage environments. The XL93LC46/46A is guaranteed to provide accurate data during read operations with V_{CC} as low as 2.0V.

Auto Increment Read Operations

In order to facilitate memory transfer operations, the XL93LC46/46A has been designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 16 bits of the addressed word have been clocked out, the data in consecutively higher address locations is output. The address will wrap around continuously with CS HIGH until the Chip Select control pin is brought LOW. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

Write Enable (WEN)

The write enable (WEN) instruction must be executed before any device programming can be done. When V_{CC} is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter the device remains enabled until a WDS instruction is executed or until V_{CC} is removed. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction. See Figure 3.)

Write (WRITE)
The WRITE instruction includes 16 bits of data to be written into the specified register. After the last data bit has been clocked into DI, and before the next rising edge of SK, CS must be brought LOW. The falling edge of CS initiates the self-timed programming cycle.

After a minimum wait of 250ns from the falling edge of CS (t_{CS}), if CS is brought HIGH, DO will indicate the READY/$\overline{\text{BUSY}}$ status of the chip: logical "0" means programming is still in progress; logical "1" means the selected register has been written, and the part is ready for another instruction. (See Figure 4.) (NOTE: The combination of CS HIGH, DI HIGH and the rising edge of the SK clock, resets the READY/$\overline{\text{BUSY}}$ flag. Therefore, it is important not to reset the READY/$\overline{\text{BUSY}}$ flag through this combination of control signals, if you want to access it.) Before a WRITE instruction can be executed, the device must be write enabled (see WEN).

Write All (WRALL)
The write all (WRALL) instruction programs all registers with the data pattern specified in the instruction.

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (t_{CS}), the DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the chip. (See Figure 5.)

Write Disable (WDS)
The write disable (WDS) instruction disables all programming capabilities. This protects the entire memory array against accidental modification of data until a WEN instruction is executed. (When V_{CC} is applied, the part powers up in the write disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction. See Figure 6.)

Erase Register
After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of t_{CS} will cause DO to indicate the READY/$\overline{\text{BUSY}}$ status of the chip: a logical "0" indicates programming is still in progress; a logical "1" indicates the erase cycle is complete and the part is ready for another instruction. (See Figure 7.) Erase of a register sets all of the bits of the register to a logical "1".

Erase All (ERAL)
Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1". (See Figure 8.)

V_{CC} Lockout - Inadvertent Write Protection (XL93LC46A only)
To ensure against inadvertent write operation, the XL93LC46A has been equipped with an internal V_{CC} sensor circuit which inhibits data alteration when the supply voltage (V_{CC}) falls below V_{WI}. If the applied V_{CC} is below 3.75V (typical), the XL93LC46A is inhibited from executing write operations thereby protecting the non-volatile data from inadvertent write operations.

XL93LC46/46A INSTRUCTION SET

Instruction	Start Bit	OP Code	Address	Input Data
READ	1	10	(A_5-A_0)	
WEN (Write Enable)	1	00	11XXXX	
WRITE	1	01	(A_5-A_0)	D_{15}-D_0
WRALL (Write All Registers)	1	00	01XXXX	D_{15}-D_0
WDS (Write Disable)	1	00	00XXXX	
ERASE	1	11	(A_5-A_0)	
ERAL (Erase All Registers)	1	00	10XXXX	

ABSOLUTE MAXIMUM RATINGS

Temperature under bias: ..... -40°C to +85°C
Storage Temperature ..... -65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin ..... -0.3 to Vcc + 0.3V
ESD Rating 2000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may adversely affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = -40°C to +85°C

Symbol	Parameter	Conditions	XL93LC46 Vcc = 3.0V±10%		XL93LC46/46A Vcc = 5.0V±10%		XL93LC46/46A Vcc = 2.0V (Read Only)		Units
			Min	Max	Min	Max	Min	Max	
I_{CC1}	Operating Current CMOS Input Levels	CS = V_{CC}, SK = 250KHz		2		2		2	mA
I_{CC2}	Operating Current TTL Input Levels	CS = V_{IH}, SK = 1MHz		n/a		5		n/a	mA
I_{SB}	Standby Current	CS = DI = SK =0V		2		2		2	µA
I_{LI}	Input Leakage	V_{IN} = 0V to V_{CC} (CS, SK, DI)	-1	1	-1	1	-1	1	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc, CS = 0V	-1	1	-1	1	-1	1	µA
V_{IL}	Input Low Voltage		-0.1	0.15V_{CC}	-0.1	0.8	-0.1	0.1 V_{CC}	V
V_{IH}	Input High Voltage		0.8 V_{CC}	V_{CC}+0.2	2	V_{CC}+0.2	0.9 V_{CC}	V_{CC}+0.2	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1mA TTL		n/a		0.4		n/a	V
V_{OH1}	Output High Voltage	I_{OH} = -400µA TTL	n/a		2.4		n/a		V
V_{OL2}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2		0.2	V
V_{OH2}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc-0.2		Vcc-0.2		Vcc-0.2		V
V_{WI}	Write Inhibit Threshold		n/a	n/a	2.7	4.4	n/a	n/a	V

AC ELECTRICAL CHARACTERISTICS

T_A = -40°C to +85°C

Symbol	Parameter	Conditions	XL93LC46 Vcc = 3.0V±10%		XL93LC46/46A Vcc = 5.0V±10%		XL93LC46/46A Vcc = 2.0V (Read Only)		Units
			Min	Max	Min	Max	Min	Max	
fSK	SK Clock Frequency		0	250	0	1000	0	250	KHz
tSKH	SK High Time		1000		400		2000		ns
tSKL	SK Low Time		1000		250		2000		ns
tCS	Minimum CS Low Time		1000		250		1000		ns
tCSS	CS Setup Time	Relative to SK ⌐	200		50		200		ns
tDIS	DI Setup Time	Relative to SK ⌐	400		100		400		ns
tCSH	CS Hold Time	Relative to SK ¬	0		0		0		ns
tDIH	DI Hold Time	Relative to SK ⌐	400		100		400		ns
tPD1	Output Delay to "1"	AC Test		2000		500		2000	ns
tPD0	Output Delay to "0"	AC Test		2000		500		2000	ns
tSV	CS to Status Valid	AC Test CL = 100pF		2000		500		2000	ns
tDF	CS to DO in 3-state	CS = Low to DO = Hi-Z		400		100		400	ns
tWP	Write Cycle Time	CS = Low to DO = Ready		25		10		n/a	ms

CAPACITANCE
T_A = 25°C, f = 250KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	5	pF

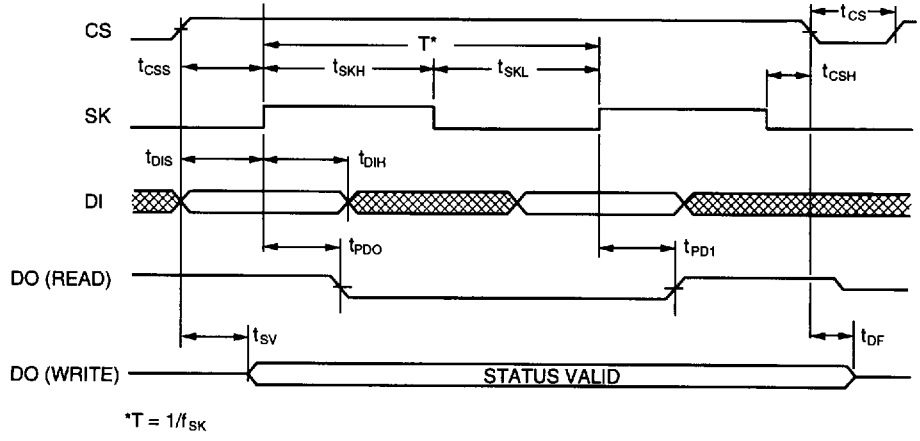
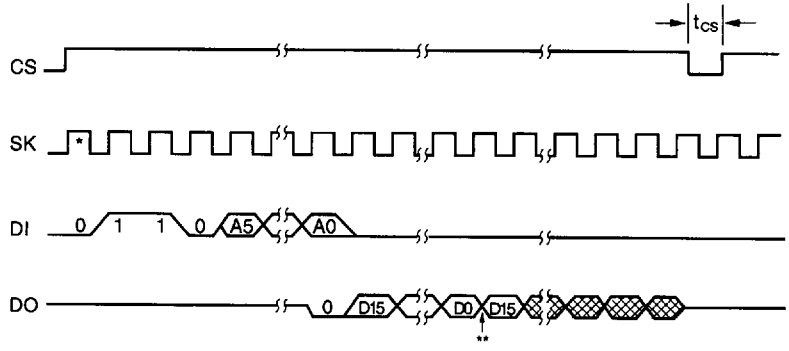
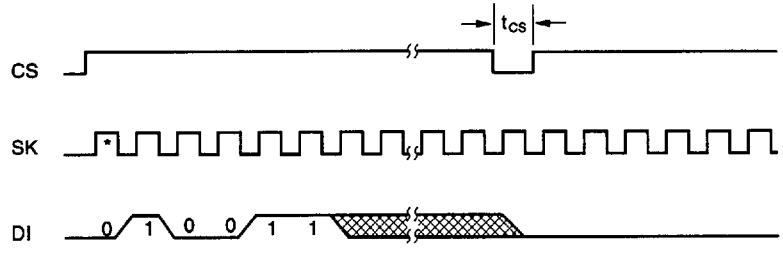


FIGURE 1. SYNCHRONOUS DATA TIMING



* This leading clock is optional.
**Address pointer automatically cycles to the next register.

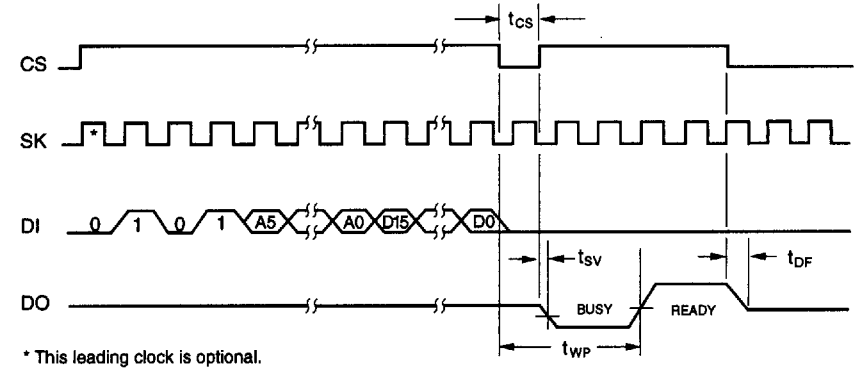
FIGURE 2. READ CYCLE TIMING



DO = 3-state

* This leading clock is optional.

FIGURE 3. WRITE ENABLE (WEN) CYCLE TIMING



* This leading clock is optional.

FIGURE 4. WRITE CYCLE TIMING

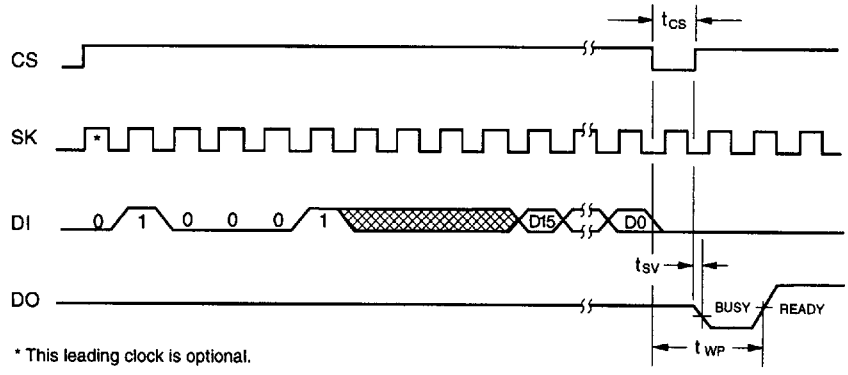


FIGURE 5. WRITE ALL (WRALL) CYCLE TIMING

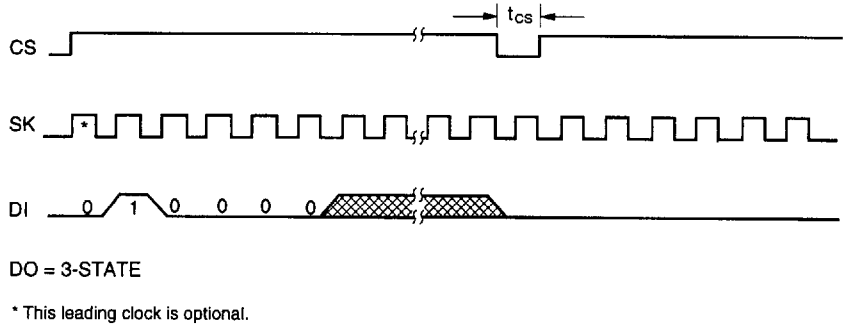
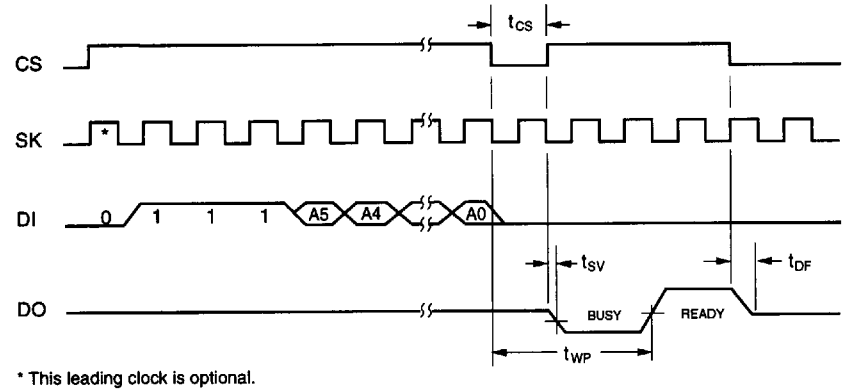
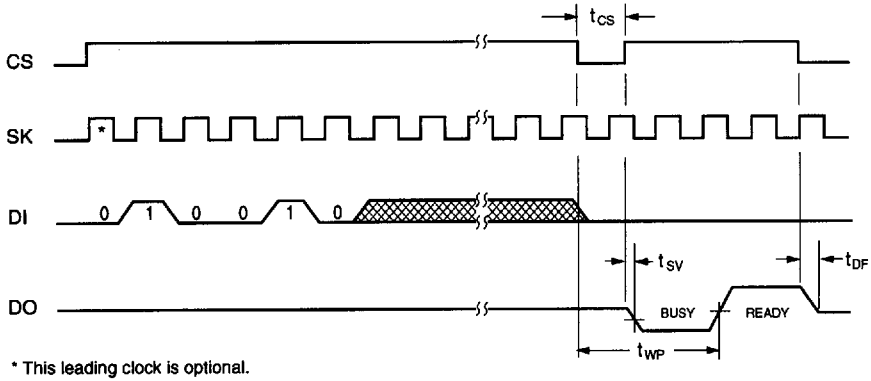


FIGURE 6. WRITE DISABLE (WDS) CYCLE TIMING



* This leading clock is optional.

FIGURE 7. ERASE (REGISTER) CYCLE TIMING



* This leading clock is optional.

FIGURE 8. ERASE ALL (ERAL) CYCLE TIMING