

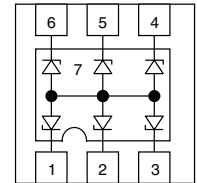
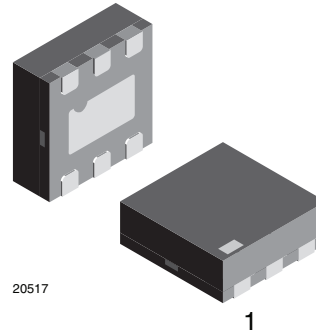
6-Line ESD-Protection Diode Array in LLP75

Features

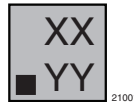
- Ultra compact LLP75-7L package
- 6-line ESD-protection
- Low leakage current $I_R < 1 \mu\text{A}$
- Low load capacitance $C_D = 40 \text{ pF}$
- ESD-immunity acc. IEC 61000-4-2
 $\pm 30 \text{ kV}$ contact discharge
 $\pm 30 \text{ kV}$ air discharge
- Working voltage range $V_{RWM} = 5 \text{ V}$
- e4 - precious metal (e.g. Ag, Au, NiPd, NiPdAu) (no Sn)
- Compliant to RoHS directive 2002/95/EC and in accordance to WEEE 2002/96/EC



RoHS
COMPLIANT
GREEN
(5-2008)**



Marking (example only)



Dot = Pin 1 marking
 XX = Date code
 YY = Type code (see table below)

Ordering Information

Device name	Ordering code	Taped units per reel (8 mm tape on 7" reel)	Minimum order quantity
VESD05A6-HAF	VESD05A6-HAF-GS08	3000	15000

Package Data

Device name	Package name	Type code	Weight	Molding compound flammability rating	Moisture sensitivity level	Soldering conditions
VESD05A6-HAF	LLP75-7L	AS	4.2 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	260 °C/10 s at terminals

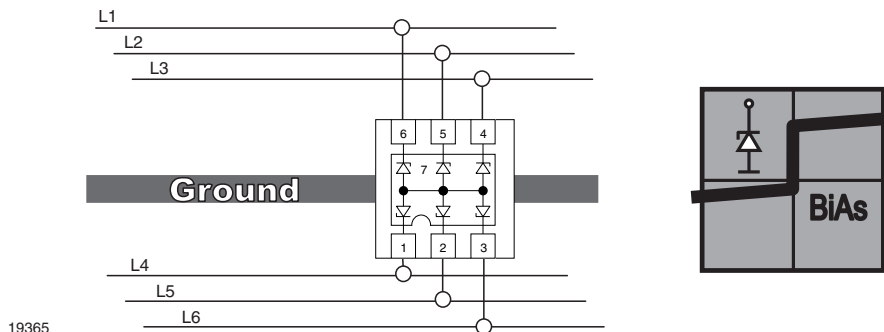
** Please see document "Vishay Material Category Policy" www.vishay.com/doc?99902

Absolute Maximum Ratings

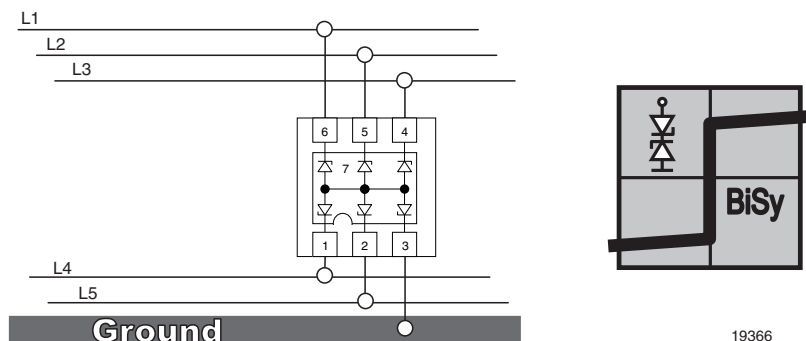
Rating	Test condition	Symbol	Value	Unit
Peak pulse current	BiAs-Mode: each input (pin 1 to pin 6) to ground (pin 2); acc. IEC 61000-4-5; $t_p = 8/20 \mu s$; single shot	I_{PPM}	5	A
Peak pulse power	BiAs-mode: each input (pin 1 to pin 6) to ground (pin 2); acc. IEC 61000-4-5; $t_p = 8/20 \mu s$; single shot	P_{PP}	60	W
ESD immunity	Acc. IEC61000-4-2; 10 pulses BiAs-mode: each input (pin 1 to pin 6) to ground (pin 2)	Contact discharge	V_{ESD}	± 30 kV
		Air discharge	V_{ESD}	± 30 kV
Operating temperature	Junction temperature	T_J	- 40 to + 125	$^{\circ}C$
Storage temperature		T_{STG}	- 55 to + 150	$^{\circ}C$

Application Note:

- a) With the **VESD05A6-HAF** 6 different signal or data lines can be clamped to ground. Due to the different clamping levels in forward and reverse direction the **VESD05A6-HAF** clamping behavior is **B**idirectional and **A**symmetrical (**BiAs**).



- b) If symmetrical clamping behaviour is required the **VESD05A6-HAF** can also be used as a **B**idirectional **S**ymmetrical protection device protecting up to 5 lines. In this case pin 7 must not be connected.



Electrical Characteristics

Ratings at 25 °C, ambient temperature unless otherwise specified

VESD05A6-HAF

BiAs mode (between pin 1, 2, 3, 4, 5 or 6 and pin 7)

Parameter	Test conditions/remarks	Symbol	Min.	Typ.	Max.	Unit
Protection paths	Number of lines which can be protected	N_{lines}			6	lines
Reverse stand off voltage	at $I_R = 1 \mu A$	V_{RWM}	5			V
Max. reverse current	at $V_R = 5 V$	I_R		< 0.1	1	μA
Reverse break down voltage	at $I_R = 1 mA$	V_{BR}	6	6.6	7.5	V
Reverse clamping voltage	at $I_{PP} = 1 A$	V_C		8.1	10	V
	at $I_{PP} = I_{PPM} = 5 A$	V_C		11.3	12	V
Forward clamping voltage	at $I_{PP} = 1 A$	V_F		1.5	1.8	V
	at $I_{PP} = I_{PPM} = 5 A$	V_F		3.2	4.5	V
Line capacitance	at $V_R = 0 V$; $f = 1 MHz$	C_D		40	50	pF
	at $V_R = 2.5 V$; $f = 1 MHz$	C_D		24		pF

Typical Characteristics

$T_{amb} = 25 \text{ }^\circ\text{C}$, unless otherwise specified

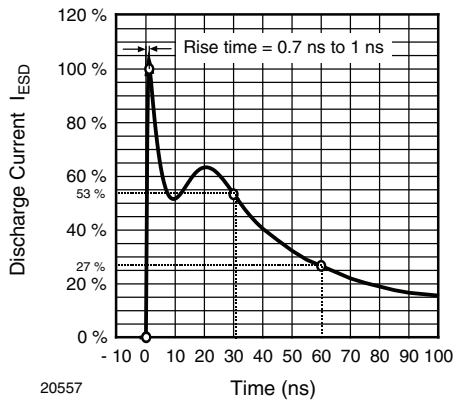


Figure 1. ESD Discharge Current Wave Form
acc. IEC 61000-4-2 (330 Ω /150 pF)

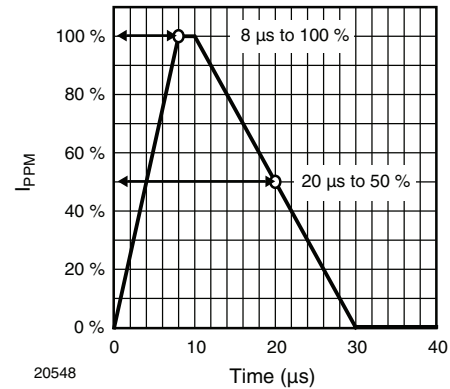


Figure 2. 8/20 μs Peak Pulse Current Wave Form
acc. IEC 61000-4-5

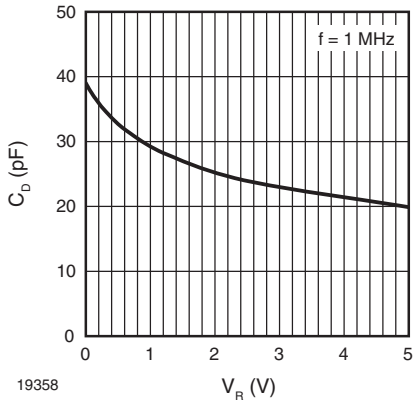


Figure 3. Typical Capacitance C_D vs. Reverse Voltage V_R

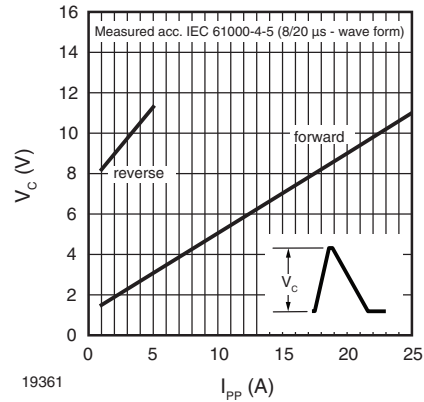


Figure 6. Typical Clamping Voltage vs. Peak Pulse Current I_{PP}

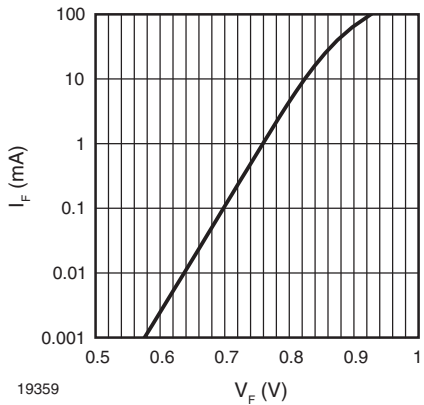


Figure 4. Typical Forward Current I_F vs. Forward Voltage V_F

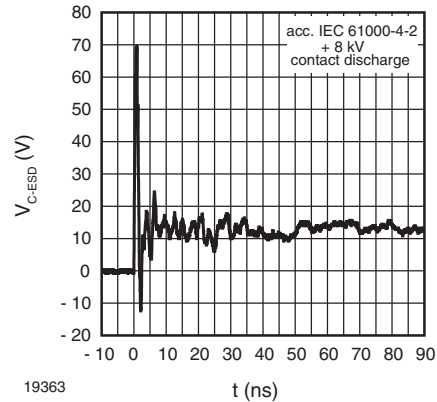


Figure 7. Typical Clamping Performance on +8 kV - ESD Events (acc. IEC 61000-4-2)

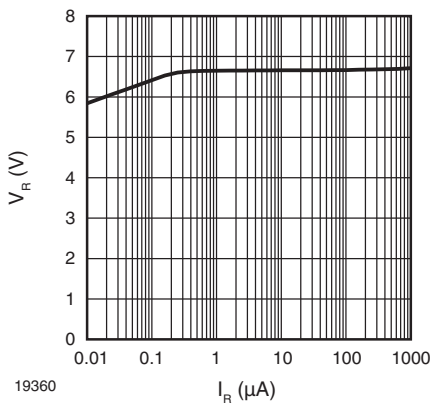


Figure 5. Typical Reverse Voltage V_R vs. Reverse Current I_R

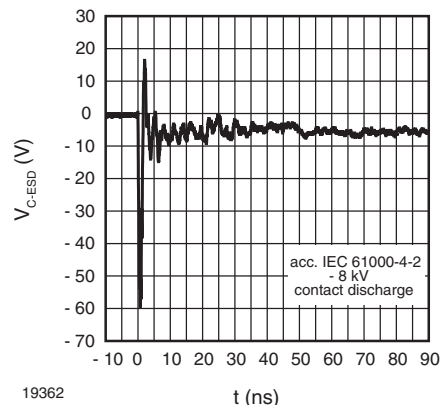


Figure 8. Typical Clamping Performance on -8 kV - ESD Events (acc. IEC 61000-4-2)

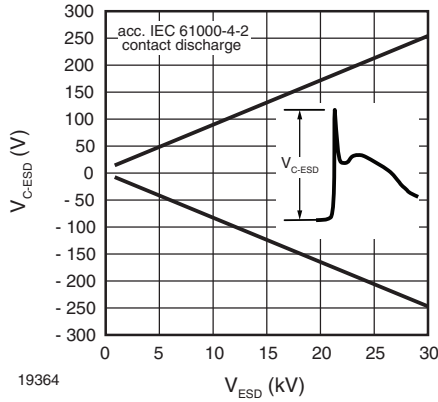
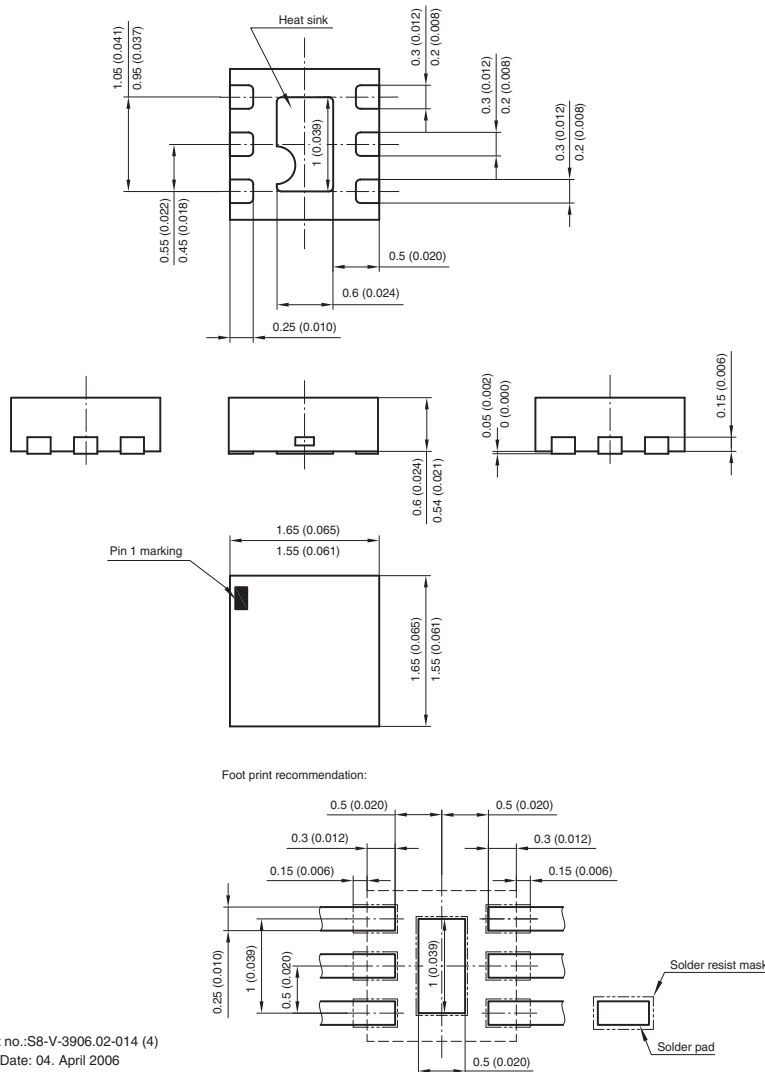


Figure 9. Typical max. Clamping Voltage at ESD Contact Discharge (acc. IEC 61000-4-2)

Package Dimensions in millimeters (inches): LLP75-7L





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