

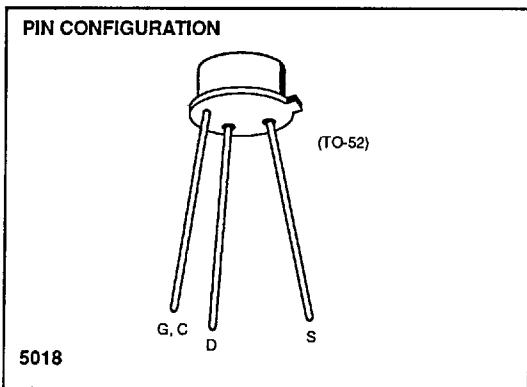
N-Channel JFET Switch



2N5432 – 2N5434

FEATURES

- Low $I_{DS(on)}$
- Excellent Switching
- Low Cutoff Current



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source Voltage -25V
Gate-Drain Voltage -25V
Gate Current 100mA
Drain Current 400mA
Storage Temperature Range -65°C to $+200^\circ\text{C}$
Operating Temperature Range -55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10sec) $+300^\circ\text{C}$
Power Dissipation 300mW
Derate above 25°C $2.3\text{mW}/^\circ\text{C}$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

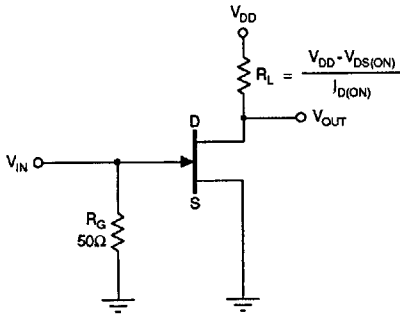
Part	Package	Temperature Range
2N5432-34	Hermetic TO-52	-55°C to $+150^\circ\text{C}$
X2N5432-34	Sorted Chips in Carriers	-55°C to $+150^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

SYMBOL	PARAMETER	2N5432		2N5433		2N5434		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
I_{GSS}	Gate Reverse Current		-200		-200		-200	pA	$V_{GS} = -15\text{V}$, $V_{DS} = 0$
			-200		-200		-200	nA	$T_A = 150^\circ\text{C}$
BV_{GSS}	Gate-Source Breakdown Voltage	-25		-25		-25		V	$I_G = -1\mu\text{A}$, $V_{DS} = 0$
$I_{D(off)}$	Drain Cutoff Current		200		200		200	pA	$V_{DS} = 5\text{V}$, $V_{GS} = -10\text{V}$
			200		200		200	nA	$T_A = 150^\circ\text{C}$
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4	-10	-3	-9	-1	-4	V	$V_{DS} = 5\text{V}$, $I_D = 3\text{nA}$
I_{DSS}	Saturation Drain Current (Note 1)	150		100		30		mA	$V_{DS} = 15\text{V}$, $V_{GS} = 0$
$r_{DS(on)}$	Static Drain-Source ON Resistance	2	5		7		10	ohm	$V_{GS} = 0$, $I_D = 10\text{mA}$
$V_{DS(on)}$	Drain-Source ON Voltage		50		70		100	mV	
$r_{ds(on)}$	Drain-Source ON Resistance		5		7		10	ohm	$V_{GS} = 0$, $I_D = 0$ $f = 1\text{kHz}$
C_{iss}	Common-Source Input Capacitance (Note 2)		30		30		30	pF	$V_{DS} = 0$, $V_{GS} = -10\text{V}$ $f = 1\text{MHz}$
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 2)		15		15		15	pF	
t_d	Turn-ON Delay Time (Note 2)		4		4		4	ns	$V_{DD} = 1.5\text{V}$, $V_{GS(on)} = 0$, $V_{GS(off)} = -12\text{V}$, $I_{D(on)} = 10\text{mA}$
t_r	Rise Time (Note 2)		1		1		1		
t_{off}	Turn-OFF Delay Time (Note 2)		6		6		6		
t_f	Fall Time (Note 2)		30		30		30		

NOTES: 1. Pulse test required, pulsewidth 300 μs , duty cycle $\leq 3\%$.
2. For design reference only, not 100% tested.

SWITCHING TIME, TEST CIRCUIT



INPUT PULSE

RISE TIME 0.25ns
FALL TIME 0.75ns
PULSE WIDTH 200ns
PULSE RATE 550pps

SAMPLING SCOPE

RISE TIME 0.4ns
INPUT RESISTANCE 10MΩ
INPUT CAPACITANCE 1.5pF

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