HARRIS

# 82C84A

## CMOS Clock Generator Driver

### Features

- Generates the System Clock For CMOS or NMOS Microprocessors
- Up to 25MHz Operation
- Uses a Parallel Mode Crystal Circuit or External Frequency Source
- Provides Ready Synchronization
- Generates System Reset Output From Schmitt Trigger Input
- Capable of Clock Synchronization With Other 82C84As
- TTL Compatible Inputs/Outputs
- Very Low Power Consumption
- Single +5V Power Supply
- Wide Operating Temperature Ranges:
  - C82C84A ..... 0°C to +70°C
  - I82C84A ..... -40°C to +85°C
  - M82C84A ..... -55°C to +125°C

### Description

The Harris 82C84A is a high performance CMOS clock generator-driver which is designed to service the requirements of both CMOS and NMOS microprocessors such as the 80C86, 80C88, 8086 and the 8088. The chip contains a crystal controlled oscillator, a divide-by-three counter and complete "Ready" synchronization and reset logic.

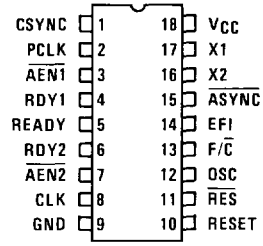
Static CMOS circuit design permits operation with an external frequency source from DC to 25MHz. Crystal controlled operation to 25MHz is guaranteed with the use of a parallel, fundamental mode crystal and two small load capacitors.

All inputs (except X1, and $\overline{RES}$) are TTL compatible over temperature and voltage ranges.

Power consumption is a fraction of that of the equivalent bipolar circuits. This speed-power characteristic of CMOS permits the designer to custom tailor his system design with respect to power and/or speed requirements.

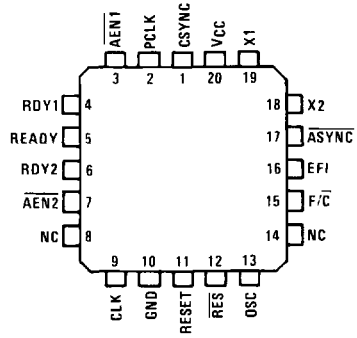
### Pinouts

TOP VIEW

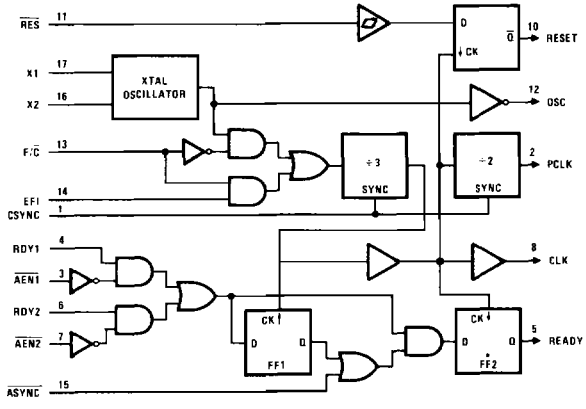



LCC/PLCC

TOP VIEW




### Block Diagram




| CONTROL PIN | LOGICAL1 | LOGICAL0 |
|---|---|---|
| F/$\overline{C}$ | External Clock | Crystal Drive |
| $\overline{RES}$ | Normal | Reset |
| RDY1<br>RDY2 | Bus Ready | Bus Not Ready |
| $\overline{AEN1}$<br>$\overline{AEN2}$ | Address Disabled | Address Enabled |
| $\overline{ASYNC}$ | 1 Stage Ready Synchronization | 2 Stage Ready Synchronization |

CAUTION These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

## Pin Description

TABLE 1.

| SYMBOL | PIN NUMBER | TYPE | DESCRIPTION |
|---|---|---|---|
| $\overline{AEN1}$, $\overline{AEN2}$ | 3, 7 | I | ADDRESS ENABLE: $\overline{AEN}$ is an active LOW signal. $\overline{AEN}$ serves to qualify its respective Bus Ready Signal (RDY1 or RDY2). $\overline{AEN1}$ validates RDY1 while $\overline{AEN2}$ validates RDY2. Two AEN signal inputs are useful in system configurations which permit the processor to access two Multi-Master System Busses. In non-Multi-Master configurations, the $\overline{AEN}$ signal inputs are tied true (LOW). |
| RDY 1, RDY 2 | 4 6 | I | BUS READY (Transfer Complete). RDY is an active HIGH signal which is an indication from a device located on the system data bus that data has been received, or is available. RDY1 is qualified by AEN1 while RDY2 is qualified by AEN2. |
| $\overline{ASYNC}$ | 15 | I | READY SYNCHRONIZATION SELECT: $\overline{ASYNC}$ is an input which defines the synchronization mode of the READY logic. When $\overline{ASYNC}$ is low, two stages of READY synchronization are provided. When $\overline{ASYNC}$ is left open or HIGH a single stage of READY synchronization is provided. |
| READY | 5 | O | READY: READY is an active HIGH signal which is the synchronized RDY signal input. READY is cleared after the guaranteed hold time to the processor has been met. |
| X1, X2 | 17, 16 | I O | CRYSTAL IN: X1 and X2 are the pins to which a crystal is attached. The crystal frequency is 3 times the desired processor clock frequency.* |
| F/$\overline{C}$ | 13 | I | FREQUENCY CRYSTAL SELECT: F/$\overline{C}$ is a strapping option. When strapped LOW, F/$\overline{C}$ permits the processor's clock to be generated by the crystal. When F/$\overline{C}$ is strapped HIGH, CLK is generated from the EFI input. |
| EFI | 14 | I | EXTERNAL FREQUENCY IN: When F/$\overline{C}$ is strapped HIGH, CLK is generated from the input frequency appearing on this pin. The input signal is a square wave 3 times the frequency of the desired CLK output. |
| CLK | 8 | O | PROCESSOR CLOCK: CLK is the clock output used by the processor and all devices which directly connect to the processor's local bus. CLK has an output frequency which is 1/3 of the crystal or EFI input frequency and a 1/3 duty cycle. |
| PCLK | 2 | O | PERIPHERAL CLOCK: PCLK is a peripheral clock signal whose output frequency is 1/2 that of CLK and has a 50% duty cycle. |
| OSC | 12 | O | OSCILLATOR OUTPUT: OSC is the output of the internal oscillator circuitry. Its frequency is equal to that of the crystal. |
| $\overline{RES}$ | 11 | I | RESET IN: $\overline{RES}$ is an active LOW signal which is used to generate RESET. The 82C84A provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration. |
| RESET | 10 | O | RESET: RESET is an active HIGH signal which is used to reset the 80C86 family processors. Its timing characteristics are determined by $\overline{RES}$. |
| CSYNC | 1 | I | CLOCK SYNCHRONIZATION: CSYNC is an active HIGH signal which allows multiple 82C84As to be synchronized to provide clocks that are in phase. When CSYNC is HIGH the internal counters are reset. When CSYNC goes LOW the internal counters are allowed to resume counting. CSYNC needs to be externally synchronized to EFI. When using the internal oscillator CSYNC should be hardwired to ground. |
| GND | 9 | | Ground |
| VCC | 18 | | VCC: the +5V power supply pin. A 0.1$\mu$F capacitor between pins 18 and 9 is recommended for decoupling. |

*If the crystal inputs are not used, X1 must be tied to VCC or GND and X2 should be left open.

## Functional Description

### Oscillator

The oscillator circuit of the 82C84A is designed primarily for use with an external parallel resonant, fundamental mode crystal from which the basic operating frequency is derived.

The crystal frequency should be selected at three times the required CPU clock. X1 and X2 are the two crystal input crystal connections. For the most stable operation of the oscillator (OSC) output circuit, two capacitors (C1 = C2) as shown in the waveform figures are recommended. The output of the oscillator is buffered and brought out on OSC so that other system timing signals can be derived from this stable, crystal-controlled source.

Capacitors C1, C2 are chosen such that their combined capacitance

$$CT = \frac{C1 \times C2}{C1 + C2} \text{ (Including stray capacitance)}$$

matches the load capacitance as specified by the crystal manufacturer. This insures operation within the frequency tolerance specified by the crystal manufacturer.

### Clock Generator

The clock generator consists of a synchronous divide-by-three counter with a special clear input that inhibits the counting. This clear input (CSYNC) allows the output clock to be synchronized with an external event (such as another 82C84A clock). It is necessary to synchronize the CSYNC input to the EFI clock external to the 82C84A. This is accomplished with two flip-flops. (See Figure 1). The counter output is a 33% duty cycle clock at one-third the input frequency.

*The F/$\overline{C}$ input is a strapping pin that selects either the crystal oscillator or the EFI input as the clock for the ÷ 3 counter. If the EFI input is selected as the clock source, the oscillator section can be used independently for another clock source. Output is taken from OSC.

### Clock Outputs

The CLK output is a 33% duty cycle clock driver designed to drive the 80C86, 80C88 processors directly. PCLK is a peripheral clock signal whose output frequency is 1/2 that of CLK. PCLK has a 50% duty cycle.

### Reset Logic

The reset logic provides a Schmitt trigger input ($\overline{RES}$) and a synchronizing flip-flop to generate the reset timing. The reset signal is synchronized to the falling edge of CLK. A simple RC network can be used to provide power-on reset by utilizing this function of the 82C84A. Waveforms for clocks and reset signals are illustrated in Figure 2.

### READY Synchronization

Two READY inputs (RDY1, RDY2) are provided to accommodate two system busses. Each input has a qualifier ($\overline{AEN1}$ and $\overline{AEN2}$, respectively). The $\overline{AEN}$ signals validate their respective RDY signals. If a Multi-Master system is not being used the $\overline{AEN}$ pin should be tied LOW.

Synchronization is required for all asynchronous active-going edges of either RDY input to guarantee that the RDY setup and hold times are met. Inactive-going edges of RDY in normally ready systems do not require synchronization but must satisfy RDY setup and hold as a matter of proper system design.

The $\overline{ASYNC}$ input defines two modes of READY synchronization operation.

When $\overline{ASYNC}$ is LOW, two stages of synchronization are provided for active READY input signals. Positive-going asynchronous READY inputs will first be synchronized to flip-flop one at the rising edge of CLK (requiring a setup time $t_{R1VCH}$) and then synchronized to flip-flop two at the next falling edge of CLK, after which time the READY output will go active (HIGH). Negative-going asynchronous READY inputs will be synchronized directly to flip-flop two at the falling edge of CLK, after which time the READY output will go inactive. This mode of operation is intended for use by asynchronous (normally not ready) devices in the system which cannot be guaranteed by design to meet the required RDY setup timing, $t_{R1VCL}$, on each bus cycle. (Refer to Figure 3.)

When $\overline{ASYNC}$ is high or left open, the first READY flip-flop is bypassed in the READY synchronization logic. READY inputs are synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices that can be guaranteed to meet the required RDY setup time. (Refer to Figure 4.)

$\overline{ASYNC}$ can be changed on every bus cycle to select the appropriate mode of synchronization for each device in the system.

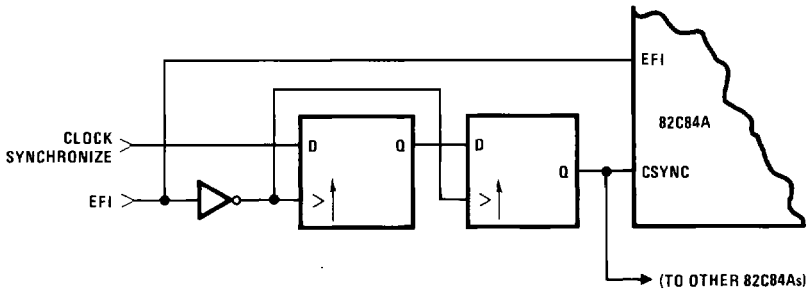



**FIGURE 1. CSYNC SYNCHRONIZATION**

*NOTE: If EFI input is used, then crystal input X1 must be tied to VCC or GND and X2 should be left open. If the crystal inputs are used then EFI should be tied to VCC or GND.

## Absolute Maximum Ratings

Supply Voltage ..... +8.0 Volts
Input, Output or I/O Voltage Applied ..... GND -0.5V to $V_{CC}$ +0.5V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
$\theta_{jc}$ ..... 28°C/W (CERDIP Package), 33°C/W (LCC Package)
$\theta_{ja}$ ..... 81°C/W (CERDIP Package), 86°C/W (LCC Package)
Gate Count ..... 50 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

*CAUTION. Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.*

## Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range
C82C84A ..... 0°C to +70°C
I82C84A ..... -40°C to +85°C
M82C84A ..... -55°C to +125°C

## D.C. Electrical Specifications

VCC = 5.0V ± 10%; $T_A$ = 0°C to +70°C (C82C84A);
$T_A$ = -40°C to +85°C (I82C84A);
$T_A$ = -55°C to +125°C (M82C84A)

| SYMBOL | PARAMETER | MIN | MAX | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|
| $V_{IH}$ | Logical One Input Voltage | 2.0<br>2.2 | | V<br>V | C82C84A, I82C84A<br>M82C84A |
| $V_{IL}$ | Logical Zero Input Voltage | | 0.8 | V | |
| VIHR | Reset Input High Voltage | VCC -0.8 | | V | |
| VILR | Reset Input Low Voltage | | 0.5 | V | |
| VT+ - VT- | Reset Input Hysteresis | 0.2 VCC | | | |
| VOH | Logical One Output Current | VCC -0.4 | | V | IOH = -4.0mA for CLK Output<br>IOH = -2.5mA for All Others |
| VOL | Logical Zero Output Voltage | | 0.4 | V | IOL = +4.0mA for CLK Output<br>IOL = +2.5mA for All Others |
| II | Input Leakage Current | -1.0 | 1.0 | μA | VIN = VCC or GND except $\overline{ASYNC}$, X1: (Note 1) |
| ICCOP | Operating Power Supply Current | | 40 | mA | Crystal Frequency = 25MHz<br>Outputs Open |

NOTES 1 $\overline{ASYNC}$ pin includes an internal 17.5kΩ nominal pull-up resistor. For $\overline{ASYNC}$ input at GND, $\overline{ASYNC}$ input leakage current = 320μA nominal, 500μA maximum. X1 - crystal feedback input.

## Capacitance $T_A$ = 25°C

| SYMBOL | PARAMETER | TYPICAL | UNITS | TEST CONDITIONS |
|---|---|---|---|---|
| CIN | Input Capacitance | 5 | pF | FREQ = 1MHz, all measurements are referenced to device GND |

## A.C. Electrical Specifications

$T_A$ = 0°C to +70°C, $V_{CC}$ = 5V ±10% – C82C84A
$T_A$ = -40°C to +85°C, $V_{CC}$ = 5V ±10% –I82C84A
$T_A$ = -55°C to +125°C, VCC = 5V ±10% –M82C84A

TIMING REQUIREMENTS

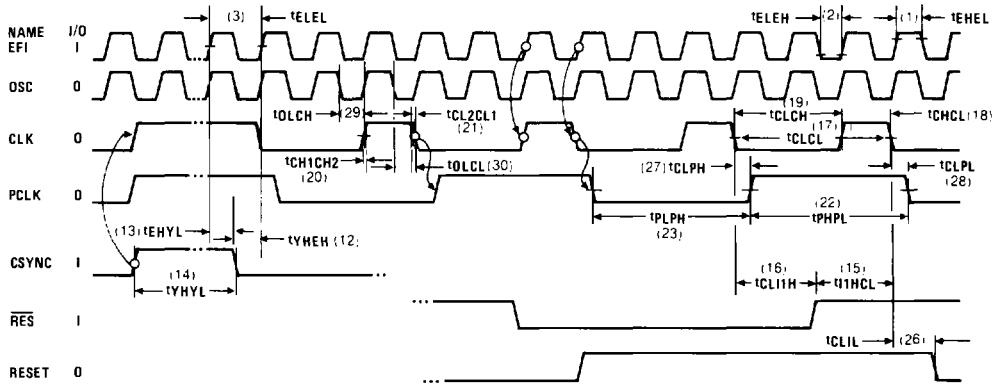
| | Symbol | Parameter | Min. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| (1) | $t_{EHEL}$ | External Frequency HIGH Time | 13 | | ns | 90% - 90% $V_{IN}$ |
| (2) | $t_{ELEH}$ | External Frequency LOW Time | 13 | | ns | 10%-10% $V_{IN}$ |
| (3) | $t_{ELEL}$ | EFI Period | 36 | | ns | |
| | | XTAL Frequency | 2.4 | 25 | MHz | |
| (4) | $t_{R1VCL}$ | RDY1, RDY2 Active Setup to CLK | 35 | | ns | ASYNC = HIGH |
| (5) | $t_{R1VCH}$ | RDY1, RDY2 Active Setup to CLK | 35 | | ns | ASYNC = LOW |
| (6) | $t_{R1VCL}$ | RDY1, RDY2 Inactive Setup to CLK | 35 | | ns | |
| (7) | $t_{CLR1X}$ | RDY1, RDY2 Hold to CLK | 0 | | ns | |
| (8) | $t_{AYVCL}$ | ASYNC Setup to CLK | 50 | | ns | |
| (9) | $t_{CLAYX}$ | ASYNC Hold to CLK | 0 | | ns | |
| (10) | $t_{A1VR1V}$ | AEN1, AEN2 Setup to RDY1, RDY2 | 15 | | ns | |
| (11) | $t_{CLA1X}$ | AEN1, AEN2 Hold to CLK | 0 | | ns | |
| (12) | $t_{YHEH}$ | CSYNC Setup to EFI | 20 | | ns | |
| (13) | $t_{EHYL}$ | CSYNC Hold to EFI | 20 | | ns | |
| (14) | $t_{YHYL}$ | CSYNC Width | $2 \cdot t_{ELEL}$ | | ns | |
| (15) | $t_{I1HCL}$ | RES Setup to CLK | 65 | | ns | (Note 2) |
| (16) | $t_{CLI1H}$ | RES Hold to CLK | 20 | | ns | (Note 2) |

TIMING RESPONSES

| | Symbol | Parameter | Min. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| (17) | $t_{CLCL}$ | CLK Cycle Period | 125 | | ns | |
| (18) | $t_{CHCL}$ | CLK HIGH Time | $(1/3\ t_{CLCL})$ +2.0 | | ns | Fig. 5 & Fig. 6 |
| (19) | $t_{CLCH}$ | CLK LOW Time | $(2/3\ t_{CLCL})$ -15.0 | | ns | Fig. 5 & Fig. 6 |
| (20) (21) | $t_{CH1CH2}$ $t_{CL2CL1}$ | CLK Rise or Fall Time | | 10 | ns | 1.0V to 3.5V |
| (22) | $t_{PHPL}$ | PCLK HIGH Time | $t_{CLCL}$-20 | | ns | |
| (23) | $t_{PLPH}$ | PCLK LOW Time | $t_{CLCL}$-20 | | ns | |
| (24) | $t_{RYLCL}$ | Ready Inactive to CLK (See note 4) | -8 | | ns | Fig. 7 & Fig. 8 |
| (25) | $t_{RYHCH}$ | Ready Active to CLK (See note 3) | $(2/3\ t_{CLCL})$ -15.0 | | ns | Fig. 7 & Fig. 8 |
| (26) | $t_{CLIL}$ | CLK to Reset Delay | | 40 | ns | |
| (27) | $t_{CLPH}$ | CLK to PCLK HIGH Delay | | 22 | ns | |
| (28) | $t_{CLPL}$ | CLK to PCLK LOW Delay | | 22 | ns | |
| (29) | $t_{OLCH}$ | OSC to CLK HIGH Delay | -5 | 22 | ns | |
| (30) | $t_{OLCL}$ | OSC to CLK LOW Delay | 2 | 35 | ns | |

NOTES
1. Output signals switch between VOH and VOL unless otherwise specified.
2. Setup and hold necessary only to guarantee recognition at next clock.
3. Applies only to T3 TW states.
4. Applies only to T2 states.
5. All timing delays are measured at 1.5 volts unless otherwise noted.
6. Input rise and fall times are driven at 1ns/V

+Figure 11 illustrates test load measurement condition.




NOTE: ALL TIMING MEASUREMENTS ARE MADE AT 1.5 VOLTS, UNLESS OTHERWISE NOTED.

FIGURE 2. WAVEFORMS FOR CLOCKS AND RESET SIGNALS

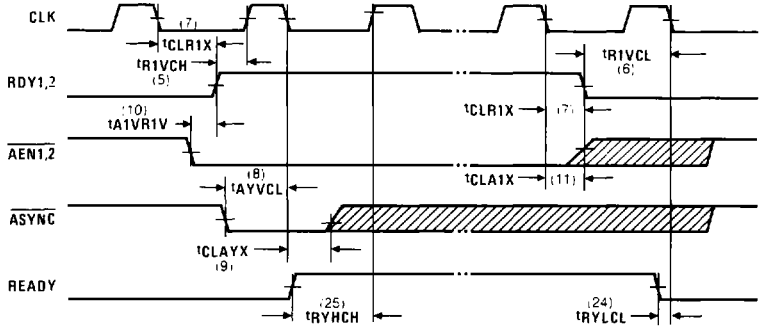



FIGURE 3. WAVEFORMS FOR READY SIGNALS (FOR ASYNCHRONOUS DEVICES)

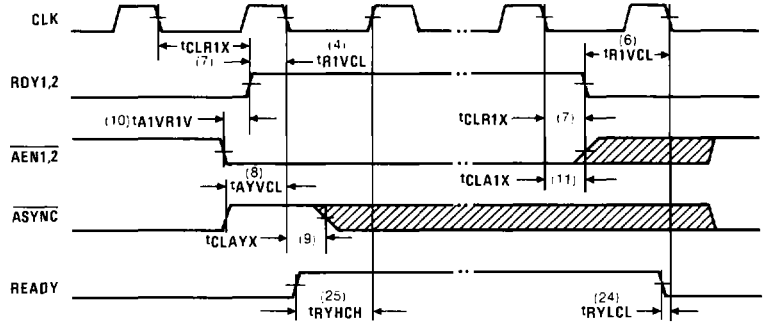



FIGURE 4. WAVEFORMS FOR READY SIGNALS (FOR SYNCHRONOUS DEVICES)

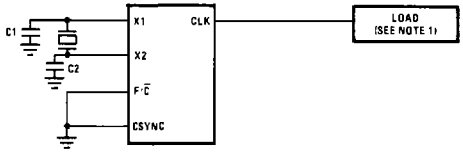



FIGURE 5. CLOCK HIGH AND LOW TIME (USING X1, X2)

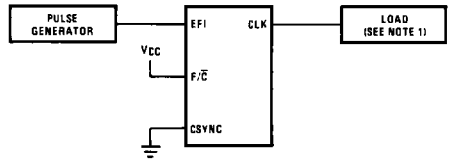



FIGURE 6. CLOCK HIGH AND LOW TIME (USING EFI)

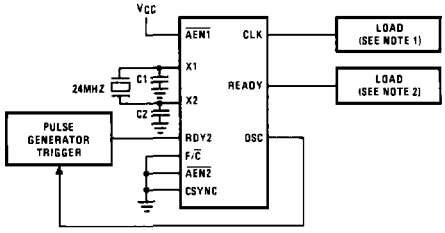



FIGURE 7. READY TO CLOCK (USING X1, X2)

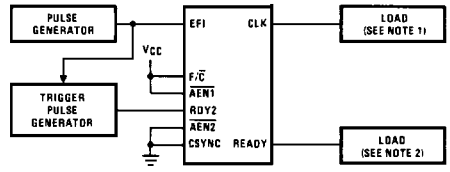



FIGURE 8. READY TO CLOCK (USING EFI)

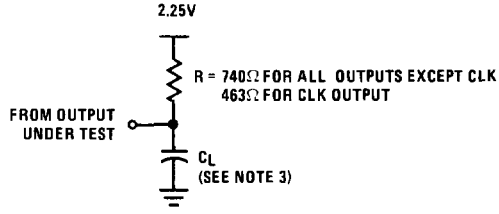
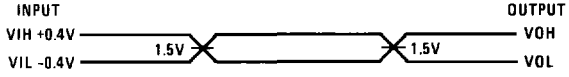



FIGURE 9. TEST LOAD MEASUREMENT CONDITIONS

NOTES:
1. $C_L$ = 100pF
2. $C_L$ = 30pF
3. $C_L$ INCLUDES PROBE AND JIG CAPACITANCE

## A.C. Testing Input, Output Waveforms




* A.C. Testing: All parameters tested as per test circuits. Input rise and fall times are driven at 1ns/V.

| PARAMETER | TYPICAL CRYSTAL SPEC |
|---|---|
| Frequency | 2.4 - 25MHz, Fundamental, "AT" cut |
| Type of Operation | Parallel |
| Unwanted Modes | -6db (Minimum) |
| Load Capacitance | 18 - 32pf |

TABLE 2. CRYSTAL SPECIFICATIONS

See Harris Publication TB-47 for recommended crystal specifications.