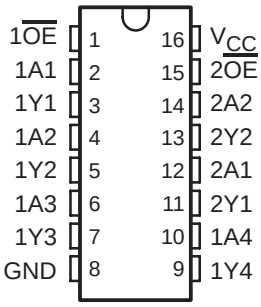
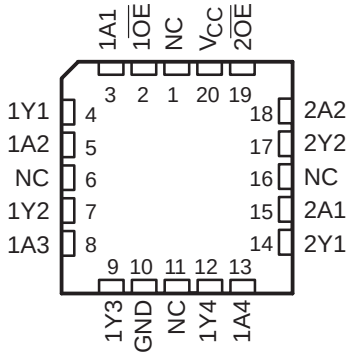
- **2-V to 5.5-V $V_{CC}$ Operation**
- **Max $t_{pd}$ of 7 ns at 5 V**
- **Typical $V_{OLP}$ (Output Ground Bounce) <0.8 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C**
- **Typical $V_{OHV}$ (Output $V_{OH}$ Undershoot) >2.3 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C**
- **Support Mixed-Mode Voltage Operation on All Ports**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

**SN54LV367A . . . J OR W PACKAGE**
**SN74LV367A . . . D, DB, DGV, NS, OR PW PACKAGE**
**(TOP VIEW)**




**SN54LV367A . . . FK PACKAGE**
**(TOP VIEW)**




NC − No internal connection

## description/ordering information

The ’LV367A devices are hex buffers and line drivers designed for 2-V to 5.5-V $V_{CC}$ operation. These devices are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The ’LV367A devices are organized as dual 4-line and 2-line buffers/drivers with active-low output-enable ($1\overline{OE}$ and $2\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes noninverted data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| −40°C to 85°C | SOIC − D | Tube of 40 | SN74LV367AD | LV367A |
| | | Reel of 2500 | SN74LV367ADR | |
| | SOP − NS | Reel of 2000 | SN74LV367ANSR | 74LV367A |
| | SSOP − DB | Reel of 2000 | SN74LV367ADBR | LV36A |
| | TSSOP − PW | Reel of 2000 | SN74LV367APWR | LV367A |
| | | Reel of 250 | SN74LV367APWT | |
| | TVSOP − DGV | Reel of 2000 | SN74LV367ADGVR | LV367A |
| −55°C to 125°C | CDIP − J | Tube of 25 | SNJ54LV367AJ | SNJ54LV367AJ |
| | CFP − W | Tube of 150 | SNJ54LV367AW | SNJ54LV367AW |
| | LCCC − FK | Tube of 55 | SNJ54LV367AFK | SNJ54LV367AFK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE**
**(each buffer/driver)**

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{OE}$ | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |

## logic diagram (positive logic)


Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . −0.5 V to 7 V
Voltage range applied to any output in the high-impedance or
power-off state, $V_O$ (see Note 1) . . . . . −0.5 V to 7 V
Output voltage range applied in the high or low state, $V_O$ (see Notes 1 and 2) . . . . . −0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . −20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0) . . . . . −50 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±35 mA
Continuous current through $V_{CC}$ or GND . . . . . ±70 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): D package . . . . . 73°C/W
DB package . . . . . 82°C/W
DGV package . . . . . 120°C/W
NS package . . . . . 64°C/W
PW package . . . . . 108°C/W
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 4)

| | | | SN54LV367A | | SN74LV367A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | $V_{CC} \times 0.7$ | | $V_{CC} \times 0.7$ | | |
| | | $V_{CC}$ = 3 V to 3.6 V | $V_{CC} \times 0.7$ | | $V_{CC} \times 0.7$ | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | $V_{CC} \times 0.7$ | | $V_{CC} \times 0.7$ | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | $V_{CC} \times 0.3$ | | $V_{CC} \times 0.3$ | |
| | | $V_{CC}$ = 3 V to 3.6 V | | $V_{CC} \times 0.3$ | | $V_{CC} \times 0.3$ | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | $V_{CC} \times 0.3$ | | $V_{CC} \times 0.3$ | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | High or low state | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| | | 3-state | 0 | 5.5 | 0 | 5.5 | |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | −50 | | −50 | µA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | −2 | | −2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | −8 | | −8 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | −16 | | −16 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | µA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 2 | | 2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | 8 | | 8 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 16 | | 16 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 2.3 V to 2.7 V | | 200 | | 200 | ns/V |
| | | $V_{CC}$ = 3 V to 3.6 V | | 100 | | 100 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | −55 | 125 | −40 | 85 | °C |



NOTE 4: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | SN54LV367A | | | SN74LV367A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{OH}$ | $I_{OH}$ = −50 μA | 2 V to 5.5 V | $V_{CC}$−0.1 | | | $V_{CC}$−0.1 | | | V |
| | $I_{OH}$ = −2 mA | 2.3 V | 2 | | | 2 | | | |
| | $I_{OH}$ = −8 mA | 3 V | 2.48 | | | 2.48 | | | |
| | $I_{OH}$ = −16 mA | 4.5 V | 3.8 | | | 3.8 | | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V to 5.5 V | | | 0.1 | | | 0.1 | V |
| | $I_{OL}$ = 2 mA | 2.3 V | | | 0.4 | | | 0.4 | |
| | $I_{OL}$ = 8 mA | 3 V | | | 0.44 | | | 0.44 | |
| | $I_{OL}$ = 16 mA | 4.5 V | | | 0.55 | | | 0.55 | |
| $I_I$ | $V_I$ = 5.5 V or GND | 0 to 5.5 V | | | ±1 | | | ±1 | μA |
| $I_{OZ}$ | $V_O$ = $V_{CC}$ or GND | 5.5 V | | | ±5 | | | ±5 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 20 | | | 20 | μA |
| $I_{off}$ | $V_I$ or $V_O$ = 0 to 5.5 V | 0 | | | 5 | | | 5 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 3.3 V | | 3 | | | 3 | | pF |
| $C_o$ | $V_I$ = $V_{CC}$ or GND | 3.3 V | | 5.2 | | | 5.2 | | pF |



## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54LV367A | | SN74LV367A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | Y | $C_L$ = 15 pF | | 6.4* | 12.7* | 1* | 16* | 1 | 16 | ns |
| $t_{en}$ | $\overline{OE}$ | Y | | | 6.9* | 14.9* | 1* | 20* | 1 | 20 | |
| $t_{dis}$ | $\overline{OE}$ | Y | | | 6.4* | 14.9* | 1* | 20* | 1 | 20 | |
| $t_{pd}$ | A | Y | $C_L$ = 50 pF | | 8.6 | 17.5 | 1 | 21 | 1 | 21 | ns |
| $t_{en}$ | $\overline{OE}$ | Y | | | 9.4 | 19.7 | 1 | 25 | 1 | 25 | |
| $t_{dis}$ | $\overline{OE}$ | Y | | | 10.1 | 19.7 | 1 | 25 | 1 | 25 | |
| $t_{sk(o)}$ | | | | | | 2 | | | | 2 | |



* On products compliant to MIL-PRF-38535, this parameter is not production tested.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54LV367A | | SN74LV367A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | Y | $C_L$ = 15 pF | | 4.7* | 8.3* | 1* | 10* | 1 | 10 | ns |
| $t_{en}$ | $\overline{OE}$ | Y | | | 5.1* | 10.5* | 1* | 12.5* | 1 | 12.5 | |
| $t_{dis}$ | $\overline{OE}$ | Y | | | 4.9* | 10.5* | 1* | 12.5* | 1 | 12.5 | |
| $t_{pd}$ | A | Y | $C_L$ = 50 pF | | 6.2 | 11.8 | 1 | 13.5 | 1 | 13.5 | ns |
| $t_{en}$ | $\overline{OE}$ | Y | | | 6.8 | 14 | 1 | 16 | 1 | 16 | |
| $t_{dis}$ | $\overline{OE}$ | Y | | | 7.3 | 13.6 | 1 | 15.5 | 1 | 15.5 | |
| $t_{sk(o)}$ | | | | | | 1.5 | | | | 1.5 | |



* On products compliant to MIL-PRF-38535, this parameter is not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54LV367A | | SN74LV367A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | Y | $C_L$ = 15 pF | | 3.6* | 5.9* | 1* | 7* | 1 | 7 | ns |
| $t_{en}$ | $\overline{OE}$ | Y | | | 3.8* | 7.2* | 1* | 8.5* | 1 | 8.5 | |
| $t_{dis}$ | $\overline{OE}$ | Y | | | 2.6* | 7.2* | 1* | 8.5* | 0 | 8.5 | |
| $t_{pd}$ | A | Y | $C_L$ = 50 pF | | 4.5 | 7.9 | 1 | 9 | 1 | 9 | ns |
| $t_{en}$ | $\overline{OE}$ | Y | | | 4.9 | 9.2 | 1 | 10.5 | 1 | 10.5 | |
| $t_{dis}$ | $\overline{OE}$ | Y | | | 4.5 | 9.2 | 1 | 10.5 | 0 | 10.5 | |
| $t_{sk(o)}$ | | | | | | 1 | | | | 1 | |



* On products compliant to MIL-PRF-38535, this parameter is not production tested.

### noise characteristics, $V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

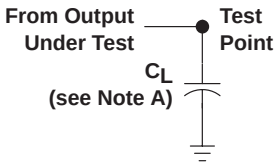
| PARAMETER | | SN74LV367A | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.5 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | −0.2 | −0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 3 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2.31 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.99 | V |

NOTE 5: Characteristics are for surface-mount packages only.

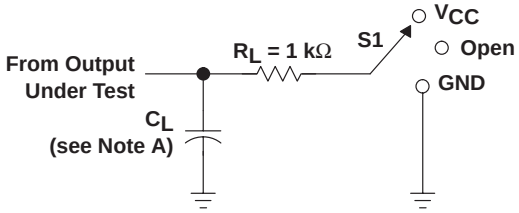
### operating characteristics, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | $C_L$ = 50 pF, f = 10 MHz | 3.3 V | 14.9 | pF |
| | | | 5 V | 17.4 | |

## PARAMETER MEASUREMENT INFORMATION

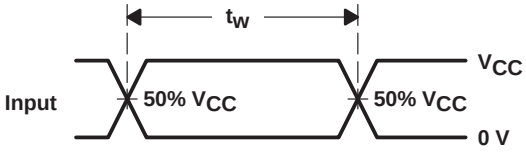



LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

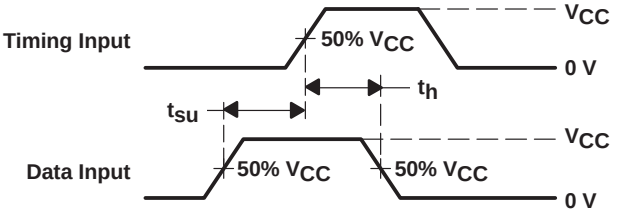



LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

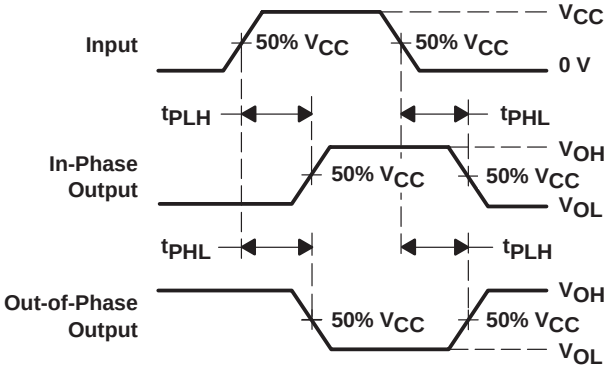
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |
| Open Drain | $V_{CC}$ |



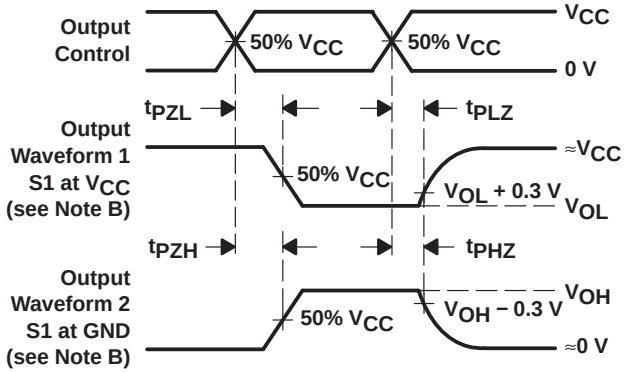

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PHL}$ and $t_{PLH}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV367AD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV367A | Samples |
| SN74LV367ADBR | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV367A | Samples |
| SN74LV367ADBRE4 | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV367A | Samples |
| SN74LV367ADBRG4 | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV367A | Samples |
| SN74LV367ADE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV367A | Samples |
| SN74LV367ADG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV367A | Samples |
| SN74LV367ADGVR | ACTIVE | TVSOP | DGV | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV367A | Samples |
| SN74LV367ADGVRE4 | ACTIVE | TVSOP | DGV | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV367A | Samples |
| SN74LV367ADGVRG4 | ACTIVE | TVSOP | DGV | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV367A | Samples |
| SN74LV367ADR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV367A | Samples |
| SN74LV367ADRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV367A | Samples |
| SN74LV367ADRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV367A | Samples |
| SN74LV367ANSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 74LV367A | Samples |
| SN74LV367ANSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 74LV367A | Samples |
| SN74LV367ANSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 74LV367A | Samples |
| SN74LV367APWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV367A | Samples |
| SN74LV367APWRE4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV367A | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV367APWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV367A | Samples |
| SN74LV367APWT | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV367A | Samples |
| SN74LV367APWTE4 | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV367A | Samples |
| SN74LV367APWTG4 | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV367A | Samples |
| SN74LV367AQPWRQ1 | OBSOLETE | TSSOP | PW | 16 | | TBD | Call TI | Call TI | | | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

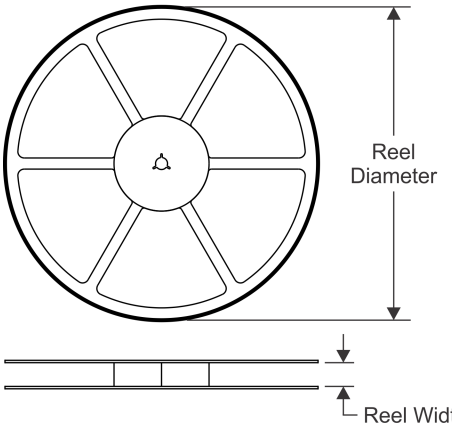
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

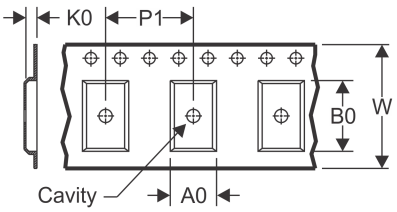
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

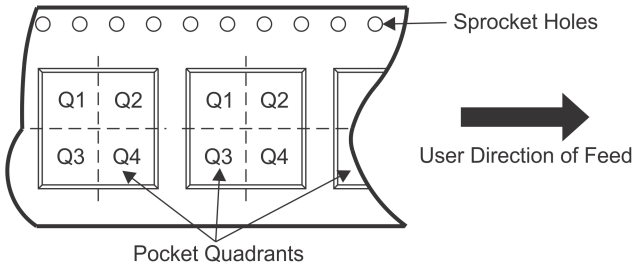



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

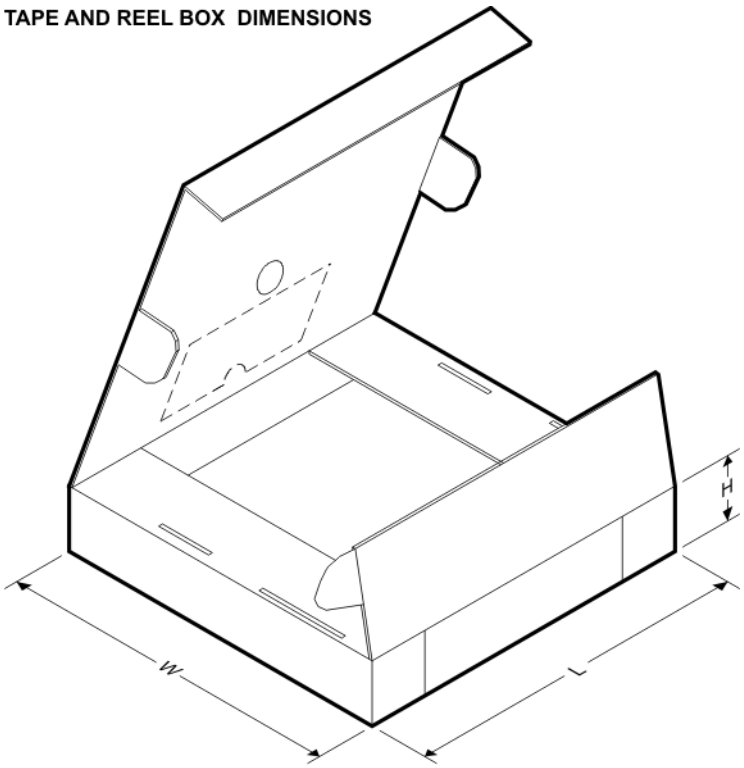
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV367ADBR | SSOP | DB | 16 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LV367ADGVR | TVSOP | DGV | 16 | 2000 | 330.0 | 12.4 | 6.8 | 4.0 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV367ADR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV367ANSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LV367APWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV367APWT | TSSOP | PW | 16 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

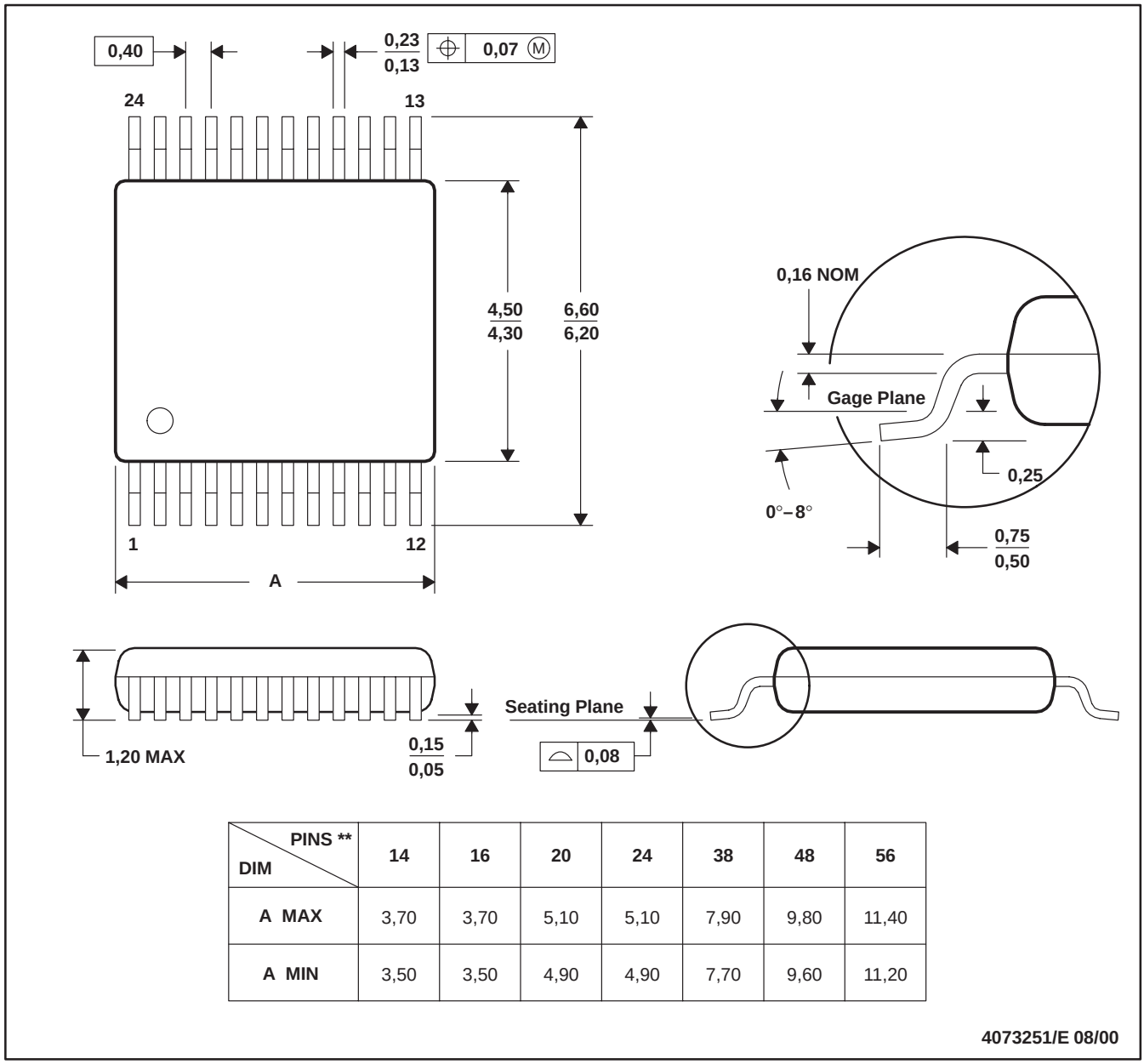



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LV367ADBR | SSOP | DB | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LV367ADGVR | TVSOP | DGV | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74LV367ADR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74LV367ANSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LV367APWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74LV367APWT | TSSOP | PW | 16 | 250 | 367.0 | 367.0 | 35.0 |

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**

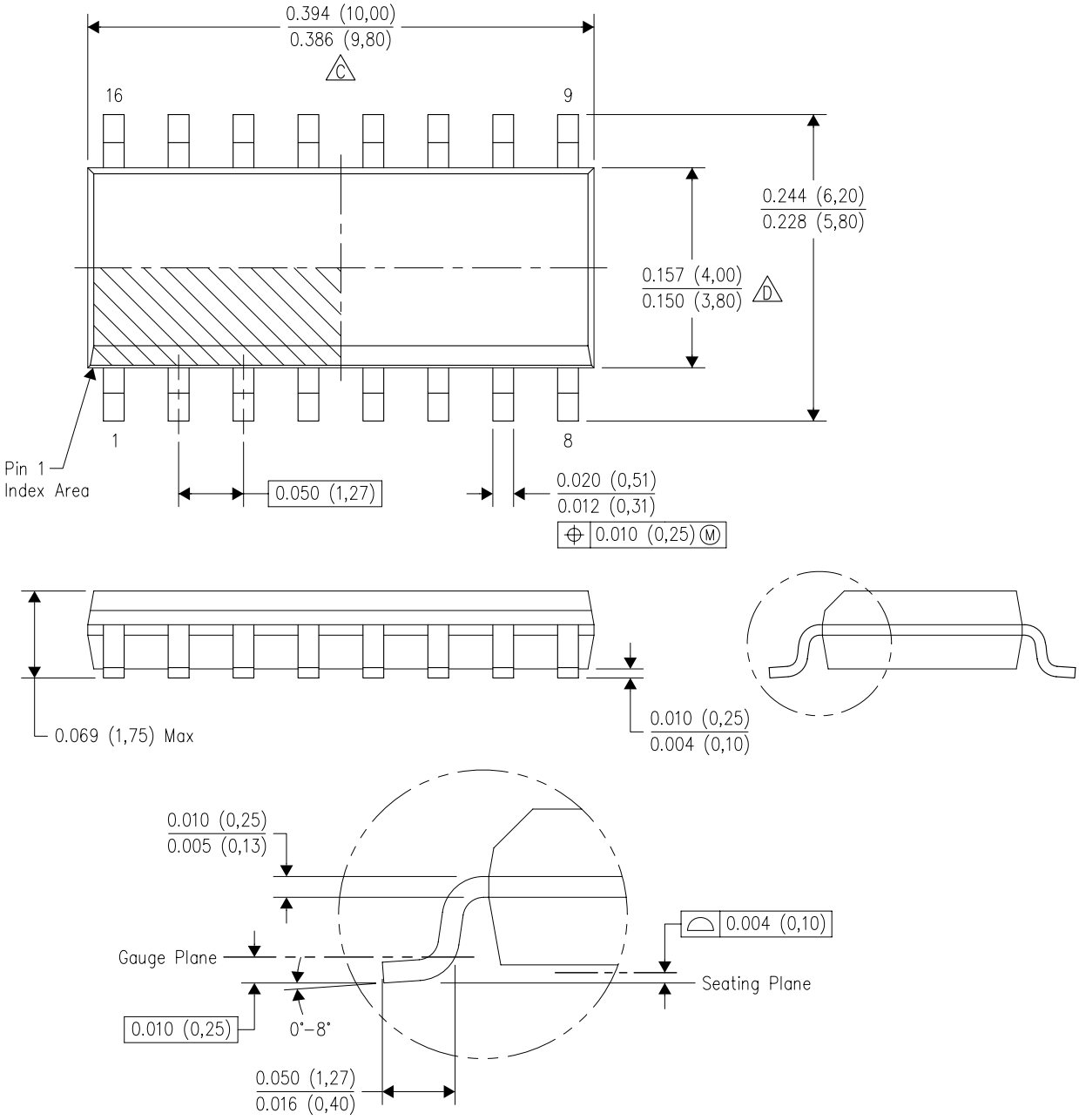



| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

**4073251/E 08/00**

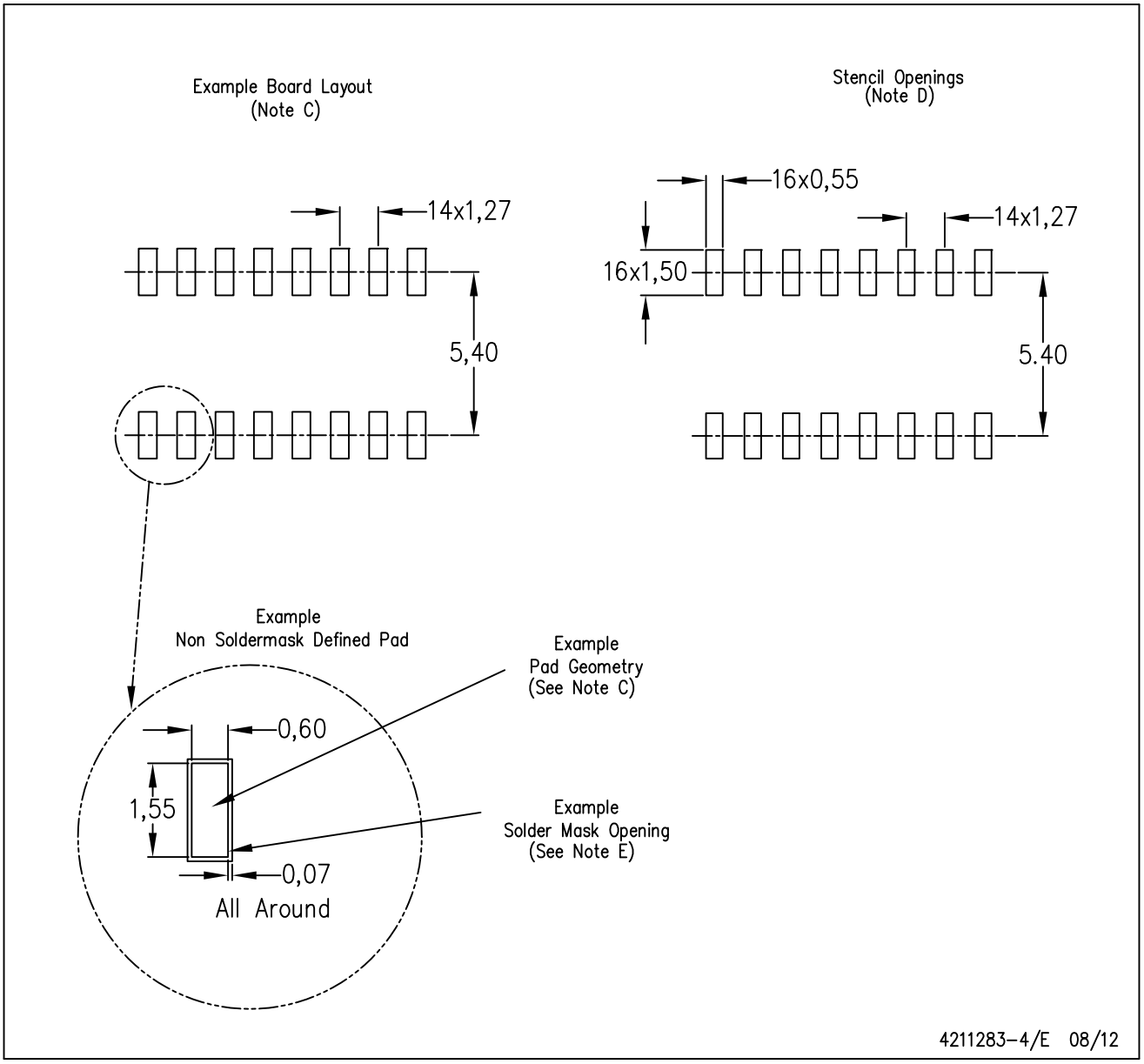
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



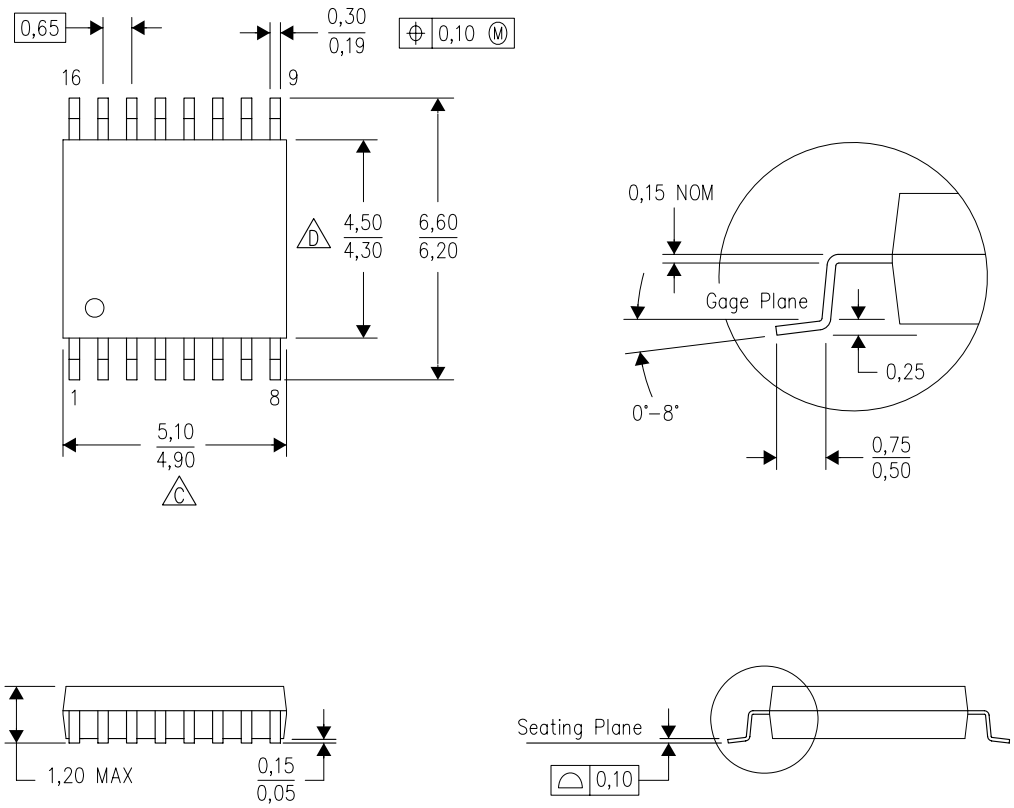

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

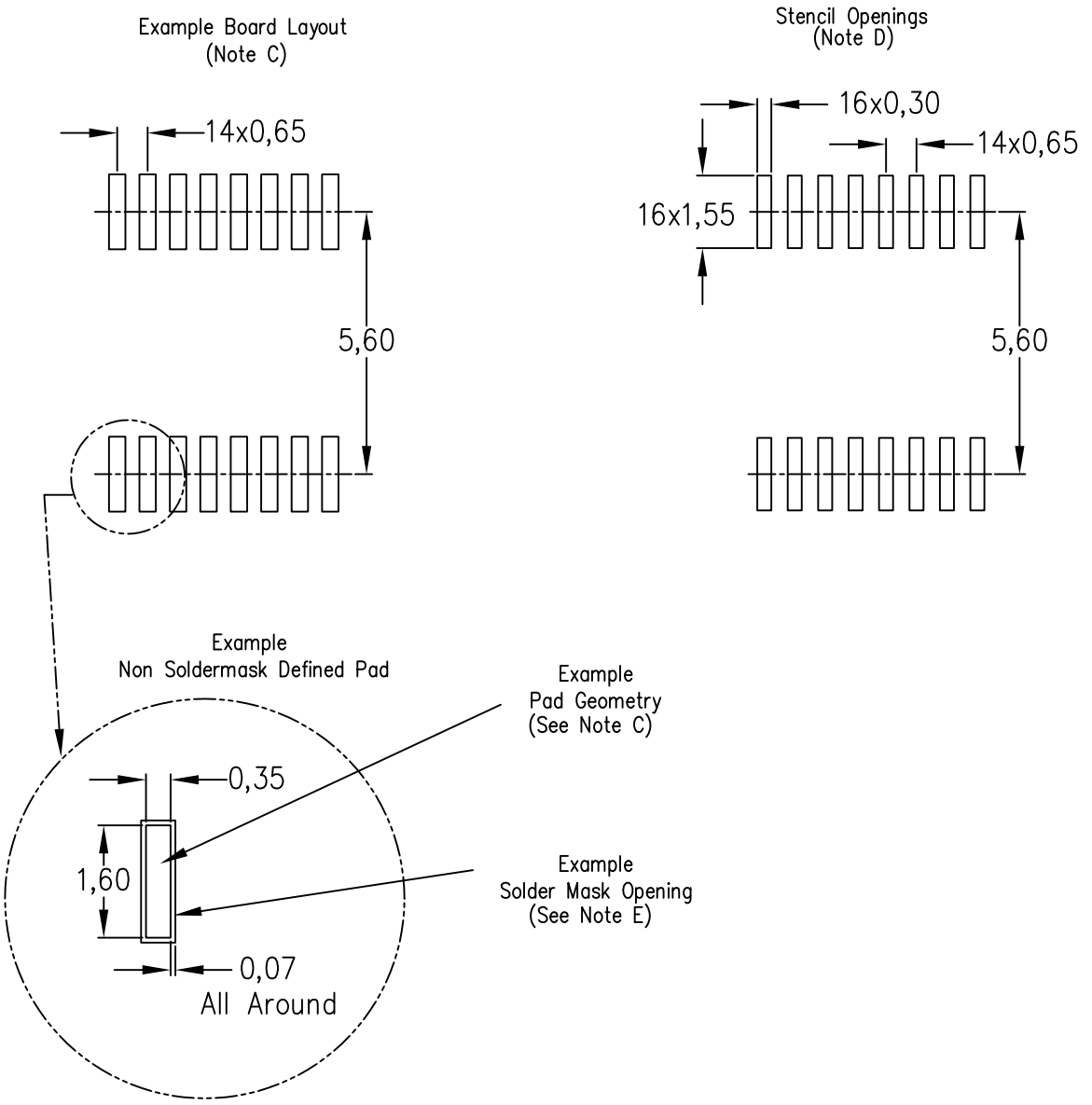
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE




4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE

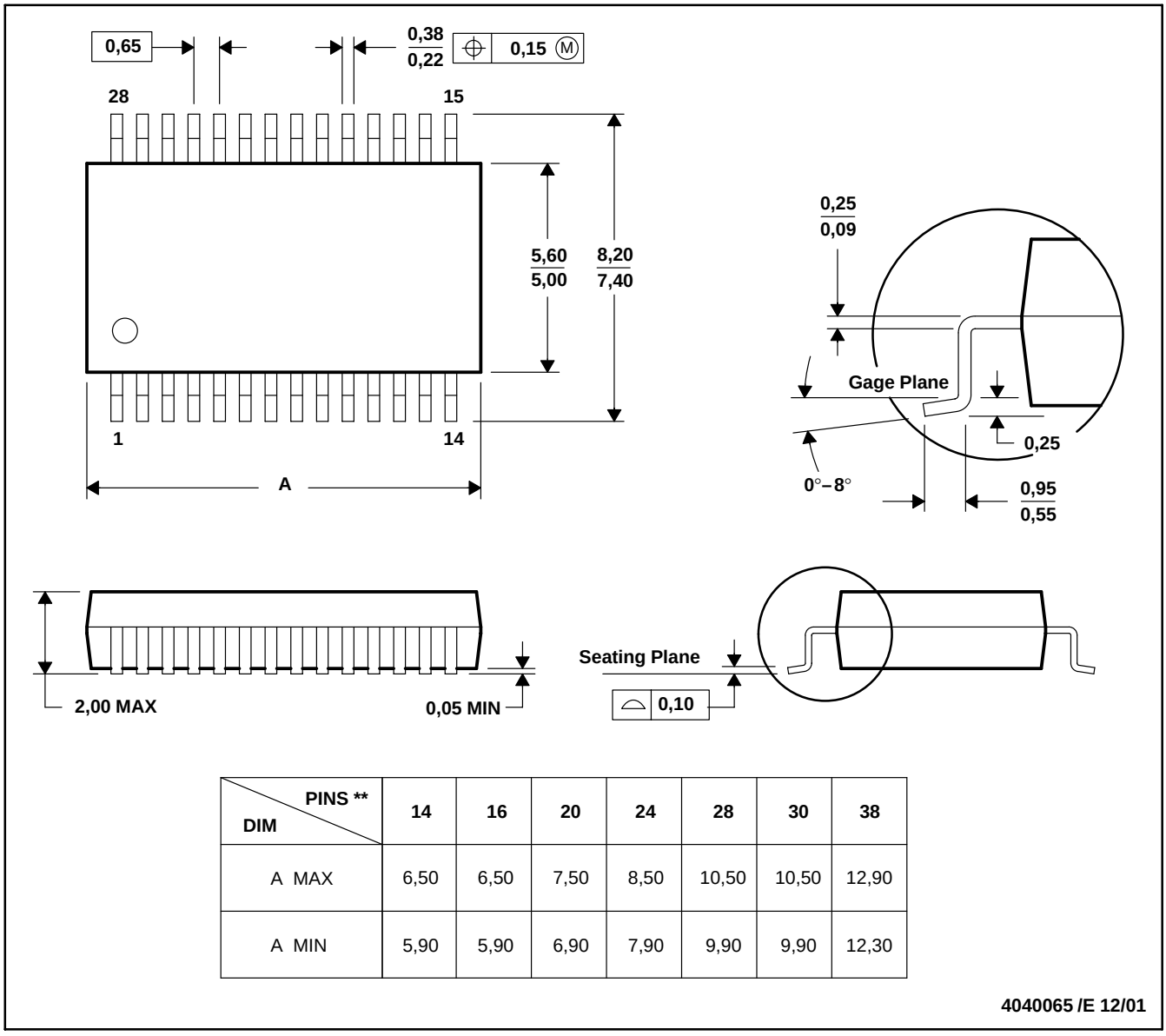



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

**DB (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**28 PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|
| A MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

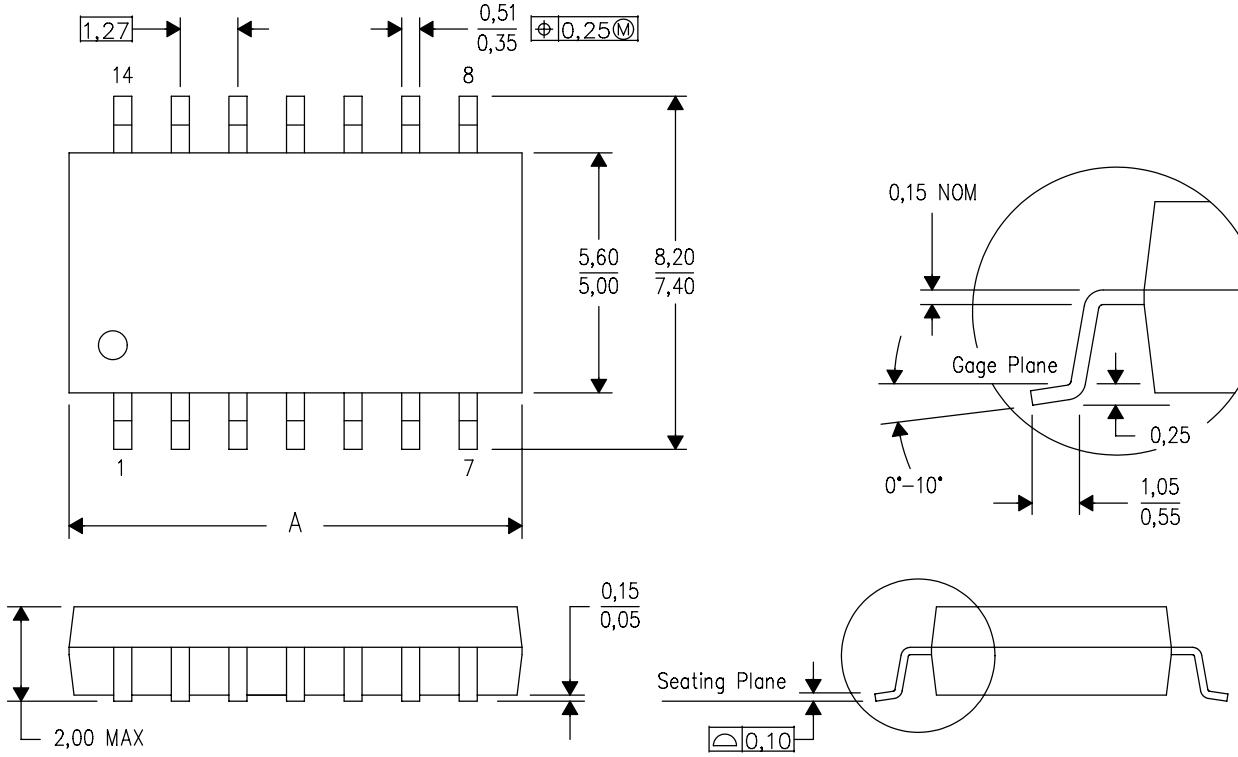
**4040065 /E 12/01**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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