

SRAM

32K x 8 SRAM

5 VOLT SRAM

FEATURES

- High speed: 10*, 12*, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with \overline{CE} and \overline{OE} options
- All inputs and outputs are TTL compatible

OPTIONS

- Timing
 - 10ns access
 - 12ns access
 - 15ns access
 - 20ns access
 - 25ns access
 - 35ns access

MARKING

-10*
-12*
-15
-20
-25
-35

Packages

Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
Plastic ZIP	Z

NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.

- 2V data retention L
- 2V data retention, low power LP
- Temperature
 - Industrial (-40°C to +85°C) IT
 - Automotive (-40°C to +125°C) AT
 - Extended (-55°C to +125°C) XT
- Part Number Example: MT5C2568Z-20 LP IT

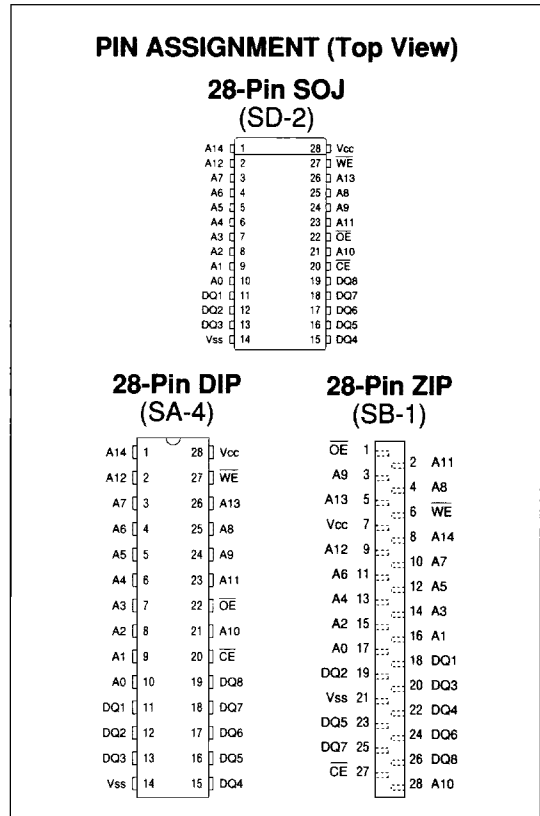
*Preliminary

GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable (\overline{CE}) and output enable (\overline{OE}) with this organization. These enhancements can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable (\overline{WE}) and \overline{CE} inputs are both LOW. Reading is

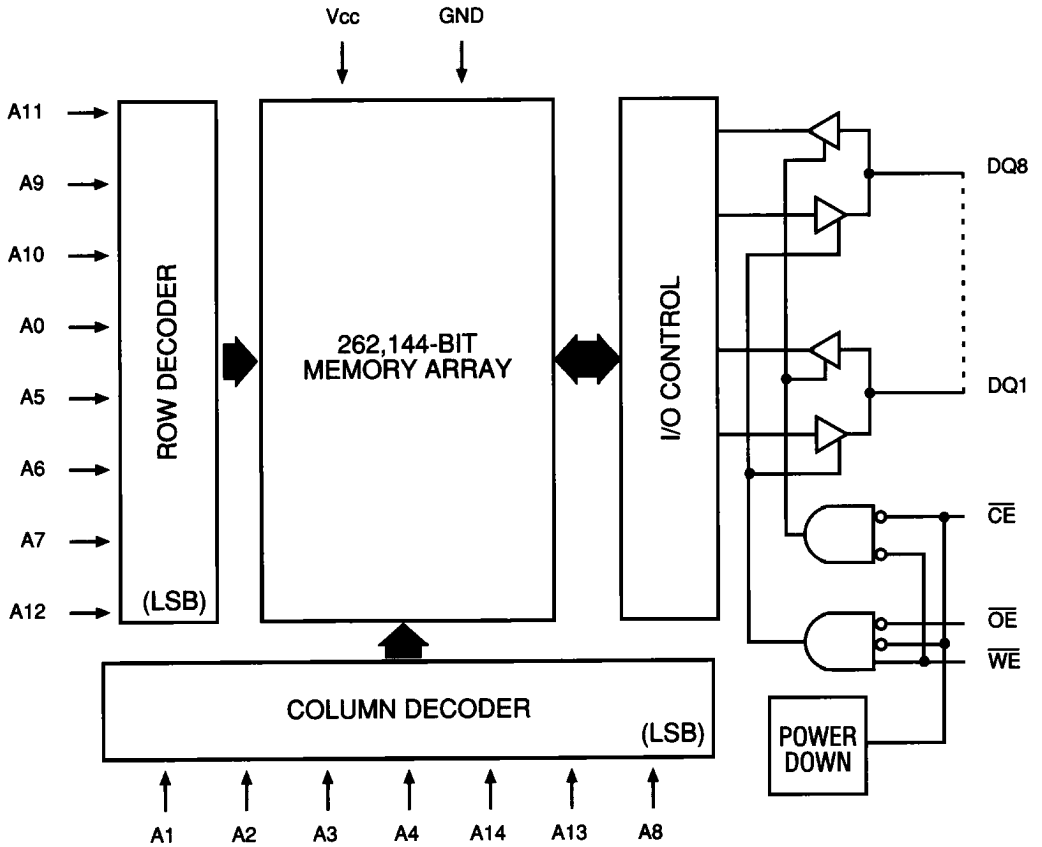


accomplished when \overline{WE} remains HIGH and \overline{CE} and \overline{OE} go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "LP" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the \overline{WE} , \overline{OE} and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	\overline{OE}	\overline{CE}	\overline{WE}	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V _{CC} Supply Relative to V _{SS}	-1V to +7V
Storage Temperature (Plastic)	-55°C to +150°C
Power Dissipation	1W
Short Circuit Output Current	50mA
Voltage on any pin relative to V _{SS}	-1V to V _{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V _{IH}	2.2	V _{CC} +1	V	1
Input Low (Logic 0) Voltage		V _{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V _{IN} ≤ V _{CC}	I _{LI}	-5	5	μA	
Output Leakage Current	Output(s) Disabled 0V ≤ V _{OUT} ≤ V _{CC}	I _{LO}	-5	5	μA	
Output High Voltage	I _{OH} = -4.0mA	V _{OH}	2.4		V	1
Output Low Voltage	I _{OL} = 8.0mA	V _{OL}		0.4	V	1
Supply Voltage		V _{CC}	4.5	5.5	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX						UNITS	NOTES
				-10 ^{+†}	-12 ^{+†}	-15 [†]	-20	-25	-35		
Power Supply Current: Operating	CE ≤ V _{IL} ; V _{CC} = MAX f = MAX = 1/1RC Outputs Open	I _{CC}	85	180	160	140	120	110	90	mA	3, 14
	"LP" VERSION	I _{CC}	65	-	-	-	110	100	80	mA	3, 14
Power Supply Current: Standby	CE ≥ V _{IH} ; V _{CC} = MAX f = MAX = 1/1RC Outputs Open	I _{SB1}	11	45	40	30	30	25	25	mA	14
	"LP" VERSION	I _{SB1}	3	-	-	-	7	7	7	mA	14
	CE ≥ V _{CC} - 0.2V; V _{CC} = MAX V _{IN} ≤ V _{SS} + 0.2V or V _{IN} ≥ V _{CC} - 0.2V; f = 0	I _{SB2}	0.6	5	5	5	5	5	7	mA	14

*Preliminary

† LP version not available in this speed grade.

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T _A = 25°C; f = 1 MHz V _{CC} = 5V	C _i	6	pF	4
Output Capacitance		C _o	5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$; $V_{CC} = 5\text{V} \pm 10\%$)

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DESCRIPTION	SYM	-10*		-12*		-15		-20		-25		-35		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle															
READ cycle time	t_{RC}	10		12		15		20		25		35		ns	
Address access time	t_{AA}		10		12		15		20		25		35	ns	
Chip Enable access time	t_{ACE}		10		12		15		20		25		35	ns	
Output hold from address change	t_{OH}	2		3		3		3		5		5		ns	
Chip Enable to output in Low-Z	t_{LZCE}	3		4		4		4		6		6		ns	7
Chip disable to output in High-Z	t_{HZCE}		6		8		8		9		9		15	ns	6, 7
Chip Enable to power-up time	t_{PU}	0		0		0		0		0		0		ns	
Chip disable to power-down time	t_{PD}		10		12		15		20		25		35	ns	
Output Enable access time	t_{AOE}		6		8		8		8		8		12	ns	
Output Enable to output in Low-Z	t_{LZOE}	0		0		0		0		0		0		ns	
Output disable to output in High-Z	t_{HZOE}		5		6		6		7		7		12	ns	6
WRITE Cycle															
WRITE cycle time	t_{WC}	10		12		15		20		25		30		ns	
Chip Enable to end of write	t_{CW}	9		10		10		15		15		20		ns	
Address valid to end of write	t_{AW}	9		10		10		15		15		20		ns	
Address setup time	t_{AS}	0		0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		0		0		ns	
WRITE pulse width	t_{WP1}	9		10		10		15		15		20		ns	
WRITE pulse width	t_{WP2}	11		12		12		15		15		20		ns	
Data setup time	t_{DS}	6		7		7		10		10		15		ns	
Data hold time	t_{DH}	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	t_{LZWE}	3		4		4		4		5		5		ns	7
Write Enable to output in High-Z	t_{HZWE}		6		7		7		10		10		15	ns	6, 7

*Preliminary

AC TEST CONDITIONS

Input pulse levels	V _{SS} to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

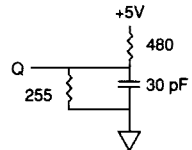


Fig. 1 OUTPUT LOAD EQUIVALENT

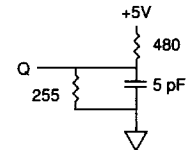


Fig. 2 OUTPUT LOAD EQUIVALENT

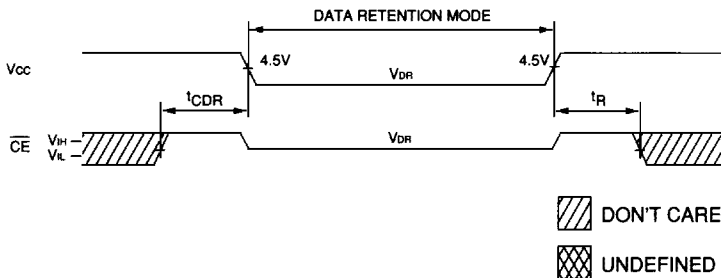
NOTES

1. All voltages referenced to V_{SS} (GND).
2. -3V for pulse width < t_{RC}/2.
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. t_{HZCE}, t_{HZOE} and t_{HZWE} are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, and t_{HZWE} is less than t_{LZWE}.
8. WE is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. t_{RC} = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Refer to the IT/XT/AT section of Micron's SRAM Data Book for applicable non-commercial temperature range specifications.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.

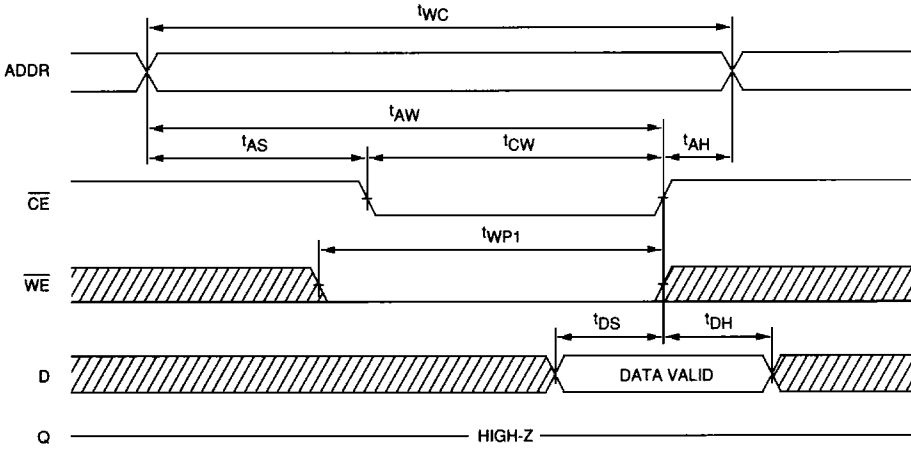
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP Versions Only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V _{CC} for Retention Data		V _{DR}	2			V	
Data Retention Current	$\overline{CE} \geq (V_{CC} - 0.2V)$ $V_{IN} \geq (V_{CC} - 0.2V)$ or $\leq 0.2V$	V _{CC} = 2V	I _{CCDR}		35	300	μA
		V _{CC} = 3V	I _{CCDR}		90	500	μA
Chip Deselect to Data Retention Time		t _{CDR}	0			ns	4
Operation Recovery Time		t _R	t _{RC}			ns	4, 11

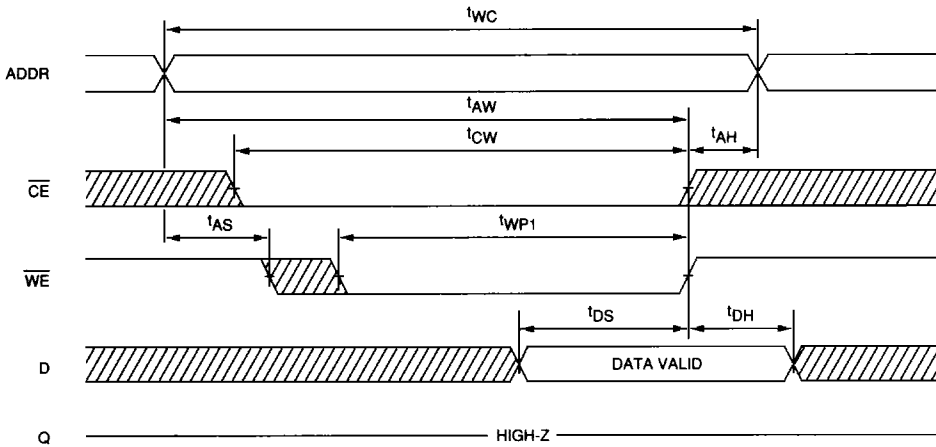
LOW V_{CC} DATA RETENTION WAVEFORM



WRITE CYCLE NO. 1¹²
(Chip Enable Controlled)



WRITE CYCLE NO. 2¹²
(Write Enable Controlled)

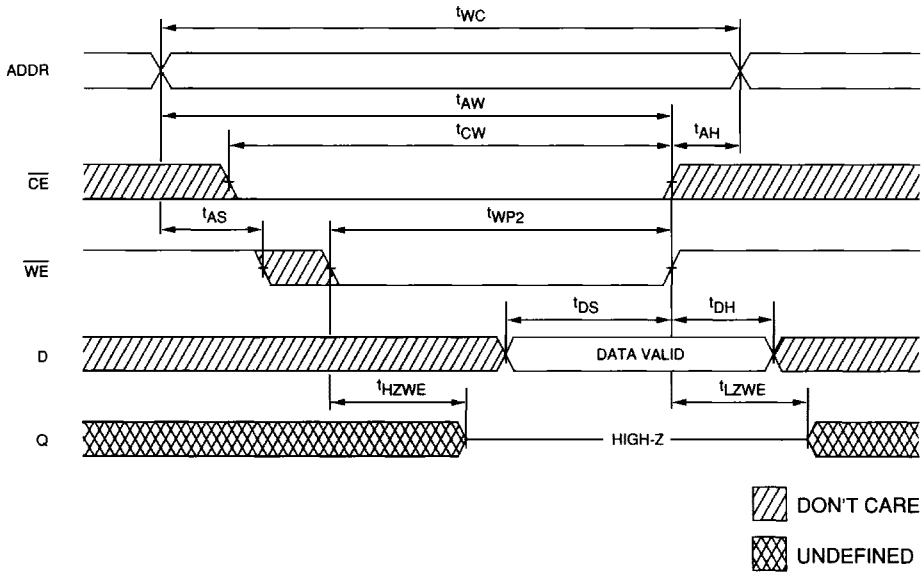


 DON'T CARE
 UNDEFINED

NOTE: Output enable (\overline{OE}) is inactive (HIGH).

WRITE CYCLE NO. 3^{7, 12}
(Write Enable Controlled)

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NOTE: Output enable (\overline{OE}) is active (LOW).