



Integrated Device Technology, Inc.

# 128K x 36, 3.3V SYNCHRONOUS SRAM WITH ZBT™ FEATURE, BURST COUNTER AND PIPELINED OUTPUTS

## ADVANCE INFORMATION IDT71V546

### FEATURES:

- 128K x 36 memory configuration, pipelined outputs
- Supports high performance system speed - 133 MHz (4.2 ns Clock-to-Data Access)
- ZBT™ Feature - No dead cycles between write and read cycles
- Internally synchronized registered outputs eliminate the need to control  $\overline{OE}$
- Single  $R/\overline{W}$  (READ/WRITE) control pin
- Positive clock-edge triggered, address, data, and control signal registers for fully pipelined applications
- 4-word burst capability (interleaved or linear)
- Individual byte write ( $\overline{BW1}$  -  $\overline{BW4}$ ) control (May tie active)
- Three chip enables for simple depth expansion
- Single 3.3V power supply (+/- 5%)
- Packaged in a JEDEC standard 100-pin TQFP package

### DESCRIPTION:

The IDT71V546 is a 3.3V high-speed 4,718,592-bit (4.5 Megabit) synchronous SRAM organized as 128K x 36 bit. It is designed to eliminate dead bus cycles when turning the bus around between reads and writes, or writes and reads. Thus it has been given the name ZBT™, or Zero Bus Turn-around.

Address and control signals are applied to the SRAM during one clock cycle, and two cycles later its associated data cycle occurs, be it read or write.

The IDT71V546 contains data I/O, address and control signal registers. Output enable is the only asynchronous signal and can be used to disable the outputs at any given time.

A Clock Enable ( $\overline{CEN}$ ) pin allows operation of the IDT71V546 to be suspended as long as necessary. All synchronous inputs are ignored when ( $\overline{CEN}$ ) is high and the internal device registers will hold their previous values.

There are three chip enable pins ( $\overline{CE1}$ ,  $CE2$ ,  $\overline{CE2}$ ) that allow the user to deselect the device when desired. If any one of these three are not active when  $ADV/\overline{LD}$  is low, no new memory operation can be initiated and any burst that was in progress is stopped. However, any pending data transfers (reads or writes) will be completed. The data bus will tri-state two cycles after chip is deselected or a write initiated.

The IDT71V546 has an on-chip burst counter. In the burst mode, the IDT71V546 can provide four cycles of data for a single address presented to the SRAM. The order of the burst sequence is defined by the LBO input pin. The LBO pin selects between linear and interleaved burst sequence. The  $ADV/\overline{LD}$  signal is used to load a new external address ( $ADV/\overline{LD} = LOW$ ) or increment the internal burst counter ( $ADV/\overline{LD} = HIGH$ ).

The IDT71V546 SRAM utilizes IDT's high-performance, high-volume 3.3V CMOS process, and is packaged in a JEDEC Standard 14mm x 20mm 100-pin thin plastic quad flatpack (TQFP) for high board density.

### PIN DESCRIPTION SUMMARY

$A_0 - A_{16}$	Address Inputs	Input	Synchronous
$\overline{CE1}$ , $CE2$ , $\overline{CE2}$	Three Chip Enables	Input	Synchronous
$\overline{OE}$	Output Enable	Input	Asynchronous
$R/\overline{W}$	Read / Write Signal	Input	Synchronous
$\overline{CEN}$	Clock Enable	Input	Synchronous
$\overline{BW1}$ , $\overline{BW2}$ , $\overline{BW3}$ , $\overline{BW4}$	Individual Byte Write Selects	Input	Synchronous
CLK	Clock	Input	N/A
$ADV/\overline{LD}$	Advance burst address / Load new address	Input	Synchronous
LBO	Linear / Interleaved Burst Order	Input	Static
$I/O_0-I/O_{31}$ , $I/OP_1-I/OP_4$	Data Input / Output	I/O	Synchronous
VDD	3.3V Power	Pwr	Static
VSS	Ground	Gnd	Static

3821 tbl 01

### (Patents Pending)

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COMMERCIAL TEMPERATURE RANGE

NOVEMBER 1997

**PIN DEFINITIONS<sup>(1)</sup>**

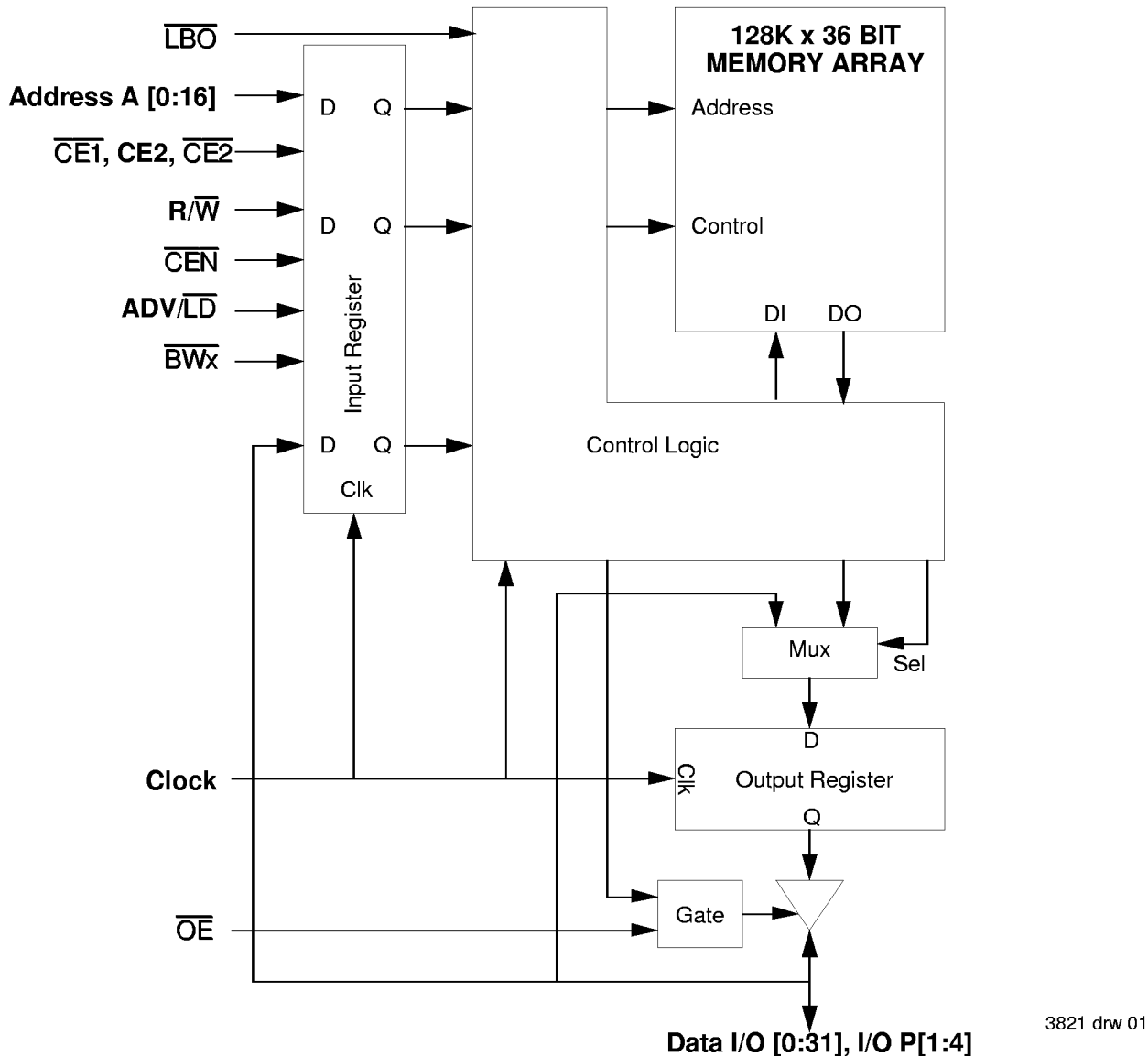
Symbol	Pin Function	I/O	Active	Description
A0-A16	Address Inputs	I	N/A	Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK, ADV/LD low, CEN low, and true chip enables.
ADV/LD	Advance / Load	I	N/A	ADV/LD is a synchronous input that is used to load the internal registers with new address and control when it is sampled low at the rising edge of clock with the chip selected. When ADV/LD is low with the chip deselected, any burst in progress is terminated. When ADV/LD is sampled high then the internal burst counter is advanced for any burst that was in progress. The external addresses are ignored when ADV/LD is sampled high.
R/W	Read / Write	I	N/A	R/W signal is a synchronous input that identifies whether the current load cycle initiated is a Read or Write access to the memory array. The data bus activity for the current cycle takes place two clock cycles later.
CEN	Clock Enable	I	LOW	Synchronous Clock Enable Input. When CEN is sampled high, all other synchronous inputs, including clock are ignored and outputs remain unchanged. The effect of CEN sampled high on the device outputs is as if the low to high clock transition did not occur. For normal operation, CEN must be sampled low at rising edge of clock.
BW1 - BW4	Individual Byte Write Enables	I	LOW	Synchronous byte write enables. Each 9-bit byte has its own active low byte write enable. On load write cycles (When R/W and ADV/LD are sampled low) the appropriate byte write signal (BW1 - BW4) must be valid. The byte write signal must also be valid on each cycle of a burst write. Byte Write signals are ignored when R/W is sampled high. The appropriate byte(s) of data are written into the device two cycles later. BW1 - BW4 can all be tied low if always doing write to the entire 36-bit word.
CE1, CE2	Chip Enables	I	LOW	Synchronous active low chip enable. CE1 and CE2 are used with CE2 to enable the IDT71V546. (CE1 or CE2 sampled high or CE2 sampled low) and ADV/LD low at the rising edge of clock, initiates a deselect cycle. The ZBT™ has a two cycle deselect, i.e., the data bus will tri-state two clock cycles after deselect is initiated.
CE2	Chip Enable	I	HIGH	Synchronous active high chip enable. CE2 is used with CE1 and CE2 to enable the chip. CE2 has inverted polarity but otherwise identical to CE1 and CE2.
CLK	Clock	I	N/A	This is the clock input to the IDT71V546. Except for OE, all timing references for the device are made with respect to the rising edge of CLK.
I/O0-I/O31 I/OP1-I/OP4	Data Input/Output	I/O	N/A	Synchronous data input/output (I/O) pins. Both the data input path and data output path are registered and triggered by the rising edge of CLK.
LBO	Linear Burst	I Order	LOW	Burst order selection input. When LBO is high the Interleaved (Intel) burst sequence is selected. When LBO is low the Linear (PowerPC) burst sequence is selected. LBO is a static DC input.
OE	Output Enable	I	LOW	Asynchronous output enable. OE must be low to read data from the 71V546. When OE is high the I/O pins are in a high-impedance state. OE does not need to be actively controlled for read and write cycles. In normal operation, OE can be tied low.
VDD	Power Supply	N/A	N/A	3.3V power supply input.
VSS	Ground	N/A	N/A	Ground pin.

**NOTE:**

3821 tbl 02

1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

### FUNCTIONAL BLOCK DIAGRAM



### RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	V <sub>SS</sub>	V <sub>DD</sub>
Commercial	0°C to +70°C	0V	3.3V +/-5%

3821 tbl 03

### RECOMMENDED DC OPERATING CONDITIONS

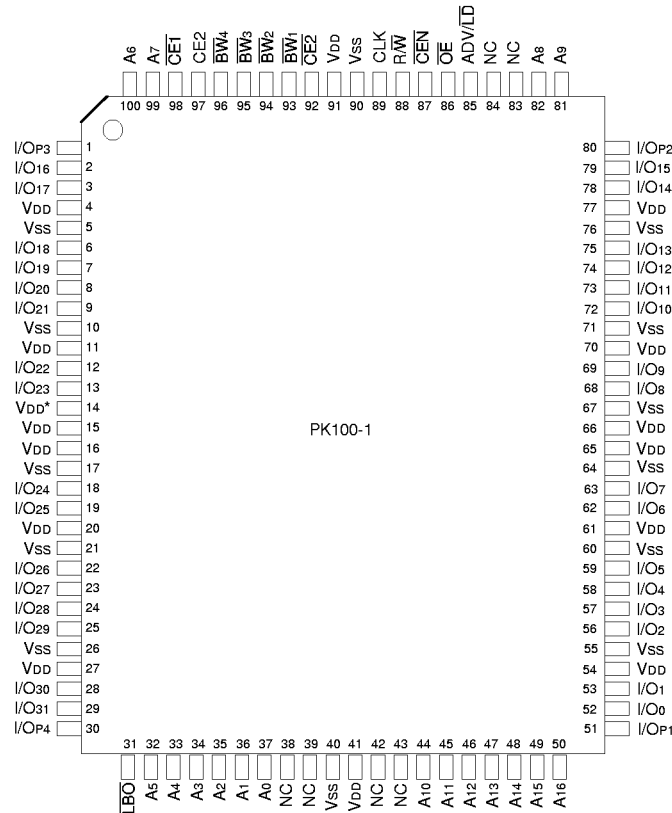
Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Core Supply Voltage	3.135	3.3	3.465	V
V <sub>SS</sub>	Core Ground Supply	0	0	0	V
V <sub>IH</sub>	Input High Voltage - Inputs	2.0	—	4.6	V
V <sub>IH</sub>	Input High Voltage - I/O	2.0	—	V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.5 <sup>(1)</sup>	—	0.8	V

**NOTES:**

- V<sub>IL</sub> (min.) = -1.0V for pulse width less than t<sub>CYC</sub>/2, once per cycle.
- V<sub>IH</sub> (max.) = +6.0V for pulse width less than t<sub>CYC</sub>/2, once per cycle.

3821 tbl 04

## PIN CONFIGURATION



3821 drw 02

## TOP VIEW TQFP

\* Pin 14 does not have to be connected directly to VDD as long as the input voltage is  $\geq V_{IH}$ .

\* Pin 83 and 84 are reserved for future A17 (8M) and A18 (16M) respectively.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Rating	Com'l.	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
$V_{TERM}^{(3)}$	Terminal Voltage with Respect to GND	-0.5 to VDD+0.5	V
$T_A$	Operating Temperature	0 to +70	°C
$T_{BIAS}$	Temperature Under Bias	-55 to +125	°C
$T_{STG}$	Storage Temperature	-55 to +125	°C
$P_T$	Power Dissipation	2.0	W
$I_{OUT}$	DC Output Current	50	mA

### NOTES:

3821 tbl 05

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- VDD and Input terminals only.
- I/O terminals.

## CAPACITANCE

( $T_A = +25^\circ\text{C}$ ,  $f = 1.0\text{MHz}$ , TQFP package)

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 3\text{dV}$	5	pF
$C_{I/O}$	I/O Capacitance	$V_{OUT} = 3\text{dV}$	7	pF

### NOTE:

3821 tbl 06

- This parameter is guaranteed by device characterization, but not production tested.

### SYNCHRONOUS TRUTH TABLE<sup>(1)</sup>

$\overline{CEN}$	R/ $\overline{W}$	Chip <sup>(5)</sup> Enable	ADV/ $\overline{LD}$	$\overline{BWx}$	ADDRESS USED	PREVIOUS CYCLE	CURRENT CYCLE	I/O (2 cycles later)
L	L	Select	L	Valid	External	X	LOAD WRITE	D
L	H	Select	L	X	External	X	LOAD READ	Q
L	X	X	H	Valid	Internal	LOAD WRITE / BURST WRITE	BURST WRITE (Advance burst counter) <sup>(2)</sup>	D
L	X	X	H	X	Internal	LOAD READ / BURST READ	BURST READ (Advance burst counter) <sup>(2)</sup>	Q
L	X	Deselect	L	X	X	X	DESELECT or STOP <sup>(3)</sup>	HiZ
L	X	X	H	X	X	DESELECT / NOOP	NOOP	HiZ
H	X	X	X	X	X	X	SUSPEND <sup>(4)</sup>	Previous value

**NOTES:**

3821 tbl 07

1. L = V<sub>IL</sub>, H = V<sub>IH</sub>, X = Don't Care.
2. When ADV/ $\overline{LD}$  signal is sampled high, the internal burst counter is incremented. The R/ $\overline{W}$  signal is ignored when the counter is advanced. Therefore the nature of the burst cycle (Read or Write) is determined by the status of the R/ $\overline{W}$  signal when the first address is loaded at the beginning of the burst cycle.
3. Deselect cycle is initiated when either ( $\overline{CE1}$ , or  $\overline{CE2}$  is sampled high or CE2 is sampled low) and ADV/ $\overline{LD}$  is sampled low at rising edge of clock. The data bus will tri-state two cycles after deselect is initiated.
4. When  $\overline{CEN}$  is sampled high at the rising edge of clock, that clock edge is blocked from propagating through the part. The state of all the internal registers and the I/O's remains unchanged.
5. To select the chip requires  $\overline{CE1} = L$ ,  $\overline{CE2} = L$ , CE2 = H on these chip enables. Chip is deselected if either one of the chip enables is false.
6. Device Outputs are ensured to be in High-Z after the first rising edge of clock upon power-up.

### PARTIAL TRUTH TABLE FOR WRITES<sup>(1)</sup>

OPERATION	R/ $\overline{W}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$
READ	H	X	X	X	X
WRITE ALL BYTES	L	L	L	L	L
WRITE BYTE 1 (I/O [0:7], I/OP <sub>1</sub> ) <sup>(2)</sup>	L	L	H	H	H
WRITE BYTE 2 (I/O [8:15], I/OP <sub>2</sub> ) <sup>(2)</sup>	L	H	L	H	H
WRITE BYTE 3 (I/O [16:23], I/OP <sub>3</sub> ) <sup>(2)</sup>	L	H	H	L	H
WRITE BYTE 4 (I/O [24:31], I/OP <sub>4</sub> ) <sup>(2)</sup>	L	H	H	H	L
NO WRITE	L	H	H	H	H

**NOTES:**

3821 tbl 08

1. L = V<sub>IL</sub>, H = V<sub>IH</sub>, X = Don't Care.
2. Multiple bytes may be selected during the same cycle.

### INTERLEAVED BURST SEQUENCE TABLE ( $\overline{LBO} = V_{DD}$ )

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	0	0	1	1	1	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address <sup>(1)</sup>	1	1	1	0	0	1	0	0

**NOTE:**

3821 tbl 09

1. Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

### LINEAR BURST SEQUENCE TABLE ( $\overline{LBO} = V_{SS}$ )

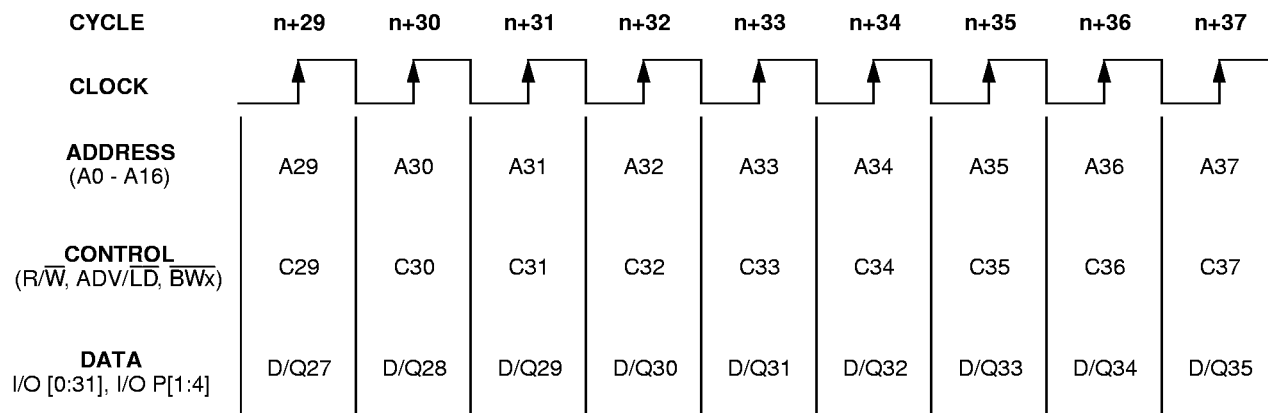
	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	1	0	1	1	0	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address <sup>(1)</sup>	1	1	0	0	0	1	1	0

**NOTE:**

3821 tbl 10

1. Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

## FUNCTIONAL TIMING DIAGRAM



3821 drw 03

### Note:

1) This assumes  $\overline{CEN}$ ,  $\overline{CE1}$ ,  $CE2$ ,  $\overline{CE2}$  are all true.

2) All Address, Control and Data\_In are only required to meet set-up and hold time with respect to the rising edge of clock. Data\_Out is valid after a clock-to-data delay from the rising edge of clock.

## DEVICE OPERATION - SHOWING MIXED LOAD, BURST, DESELECT AND NOOP CYCLES

Cycle	Address	R/W	ADV/LD	$\overline{CE}^{(1)}$	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	A0	H	L	L	L	X	X	X	Load read
n+1	X	X	H	X	L	X	X	X	Burst read
n+2	A1	H	L	L	L	X	L	Q0	Load read
n+3	X	X	L	H	L	X	L	Q0+1	Deselect or STOP
n+4	X	X	H	X	L	X	L	Q1	NOOP
n+5	A2	H	L	L	L	X	X	Z	Load read
n+6	X	X	H	X	L	X	X	Z	Burst read
n+7	X	X	L	H	L	X	L	Q2	Deselect or STOP
n+8	A3	L	L	L	L	L	L	Q2+1	Load write
n+9	X	X	H	X	L	L	X	Z	Burst write
n+10	A4	L	L	L	L	L	X	D3	Load write
n+11	X	X	L	H	L	X	X	D3+1	Deselect or STOP
n+12	X	X	H	X	L	X	X	D4	NOOP
n+13	A5	L	L	L	L	L	X	Z	Load write
n+14	A6	H	L	L	L	X	X	Z	Load read
n+15	A7	L	L	L	L	L	X	D5	Load write
n+16	X	X	H	X	L	L	L	Q6	Burst write
n+17	A8	H	L	L	L	X	X	D7	Load read
n+18	X	X	H	X	L	X	X	D7+1	Burst read
n+19	A9	L	L	L	L	L	L	Q8	Load write

### NOTES

3821 tbl 11

- $\overline{CE} = L$  is defined as  $\overline{CE1} = L$ ,  $\overline{CE2} = L$  and  $CE2 = H$ .  $\overline{CE} = H$  is defined as  $\overline{CE1} = H$ ,  $\overline{CE2} = H$  or  $CE2 = L$ .
- H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.

## READ OPERATION

Cycle	Address	R/ $\overline{W}$	ADV/ $\overline{LD}$	$\overline{CE}^{(2)}$	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	A0	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	X	X	L	X	X	X	Clock Setup Valid
n+2	X	X	X	X	X	X	L	Q0	Contents of Address A0 Read Out

**NOTE:**

3821 tbl 12

1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2.  $\overline{CE} = L$  is defined as  $\overline{CE1} = L$ ,  $\overline{CE2} = L$  and  $CE2 = H$ .  $\overline{CE} = H$  is defined as  $\overline{CE1} = H$ ,  $\overline{CE2} = H$  or  $CE2 = L$ .

## BURST READ OPERATION

Cycle	Address	R/ $\overline{W}$	ADV/ $\overline{LD}$	$\overline{CE}^{(2)}$	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	A <sub>0</sub>	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	H	X	L	X	X	X	Clock Setup Valid, Advance Counter
n+2	X	X	H	X	L	X	L	Q <sub>0</sub>	Address A <sub>0</sub> Read Out, Inc. Count
n+3	X	X	H	X	L	X	L	Q <sub>0+1</sub>	Address A <sub>0+1</sub> Read Out, Inc. Count
n+4	X	X	H	X	L	X	L	Q <sub>0+2</sub>	Address A <sub>0+2</sub> Read Out, Inc. Count
n+5	A <sub>1</sub>	H	L	L	L	X	L	Q <sub>0+3</sub>	Address A <sub>0+3</sub> Read Out, Load A <sub>1</sub>
n+6	X	X	H	X	L	X	L	Q <sub>0</sub>	Address A <sub>0</sub> Read Out, Inc. Count
n+7	X	X	H	X	L	X	L	Q <sub>1</sub>	Address A <sub>1</sub> Read Out, Inc. Count
n+8	A <sub>2</sub>	H	L	L	L	X	L	Q <sub>1+1</sub>	Address A <sub>1+1</sub> Read Out, Load A <sub>2</sub>

**NOTE:**

3821 tbl 13

1. H = High; L = Low; X = Don't Care; Z = High Impedance..
2.  $\overline{CE} = L$  is defined as  $\overline{CE1} = L$ ,  $\overline{CE2} = L$  and  $CE2 = H$ .  $\overline{CE} = H$  is defined as  $\overline{CE1} = H$ ,  $\overline{CE2} = H$  or  $CE2 = L$ .

## WRITE OPERATION

Cycle	Address	R/ $\overline{W}$	ADV/ $\overline{LD}$	$\overline{CE}^{(2)}$	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	A0	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	X	X	L	X	X	X	Clock Setup Valid
n+2	X	X	X	X	L	X	X	D0	Write to Address A0

**NOTE:**

3821 tbl 14

1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2.  $\overline{CE} = L$  is defined as  $\overline{CE1} = L$ ,  $\overline{CE2} = L$  and  $CE2 = H$ .  $\overline{CE} = H$  is defined as  $\overline{CE1} = H$ ,  $\overline{CE2} = H$  or  $CE2 = L$ .

## BURST WRITE OPERATION

Cycle	Address	R/ $\overline{W}$	ADV/ $\overline{LD}$	$\overline{CE}^{(2)}$	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	A <sub>0</sub>	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	H	X	L	L	X	X	Clock Setup Valid, Inc. Count
n+2	X	X	H	X	L	L	X	D <sub>0</sub>	Address A <sub>0</sub> Write, Inc. Count
n+3	X	X	H	X	L	L	X	D <sub>0+1</sub>	Address A <sub>0+1</sub> Write, Inc. Count
n+4	X	X	H	X	L	L	X	D <sub>0+2</sub>	Address A <sub>0+2</sub> Write, Inc. Count
n+5	A <sub>1</sub>	L	L	L	L	L	X	D <sub>0+3</sub>	Address A <sub>0+3</sub> Write, Load A <sub>1</sub>
n+6	X	X	H	X	L	L	X	D <sub>0</sub>	Address A <sub>0</sub> Write, Inc. Count
n+7	X	X	H	X	L	L	X	D <sub>1</sub>	Address A <sub>1</sub> Write, Inc. Count
n+8	A <sub>2</sub>	L	L	L	L	L	X	D <sub>1+1</sub>	Address A <sub>1+1</sub> Write, Load A <sub>2</sub>

**NOTE:**

3821 tbl 15

1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2.  $\overline{CE} = L$  is defined as  $\overline{CE1} = L$ ,  $\overline{CE2} = L$  and  $CE2 = H$ .  $\overline{CE} = H$  is defined as  $\overline{CE1} = H$ ,  $\overline{CE2} = H$  or  $CE2 = L$ .

### READ OPERATION WITH CLOCK ENABLE USED

Cycle	Address	R/ $\overline{W}$	ADV/ $\overline{LD}$	$\overline{CE}^{(2)}$	$\overline{CEN}$	$\overline{BW}_x$	$\overline{OE}$	I/O	Comments
n	A0	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored.
n+2	A1	H	L	L	L	X	X	X	Clock Valid
n+3	X	X	X	X	H	X	L	Q0	Clock Ignored. Data Q0 is on the bus
n+4	X	X	X	X	H	X	L	Q0	Clock Ignored. Data Q0 is on the bus
n+5	A2	H	L	L	L	X	L	Q0	Address A0 Read out (bus trans.)
n+6	A3	H	L	L	L	X	L	Q1	Address A1 Read out (bus trans.)
n+7	A4	H	L	L	L	X	L	Q2	Address A2 Read out (bus trans.)

**NOTE:**

3821 tbl 16

1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2.  $\overline{CE} = L$  is defined as  $\overline{CE1} = L$ ,  $\overline{CE2} = L$  and  $CE2 = H$ .  $\overline{CE} = H$  is defined as  $\overline{CE1} = H$ ,  $\overline{CE2} = H$  or  $CE2 = L$ .

### WRITE OPERATION WITH CLOCK ENABLE USED

Cycle	Address	R/ $\overline{W}$	ADV/ $\overline{LD}$	$\overline{CE}^{(2)}$	$\overline{CEN}$	$\overline{BW}_x$	$\overline{OE}$	I/O	Comments
n	A0	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored.
n+2	A1	L	L	L	L	L	X	X	Clock Valid
n+3	X	X	X	X	H	X	X	X	Clock Ignored
n+4	X	X	X	X	H	X	X	X	Clock Ignored
n+5	A2	L	L	L	L	L	X	D0	Write data D0
n+6	A3	L	L	L	L	L	X	D1	Write data D1
n+7	A4	L	L	L	L	L	X	D2	Write data D2

**NOTE:**

3821 tbl 17

1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2.  $\overline{CE} = L$  is defined as  $\overline{CE1} = L$ ,  $\overline{CE2} = L$  and  $CE2 = H$ .  $\overline{CE} = H$  is defined as  $\overline{CE1} = H$ ,  $\overline{CE2} = H$  or  $CE2 = L$ .



### READ OPERATION WITH CHIP ENABLE USED<sup>(1)</sup>

Cycle	Address	R/ $\overline{W}$	ADV/ $\overline{LD}$	$\overline{CE}^{(2)}$	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	X	X	L	H	L	X	X	?	Deselected
n+1	X	X	L	H	L	X	X	?	Deselected
n+2	A0	H	L	L	L	X	X	Z	Address and Control meet setup
n+3	X	X	L	H	L	X	X	Z	Deselected or STOP
n+4	A1	H	L	L	L	X	L	Q0	Address A0 read out. Load A1
n+5	X	X	L	H	L	X	X	Z	Deselected or STOP
n+6	X	X	L	H	L	X	L	Q1	Address A1 Read out. Deselected
n+7	A2	H	L	L	L	X	X	Z	Address and control meet setup
n+8	X	X	L	H	L	X	X	Z	Deselected or STOP
n+9	X	X	L	H	L	X	L	Q2	Address A2 read out. Deselected

**NOTES:**

3821 tbl 18

1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2.  $\overline{CE} = L$  is defined as  $\overline{CE1} = L$ ,  $\overline{CE2} = L$  and  $CE2 = H$ .  $\overline{CE} = H$  is defined as  $\overline{CE1} = H$ ,  $\overline{CE2} = H$  or  $CE2 = L$ .
3. Device Outputs are ensured to be in High-Z after the first rising edge of clock upon power-up.

### WRITE OPERATION WITH CHIP ENABLE USED<sup>(1)</sup>

Cycle	Address	R/ $\overline{W}$	ADV/ $\overline{LD}$	$\overline{CE}^{(2)}$	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	X	X	L	H	L	X	X	?	Deselected
n+1	X	X	L	H	L	X	X	?	Deselected
n+2	A0	L	L	L	L	L	X	Z	Address and Control meet setup
n+3	X	X	L	H	L	X	X	Z	Deselected or STOP
n+4	A1	L	L	L	L	L	X	D0	Data D0 Write In. Load A1
n+5	X	X	L	H	L	X	X	Z	Deselected or STOP
n+6	X	X	L	H	L	X	X	D1	Data D1 Write In. Deselected
n+7	A2	L	L	L	L	L	X	Z	Address and control meet setup
n+8	X	X	L	H	L	X	X	Z	Deselected or STOP
n+9	X	X	L	H	L	X	X	D2	Data D2 Write In. Deselected

**NOTES:**

3821 tbl 19

1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2.  $\overline{CE} = L$  is defined as  $\overline{CE1} = L$ ,  $\overline{CE2} = L$  and  $CE2 = H$ .  $\overline{CE} = H$  is defined as  $\overline{CE1} = H$ ,  $\overline{CE2} = H$  or  $CE2 = L$ .

### DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V<sub>DD</sub> = 3.3V +/-5%)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I <sub>LI</sub>	Input Leakage Current	V <sub>DD</sub> = Max., V <sub>IN</sub> = 0V to V <sub>DD</sub>	—	5	μA
I <sub>LI</sub>	$\overline{\text{LBO}}$ Input Leakage Current <sup>(1)</sup>	V <sub>DD</sub> = Max., V <sub>IN</sub> = 0V to V <sub>DD</sub>	—	30	μA
I <sub>LO</sub>	Output Leakage Current	$\overline{\text{CE}} \geq V_{IH}$ or $\overline{\text{OE}} \geq V_{IH}$ , V <sub>OUT</sub> = 0V to V <sub>DD</sub> , V <sub>DD</sub> = Max.	—	5	μA
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 5mA, V <sub>DD</sub> = Min.	—	0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -5mA, V <sub>DD</sub> = Min.	2.4	—	V

**NOTE:**

1. The  $\overline{\text{LBO}}$  pin will be internally pulled to V<sub>DD</sub> if it is not actively driven in the application.

3821 tbl 20

### DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE<sup>(1)</sup> (V<sub>DD</sub> = 3.3V +/-5%, V<sub>HD</sub> = V<sub>DD</sub>-0.2V, V<sub>LD</sub> = 0.2V)

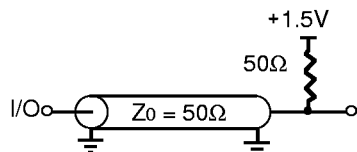
Symbol	Parameter	Test Condition	S4	SA4	S5	S6	Unit
I <sub>DD</sub>	Operating Power Supply Current	Device Selected, Outputs Open, ADV/ $\overline{\text{LD}}$ = X, V <sub>DD</sub> = Max., V <sub>IN</sub> ≥ V <sub>IH</sub> or ≤ V <sub>IL</sub> , f = f <sub>MAX</sub> <sup>(2)</sup>	300	275	250	225	mA
ISB1	CMOS Standby Power Supply Current	Device Deselected, Outputs Open, V <sub>DD</sub> = Max., V <sub>IN</sub> ≥ V <sub>HD</sub> or ≤ V <sub>LD</sub> , f = 0 <sup>(2)</sup>	20	20	20	20	mA
ISB2	Clock Running Power Supply Current	Device Deselected, Outputs Open V <sub>DD</sub> = Max., V <sub>IN</sub> ≥ V <sub>HD</sub> or ≤ V <sub>LD</sub> , f = f <sub>MAX</sub> <sup>(2)</sup>	90	85	80	70	mA
ISB3	Idle Power Supply Current	Device Selected, Outputs Open, $\overline{\text{CEN}} \geq V_{IH}$ V <sub>DD</sub> = Max., V <sub>IN</sub> ≥ V <sub>HD</sub> or ≤ V <sub>LD</sub> , f = f <sub>MAX</sub> <sup>(2)</sup>	25	25	25	25	mA

**NOTES:**

- All values are maximum guaranteed values.
- At f = f<sub>MAX</sub>, inputs are cycling at the maximum frequency of read cycles of 1/t<sub>CYC</sub>; f=0 means no input lines are changing.

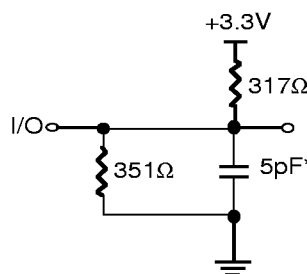
3821 tbl 21

### AC TEST LOADS



3821 drw 04

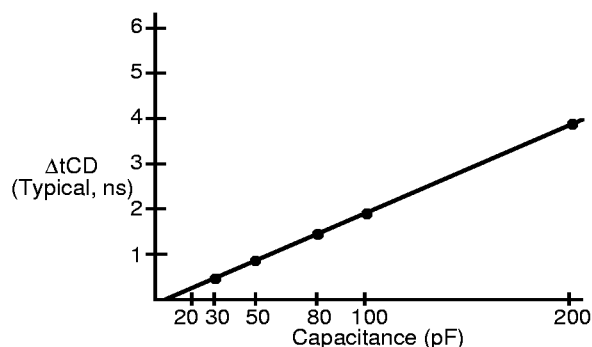
Figure 1. AC Test Load



3821 drw 05

Figure 2. AC Test Load (for t<sub>OHZ</sub>, t<sub>CHZ</sub>, t<sub>OLZ</sub>, and t<sub>DC1</sub>)

\* Including scope and jig



3821 drw 06

Figure 3. Lumped Capacitive Load, Typical Derating

### AC TEST CONDITIONS

Input Pulse Levels	0 to 3V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
AC Test Load	See Figures 1 & 2

3821 tbl 22

## AC ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = 3.3V +/-5%, T<sub>A</sub> = 0 to 70°C)

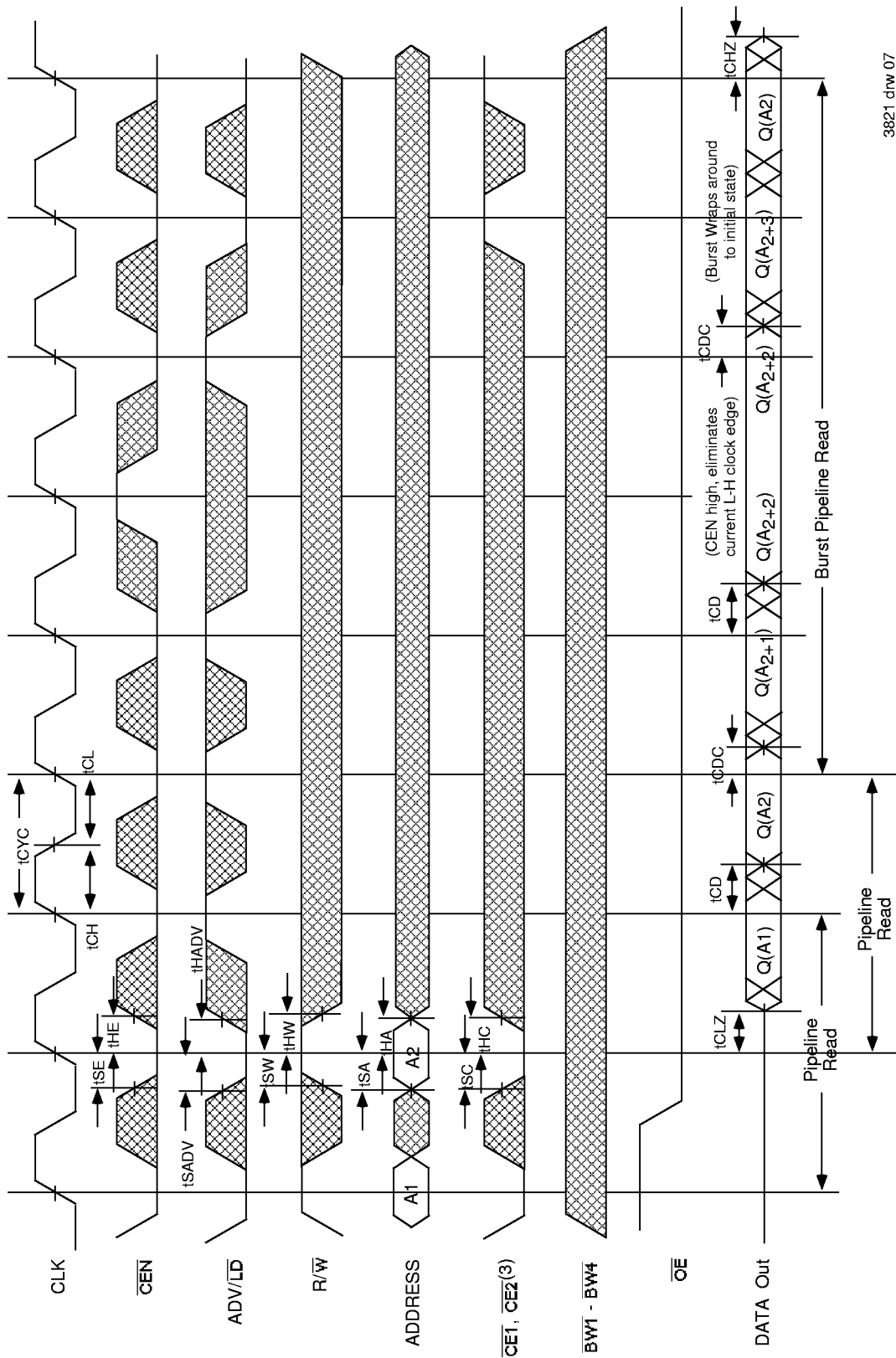
Symbol	Parameter	IDT71V546S4		IDT71V546SA4		IDT71V546S5		IDT71V546S6		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Clock Parameters</b>										
t <sub>CYC</sub>	Clock Cycle Time	7.5	—	8.5	—	10	—	12	—	ns
t <sub>F</sub> <sup>(1)</sup>	Clock Frequency	—	133	—	117	—	100	—	83	MHz
t <sub>CH</sub> <sup>(2)</sup>	Clock High Pulse Width	2.5	—	3	—	3.5	—	4	—	ns
t <sub>CL</sub> <sup>(2)</sup>	Clock Low Pulse Width	2.5	—	3	—	3.5	—	4	—	ns
<b>Output Parameters</b>										
t <sub>CD</sub>	Clock High to Valid Data	—	4.2	—	4.5	—	5	—	6	ns
t <sub>CDC</sub>	Clock High to Data Change	1.5	—	1.5	—	1.5	—	1.5	—	ns
t <sub>CLZ</sub> <sup>(3, 4, 5)</sup>	Clock High to Output Active	1.5	—	1.5	—	1.5	—	1.5	—	ns
t <sub>CHZ</sub> <sup>(3, 4, 5)</sup>	Clock High to Data High-Z	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	ns
t <sub>OE</sub>	Output Enable Access Time	—	4.2	—	4.5	—	5	—	6	ns
t <sub>OLZ</sub> <sup>(3, 4)</sup>	Output Enable Low to Data Active	0	—	0	—	0	—	0	—	ns
t <sub>OHZ</sub> <sup>(3, 4)</sup>	Output Enable High to Data High-Z	—	3.5	—	3.5	—	3.5	—	3.5	ns
<b>Set Up Times</b>										
t <sub>SE</sub>	Clock Enable Setup Time	2.0	—	2.0	—	2.2	—	2.5	—	ns
t <sub>SA</sub>	Address Setup Time	2.0	—	2.0	—	2.2	—	2.5	—	ns
t <sub>SD</sub>	Data In Setup Time	1.7	—	1.7	—	2.0	—	2.5	—	ns
t <sub>SW</sub>	Read/Write (R/W) Setup Time	2.0	—	2.0	—	2.2	—	2.5	—	ns
t <sub>SADV</sub>	Advance/Load (ADV/LD) Setup Time	2.0	—	2.0	—	2.2	—	2.5	—	ns
t <sub>SC</sub>	Chip Enable/Select Setup Time	2.0	—	2.0	—	2.2	—	2.5	—	ns
t <sub>SB</sub>	Byte Write Enable (BWx) Setup Time	2.0	—	2.0	—	2.2	—	2.5	—	ns
<b>Hold Times</b>										
t <sub>HE</sub>	Clock Enable Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t <sub>HA</sub>	Address Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t <sub>HD</sub>	Data In Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t <sub>HW</sub>	Read/Write (R/W) Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t <sub>HADV</sub>	Advance/Load (ADV/LD) Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t <sub>HC</sub>	Chip Enable/Select Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t <sub>HB</sub>	Byte Write Enable (BWx) Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns

**NOTES:**

1. t<sub>F</sub> = 1/t<sub>CYC</sub>.
2. Measured as HIGH above 2.0V and LOW below 0.8V.
3. Transition is measured ±200mV from steady-state.
4. These parameters are guaranteed with the AC load (Figure 2) by device characterization. They are not production tested.
5. To avoid bus contention, the output buffers are designed such that t<sub>CHZ</sub> (device turn-off) is about 2 ns faster than t<sub>CLZ</sub> (device turn-on) at a given temperature and voltage. The specs as shown do not imply bus contention because t<sub>CLZ</sub> is a Min. parameter that is worse case at totally different test conditions (0C, 3.465V) than t<sub>CHZ</sub>, which is a Max. parameter (worse case at 70C, 3.135V). It is not possible for two SRAMs on the same board to be at such different voltage and temperature.

3821 tbl 23

# TIMING WAVEFORM OF READ CYCLE<sup>(1, 2, 3, 4)</sup>

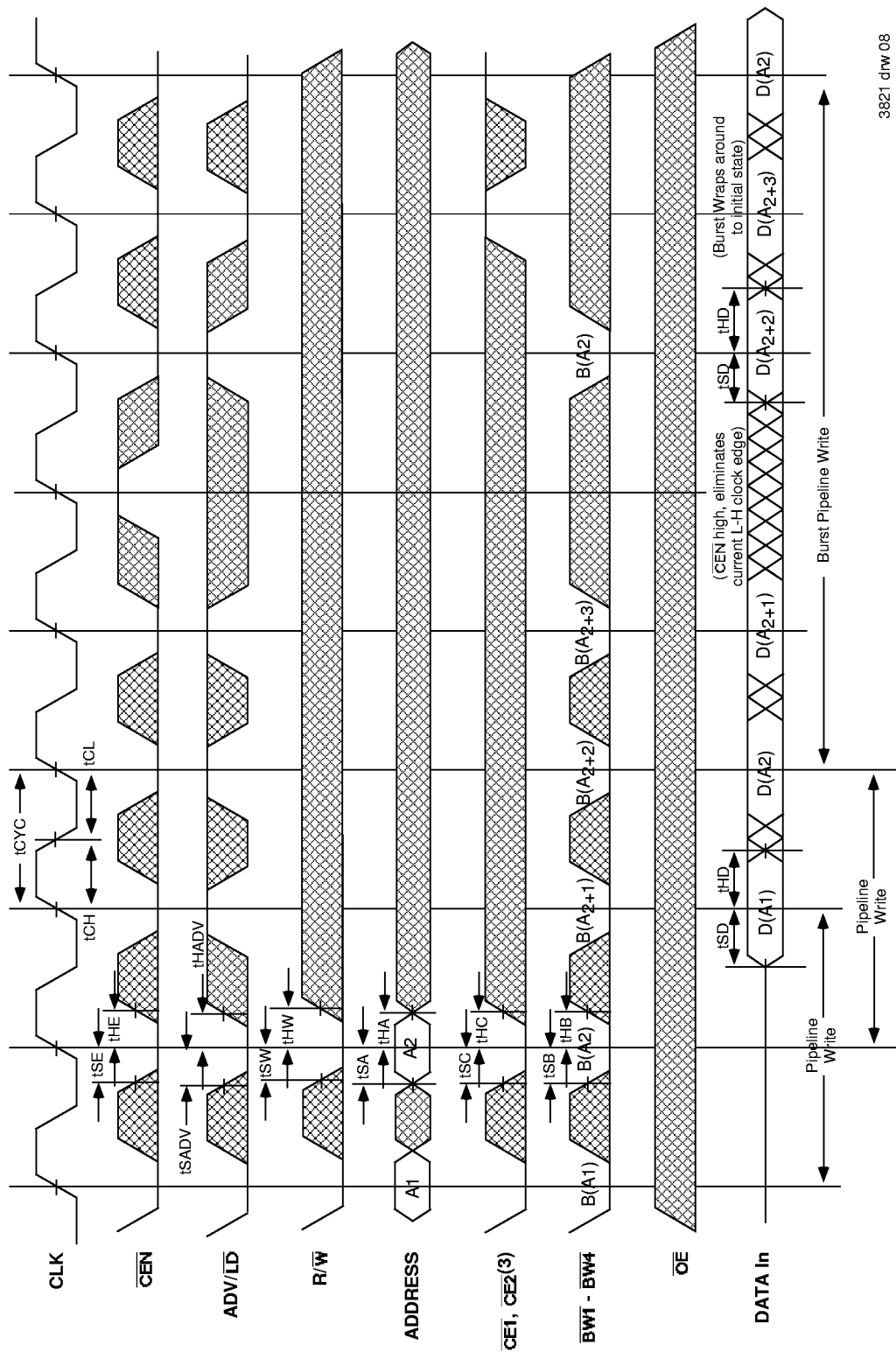


3821 drw 07

**NOTES:**

1.  $Q(A1)$  represents the first output from the external address A1.  $Q(A2)$  represents the first output from the external address A2;  $Q(A2+1)$  represents the next output data in the burst sequence of the base address A2, etc. where address bits A0 and A1 are advancing for the four word burst in the sequence defined by the state of the LBO input.
2. CE2 timing transitions are identical but inverted to the  $\overline{CE1}$  and  $\overline{CE2}$  signals. For example, when  $\overline{CE1}$  and  $\overline{CE2}$  are LOW on this waveform, CE2 is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling  $\overline{ADV/LD}$  LOW.
4.  $\overline{R/W}$  is don't care when the SRAM is bursting ( $\overline{ADV/LD}$  sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the  $\overline{R/W}$  signal when new address and control are loaded into the SRAM.

## TIMING WAVEFORM OF WRITE CYCLES(1, 2, 3, 4, 5)

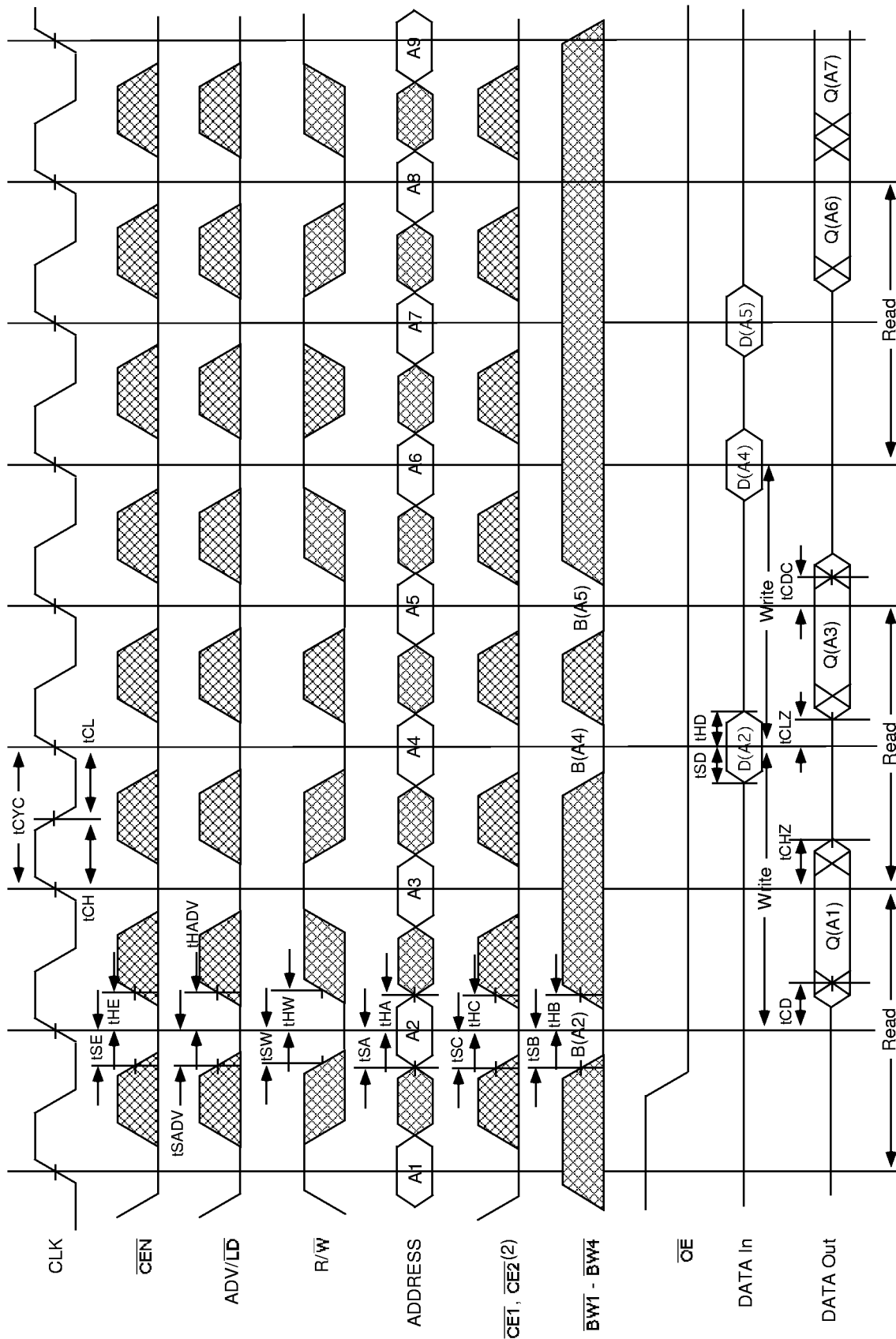


3821 drw.08

**NOTES:**

1. D(A1) represents the first input to the external address A1. D(A2) represents the first input to the external address A2; D(A2+1) represents the next input data in the burst sequence of the base address A2, etc. where address bits A0 and A1 are advancing for the four word burst in the sequence defined by the state of the LBO input.
2. CE2 timing transitions are identical but inverted to the  $\overline{CE1}$  and  $\overline{CE2}$  signals. For example, when  $\overline{CE1}$  and  $\overline{CE2}$  are LOW on this waveform, CE2 is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling  $\overline{ADV/LD}$  LOW.
4. R/W is don't care when the SRAM is bursting ( $\overline{ADV/LD}$  sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the R/W signal when new address and control are loaded into the SRAM.
5. Individual Byte Write signals (BWx) must be valid on all write and burst-write cycles. A write cycle is initiated when R/W signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

TIMING WAVEFORM OF COMBINED READ AND WRITE CYCLES<sup>(1, 2, 3)</sup>

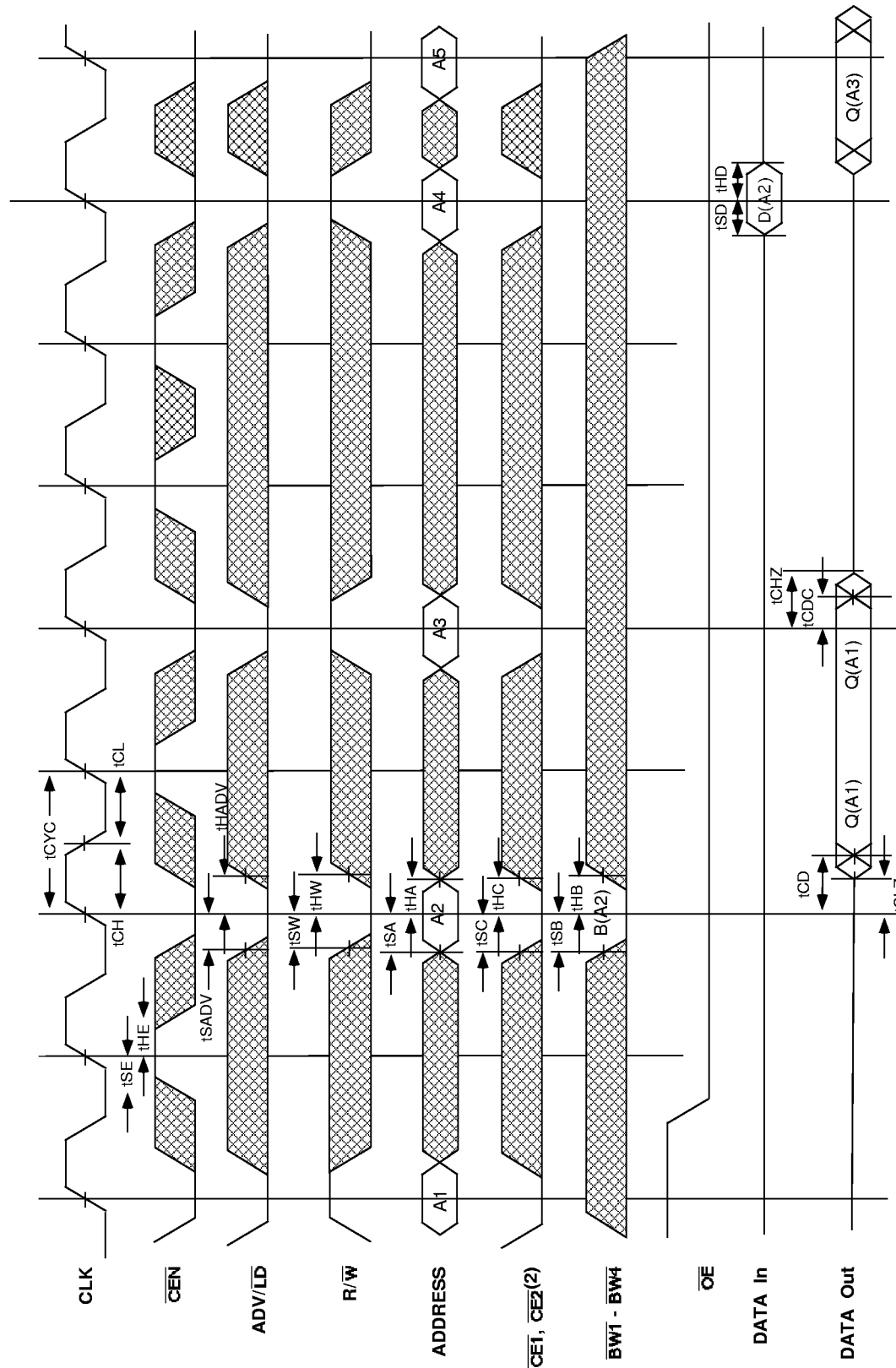


3821 drw 09

**NOTES:**

1. Q (A1) represents the first output from the external address A1. D (A2) represents the input data to the SRAM corresponding to address A2.
2. CE2 timing transitions are identical but inverted to the CE1 and CE2 signals. For example, when CE1 and CE2 are LOW on this waveform, CE2 is HIGH.
3. Individual Byte Write signals (BWx) must be valid on all write and burst-write cycles. A write cycle is initiated when R/W signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

# TIMING WAVEFORM OF $\overline{CE2}$ OPERATION<sup>(1, 2, 3, 4)</sup>

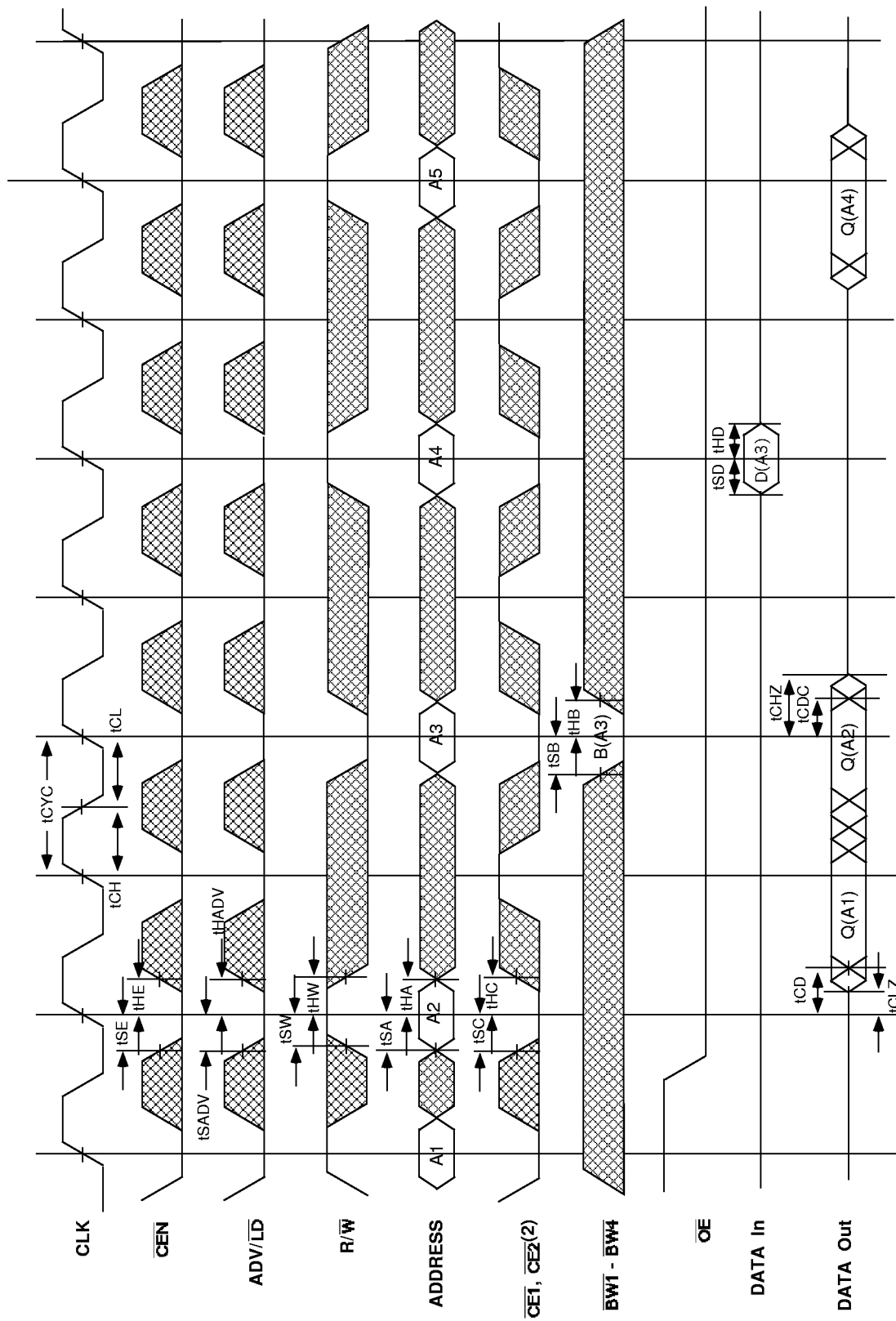


3821 drw 10

**NOTES:**

1. Q (A1) represents the first output from the external address A1. D (A2) represents the input data to the SRAM corresponding to address A2.
2.  $\overline{CE2}$  timing transitions are identical but inverted to the  $\overline{CE1}$  and  $\overline{CE2}$  signals. For example, when  $\overline{CE1}$  and  $\overline{CE2}$  are LOW on this waveform,  $\overline{CE2}$  is HIGH.
3.  $\overline{CE2}$  when sampled high on the rising edge of clock will block that L-H transition of the clock from propagating into the SRAM. The part will behave as if the L-H clock transition did not occur. All internal registers in the SRAM will retain their previous state.
4. Individual Byte Write signals ( $\overline{BWx}$ ) must be valid on all write and burst-write cycles. A write cycle is initiated when  $\overline{R/W}$  signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

### TIMING WAVEFORM OF $\overline{CS}$ OPERATION<sup>(1, 2, 3, 4)</sup>



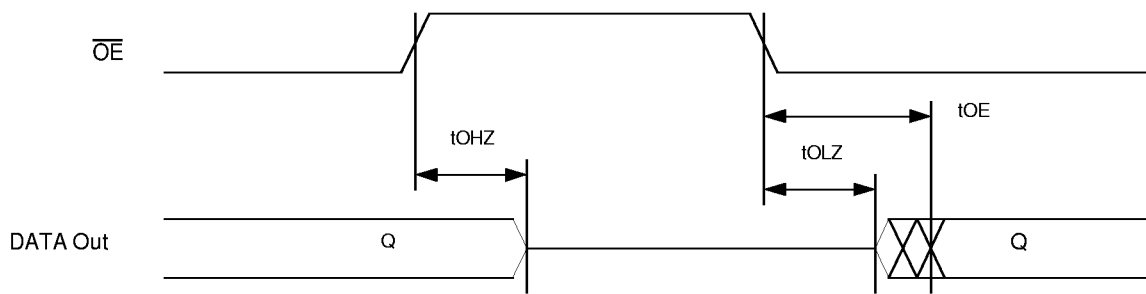
3821 drw 11

**NOTES:**

1. Q (A1) represents the first output from the external address A1. D (A3) represents the input data to the SRAM corresponding to address A3 etc.
2. CE2 timing transitions are identical but inverted to the  $\overline{CE1}$  and  $\overline{CE2}$  signals. For example, when  $\overline{CE1}$  and  $\overline{CE2}$  are LOW on this waveform, CE2 is HIGH.
3. When either one of the Chip enables ( $\overline{CE1}$ , CE2,  $\overline{CE2}$ ) is sampled inactive at the rising clock edge, a deselect cycle is initiated. The data-bus tri-states two cycles after the initiation of the deselect cycle. This allows for any pending data transfers (reads or writes) to be completed.
4. Individual Byte Write signals ( $\overline{BWx}$ ) must be valid on all write and burst-write cycles. A write cycle is initiated when R/W signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.



### TIMING WAVEFORM OF $\overline{OE}$ OPERATION<sup>(1)</sup>



3821 drw 12

**NOTE:**

1. A read operation is assumed to be in progress.

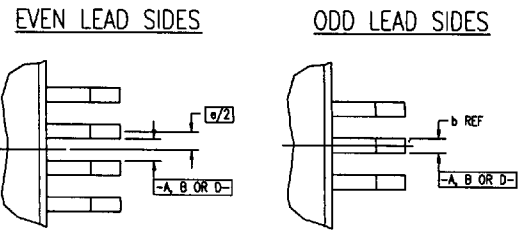
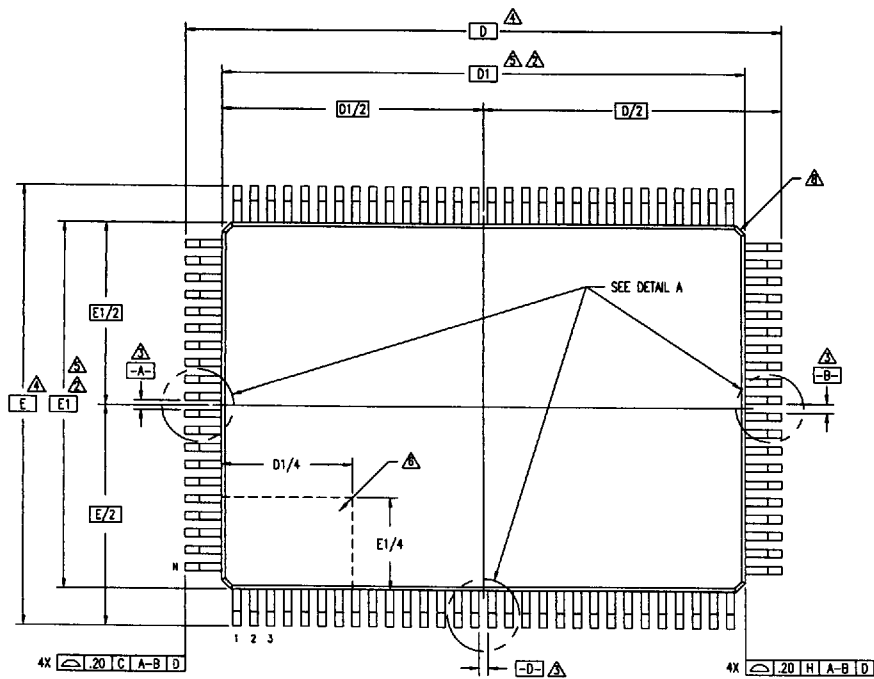
### ORDERING INFORMATION

IDT	<u>71V546</u>	<u>S</u>	<u>XX</u>	<u>PF</u>	
	Device Type	Power	Speed	Package	
				PF	} Plastic Thin Quad Flatpack, 100 pin (PK100-1)
				4 A4 5 6	
					} tCD = 4.2ns tCD = 4.5ns tCD = 5.0ns tCD = 6.0ns

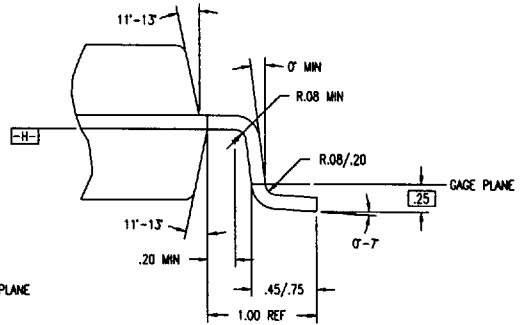
3821 drw 13

PACKAGE DIAGRAM OUTLINES  
TQFP (Continued)

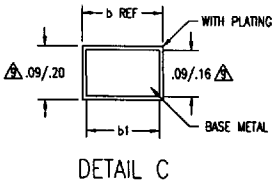
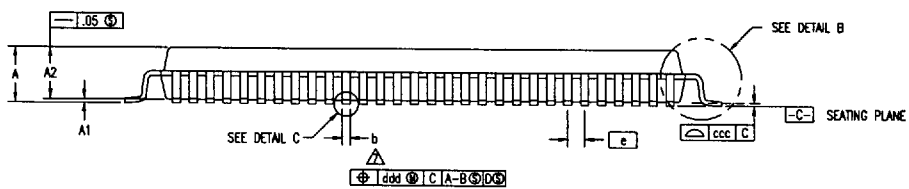
REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
26749	00	INITIAL RELEASE	08/08/94	T. VU
27389	01	REDRAW TO JEDEC FORMAT	12/12/94	



DETAIL A



DETAIL B



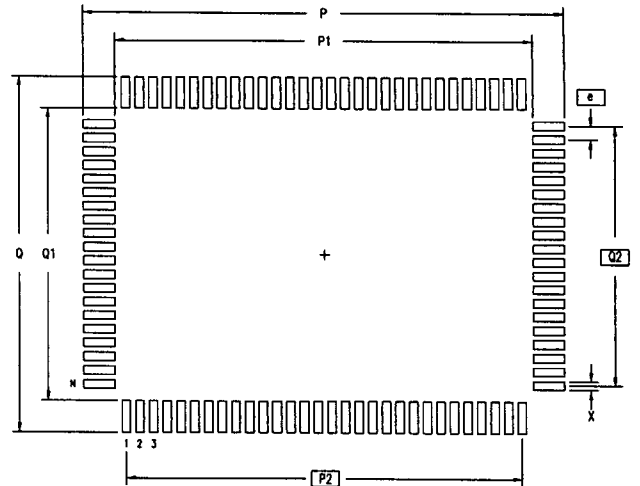
TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2875 Stander Way, Santa Clara, CA 95054 PHONE: (408) 727-8118 FAX: (408) 482-8874 TROC: 910-338-2070
DECIMAL	ANGULAR	
XXX±	±	
XXXX±		
XXXX±		
APPROVALS	DATE	TITLE
MM	08/08/94	PK. PACKAGE OUTLINE
CHECKED		14.0 X 20.0 X 1.4 mm TQFP
		1.00/.10 FORM
		SIZE
		C DRAWING No.
		PSC-4045
		REV
		01

PACKAGE DIAGRAM OUTLINES  
TQFP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
26749	00	INITIAL RELEASE	08/09/94	T. WJ
27369	01	REDRAW TO JEDEC FORMAT	12/12/94	

SYMBOL	DWG # PK100-1			NOTE	DWG # PK128-1			NOTE
	JEDEC VARIATION				JEDEC VARIATION			
	MIN	NOM	MAX		MIN	NOM	MAX	
A	-	-	1.60		-	-	1.60	
A1	.05	.10	.15		.05	.10	.15	
A2	1.35	1.40	1.45		1.35	1.40	1.45	
D	22.00 BSC			4	22.00 BSC			4
D1	20.00 BSC			5,2	20.00 BSC			5,2
E	16.00 BSC			4	16.00 BSC			4
E1	14.00 BSC			5,2	14.00 BSC			5,2
N	100				128			
ND	30				38			
NE	20				26			
e	.65 BSC				.50 BSC			
b	.22	.32	.38	7	.17	.22	.27	7
b1	.22	.30	.33		.17	.20	.23	
ccc	-	-	.10		-	-	.08	
ddd	-	-	.13		-	-	.08	

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX
P	22.80	23.00	22.80	23.00
P1	19.80	20.00	19.80	20.00
P2	18.85 BSC		18.50 BSC	
Q	16.80	17.00	16.80	17.00
Q1	13.80	14.00	13.80	14.00
Q2	12.35 BSC		12.50 BSC	
X	.30	.50	.30	.40
e	.65 BSC		.50 BSC	
N	100		128	

NOTES:

- 1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- △ TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm
- △ DATUMS [A-B] AND [-D-] TO BE DETERMINED AT DATUM PLANE [-H-]
- △ DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE [-C-]
- △ DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
- △ DETAILS OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
- △ DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
- △ EXACT SHAPE OF EACH CORNER IS OPTIONAL
- △ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
- 10 ALL DIMENSIONS ARE IN MILLIMETERS
- 11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATION DJ AND BX

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DECIMAL	ANGULAR	
XXX±	±	
XXXX±		
XXXX±		
APPROVALS DATE		TITLE
DRAWN	08/09/94	PK PACKAGE OUTLINE
CHECKED		14.0 X 20.0 X 1.4 mm TQFP
		1.00/.10 FORM
SIZE	DRAWING No.	REV
C	PSC-4045	01
DO NOT SCALE DRAWING		