MOTOROLA

MC74AC825
MC74ACT825
MC74AC826
MC74ACT826

Product Preview

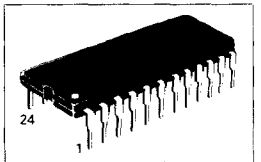
8-Bit D-Type Flip-Flop

8-BIT D-TYPE FLIP-FLOP

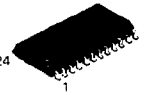
The MC74AC825/74ACT825 and MC74AC826/74ACT826 are 8-bit buffered registers. They have Clock Enable and Clear features which are ideal for parity bus interfacing in high performance microprogramming systems. Also included are multiple enables that allow multi-use control of the interface. The MC74AC825/74ACT825 has noninverting outputs; the MC74AC826/74ACT826 has inverting outputs.

The MC74AC825/74ACT825 is fully compatible with AMD's AM29825.

- Outputs Source/Sink 24 mA
- Inputs and Outputs are on Opposite Sides
- 'ACT825 and 'ACT826 Have TTL Compatible Inputs

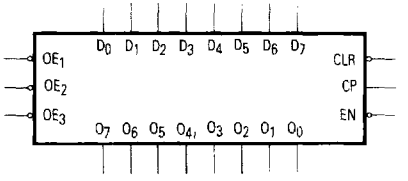


N SUFFIX
CASE 649-03
PLASTIC

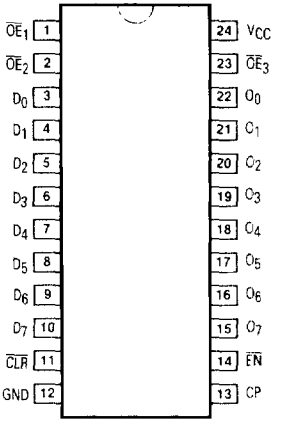


DW SUFFIX
CASE 751E-02
PLASTIC

LOGIC SYMBOL (MC74AC825/74ACT825)*



*The MC74AC826/74ACT826 has inverting outputs.



PIN NAMES

D_0–D_7	Data Inputs
O_0–O_7	Data Outputs (MC74AC825/74ACT825)
$\overline{O}_0$–$\overline{O}_7$	Data Outputs (MC74AC826/74ACT826)
$\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$	Output Enables
$\overline{EN}$	Clock Enable
$\overline{CLR}$	Clear
CP	Clock Input

5

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

FUNCTIONAL DESCRIPTION

The MC74AC825/74ACT825 and MC74AC826/74ACT826 consist of eight D-type edge-triggered flip-flops. These devices have 3-state outputs for bus systems, organized in a broadside pinning. In addition to the clock and output enable pins, the buffered clock (CP) and buffered Output Enable ($\overline{OE}$) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With $\overline{OE}_1$, $\overline{OE}_2$ and $\overline{OE}_3$ LOW, the contents of the flip-flops are available at the outputs. When one of $\overline{OE}_1$, $\overline{OE}_2$ or $\overline{OE}_3$ is HIGH, the outputs go to the high impedance state.

Operation of the OE input does not affect the state of the flip-flops. The MC74AC825/74ACT825 and MC74AC826/74ACT826 have Clear ($\overline{CLR}$) and Clock Enable ($\overline{EN}$) pins. These pins are ideal for parity bus interfacing in high performance systems.

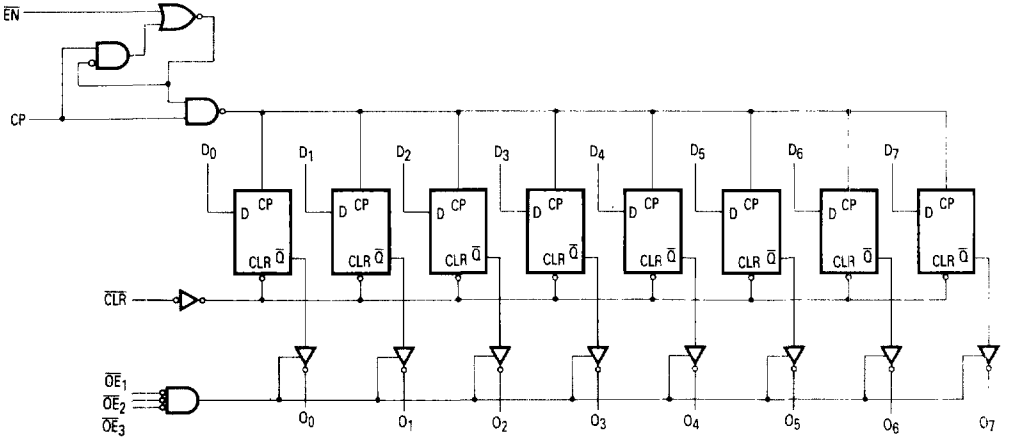
When $\overline{CLR}$ is LOW and $\overline{OE}$ is LOW, the outputs are LOW. When $\overline{CLR}$ is HIGH, data can be entered into the flip-flops. When $\overline{EN}$ is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When $\overline{EN}$ is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

FUNCTION TABLE

Inputs					Internal	Outputs		Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	CP	Dn	Q	O ('825)	$\overline{O}$ ('826)	
H	X	L	⌐	L	L	Z	Z	High Z
H	X	L	⌐	H	H	Z	Z	High Z
H	L	X	X	X	L	Z	Z	Clear
L	L	X	X	X	L	L	L	Clear
H	H	H	X	X	NC	Z	Z	Hold
L	H	H	X	X	NC	NC	NC	Hold
H	H	L	⌐	L	L	Z	Z	Load
H	H	L	⌐	H	H	Z	Z	Load
L	H	L	⌐	L	L	L	H	Load
L	H	L	⌐	H	H	H	L	Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Transition
NC = No Change

LOGIC DIAGRAM (MC74AC825/74ACT825)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays. The MC74AC826/74ACT826 also has the same logic diagram with inverting outputs.

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT825/826)	1.5	mA	V_{IN} = V_{CC} − 2.1 V, V_{CC} = 5.5 V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0		100 125				MHz	3-3
t_{PLH}	Propagation Delay CP to O_n	3.3 5.0		9.0 6.5				ns	3-6
t_{PHL}	Propagation Delay CP to O_n	3.3 5.0		9.0 6.5				ns	3-6
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	3.3 5.0		14.5 10.5				ns	3-6
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	3.3 5.0		9.0 6.0				ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	3.3 5.0		9.5 6.5				ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	3.3 5.0		12.5 8.5				ns	3-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	3.3 5.0		12 7.5				ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF		74AC T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	3.0 2.0			ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	2.0 1.5			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{EN}$ to CP	3.3 5.0	3.0 2.0			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{EN}$ to CP	3.3 5.0	2.0 1.5			ns	3-9
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	3.5 2.5			ns	3-6
t_w	$\overline{CLR}$ Pulse Width, LOW	3.3 5.0	5.0 3.5			ns	3-6
t_{rec}	$\overline{CLR}$ to CP Recovery Time	3.3 5.0	2.0 1.5			ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0		110				MHz	3-3
t_{PLH}	Propagation Delay CP to O_n	5.0		8.0				ns	3-6
t_{PHL}	Propagation Delay CP to O_n	5.0		8.0				ns	3-6
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	5.0		12				ns	3-6
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	5.0		7.5				ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	5.0		8.0				ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	5.0		11				ns	3-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	5.0		9.5				ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF		74ACT T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	2.0			ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	1.0			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{EN}$ to CP	5.0	2.0			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{EN}$ to CP	5.0	1.5			ns	3-9
t_w	CP Pulse Width HIGH or LOW	5.0	3.0			ns	3-6
t_w	$\overline{CLR}$ Pulse Width, LOW	5.0	3.5			ns	3-6
t_{rec}	$\overline{CLR}$ to CP Recovery Time	5.0	1.5			ns	3-9

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance		pF	V_{CC} = 5.0 V