The documentation and process conversion measures necessary to comply with this document shall be completed by 30 September 2006.

INCH-POUND

MIL-PRF-19500/392H
31 July 2006
SUPERSEDING
MIL-PRF-19500/392G
26 March 2004

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, TRANSISTOR, PNP, SILICON, SWITCHING,
TYPES 2N3485A AND 2N3486A, JAN, JANTX, AND JANTXV

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for PNP silicon switching transistors. Three levels of product assurance are provided for each device type as specified in MIL-PRF-19500.

1.2 Physical dimensions. See figure 1 (TO-46).

1.3 Maximum ratings, unless otherwise specified, T_C =+ 25°C.

P_T	P_T	$R_{\theta JC}$	$R_{\theta JA}$	V_{CBO}	V_{CEO}	V_{EBO}	I_C	T_J and T_{STG}
T_A =+25°C (1) (2)	T_C = +25°C (1) (2)							
W	W	°C/W	°C/W	V dc	V dc	V dc	mA dc	°C
0.5	2.0	80	325	60	60	5	600	-65 TO +200

(1) For derate see figures 2 and 3.
(2) For thermal impedance see figures 4 and 5.

Comments, suggestions, or questions on this document should be addressed to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://assist.daps.dla.mil .

1.4 Primary electrical characteristics.

	h_{FE2} V_{CE} = 10 V dc I_C = 1.0 mA dc		h_{FE4} V_{CE} = 10 V dc I_C = 150 mA dc (1)		$\|h_{fe}\|$ V_{CE} = 20 V dc I_C = 50 mA dc f = 100 MHz	C_{obo} 100 kHz ≤ f ≤ 1 Mhz V_{CB} = 10 V dc I_E = 0	Switching			
							t_{on}	t_{off}		$t_{on} + t_{off}$ (nonsaturated)
	2N3485A	2N3486A	2N3485A	2N3486A		pF	ns	2N3485A	2N3486A	ns
Min	40	100	40	100	2.0					
Max			120	300	10	8	45	175	200	18

(1) Pulsed (see 4.5.1).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

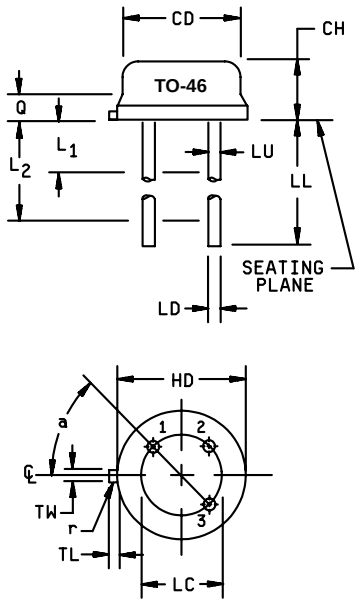
DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.178	.195	4.52	4.95	
CH	.065	.085	1.65	2.16	
HD	.209	.230	5.31	5.84	
LC	.100 TP		2.54 TP		5
LD	.016	.021	0.41	0.53	
LL	.500	1.750	12.70	44.45	6
LU	.016	.019	0.41	0.48	6
L_1		.050		1.27	6
L_2	.250		6.35		6
Q		.040		1.02	3
TL	.028	.048	0.71	1.22	8
TW	.036	.046	0.91	1.17	4
r		.010		0.25	9
α	45° TP		45° TP		5



NOTES:

1. Dimensions are in inches. Lead 1 is emitter, lead 2 is base, and lead 3 is collector.
2. Millimeters are given for general information only.
3. Symbol TL is measured from HD maximum.
4. Details of outline in this zone are optional.
5. Leads at gauge plane .054 inch (1.37 mm) +.001 inch (0.03 mm) -.000 inch (0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of TP relative to tab. Device may be measured by direct methods or by gauge.
6. Symbol LU applies between L_1 and L_2. Dimension LD applies between L_2 and LL minimum.
7. Lead number three is electrically connected to case.
8. Beyond r maximum, TW shall be held for a minimum length of .011 inch (0.28 mm).
9. Symbol r applied to both inside corners of tab.
10. In accordance with ANSI Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 1. Physical dimensions - TO-46.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500, and figure 1 (TO-46) herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.6 Electrical test requirements. The electrical test requirements shall be as specified in tables I and II.

3.7 Marking. Marking shall be in accordance with MIL-PRF-19500. At the option of the manufacturer, marking may be omitted from the body, but shall be retained on the initial container.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and table I and table II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

* 4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.3 Screening (JANTX and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table IV of MIL-PRF-19500)	Measurements
	JANTX and JANTXV levels
(1) 3c	Thermal impedance, method 3131 of MIL-STD-750. See 4.3.2.
7	Optional
9	Not applicable.
10	24 hours minimum.
11	I_{CBO2}, h_{FE4}
12	See 4.3.1.
13	Subgroup 2 of table I herein; ΔI_{CBO2} = 100 percent of initial value or 5 nA dc whichever is greater. $\Delta h_{FE4} = \pm 15$ percent.
14	Required

(1) Shall be performed anytime after temperature cycling, screen 3a; and does not need to be repeated in screening requirements.

* 4.3.1 Power burn-in conditions. Power burn-in conditions are as follows: V_{CB} = 10 - 30 V dc. Power shall be applied to achieve T_J = +135°C minimum using a minimum P_D = 75 percent of P_T maximum rated as defined in 1.3. With approval of the qualifying activity and preparing activity, alternate burn-in criteria (hours, bias conditions, T_J, and mounting conditions) may be used for JANTX and JANTXV quality levels. A justification demonstrating equivalence is required. In addition, the manufacturing site's burn-in data and performance history will be essential criteria for burn-in modification approval.

* 4.3.2 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{SW} (V_C and V_H where appropriate). Measurement delay time (t_{MD}) = 70 μs max. See table II, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500 and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in 4.4.2.1. Electrical measurements (end-points) and delta requirements for JAN, JANTX, and JANTXV shall be after each step in 4.4.2.1 and shall be in accordance with table I, subgroup 2 and 4.5.2 herein.

* 4.4.2.1 Group B inspection, (JAN, JANTX, and JANTXV). Separate samples may be used for each step. In the event of a lot failure, the resubmission requirements of MIL-PRF-19500 shall apply. In addition, all catastrophic failures during CI shall be analyzed to the extent possible to identify root cause and corrective action. Whenever a failure is identified as wafer lot and /or wafer processing related, the entire wafer lot and related devices assembled from the wafer lot shall be rejected unless an appropriate determined corrective action to eliminate the failure mode has been implemented and the devices from the wafer lot are screened to eliminate the failure mode.

Step	Method	Condition
1	1026	Steady-state life: Test condition B, 1,000 hours minimum, V_{CB} = 10 V dc, power shall be applied to achieve T_J = +150°C minimum using a minimum of P_D = 75 percent of maximum rated P_T as defined in 1.3. n = 45 devices, c = 0. The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.
2	1048	Blocking life, T_A = +150°C, V_{CB} = 80 percent of rated voltage, 48 hours minimum. n = 45 devices, c = 0.
3	1032	High-temperature life (non-operating), t = 340 hours, T_A = +200°C. n = 22, c = 0.

4.4.2.2 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements.

a. For JAN, JANTX, and JANTXV samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot. See MIL-PRF-19500.

b. Shall be chosen from an inspection lot that has been submitted to and passed table I, subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (group B for JAN, JANTX, and JANTXV) may be pulled prior to the application of final lead finish.

4.4.3 Group C inspection, Group C inspection shall be conducted in accordance with the conditions specified in 4.4.3.1 (JAN, JANTX, and JANTXV) herein for group C testing. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup 2 and 4.5.2 herein.

* 4.4.3.1 Group C inspection, table E-VII (JAN, JANTX, and JANTXV) of MIL-PRF-19500.

	Subgroup	Method	Condition
	C2	2036	Test condition E.
*	C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see 1.3) and in accordance with thermal impedance curves.
	C6		Not applicable.

4.4.3.2 Group C sample selection. Samples for subgroups in group C shall be chosen at random from any inspection lot containing the intended package type and lead finish procured to the same specification which is submitted to and passes table I tests for conformance inspection. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table II herein. Electrical measurements (end-points) and delta measurements shall be in accordance with the applicable steps of 4.5.2 and table I, subgroup 2 herein.

4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Delta requirements. Delta requirements shall be as specified below:

Step	Inspection	MIL-STD-750		Symbol	Limit
		Method	Conditions		
1	Collector-base cutoff current	3036	Bias condition D, V_{CB} = 50 V dc	ΔI_{CB02} (1)	100 percent of initial value or ±5 nA dc, whichever is greater.
2	Forward current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 150 mA dc; pulsed see 4.5.1	Δh_{FE4} (1)	±25 percent change from initial reading.

(1) Devices which exceed the table I limits for this test shall not be accepted.

* TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 1 2/						
Visual and mechanical inspection 3/	2071	n = 45 devices, c = 0.				
Solderability 3/	2026	n = 15 leads, c = 0.				
Resistance to solvents 3/ 4/	1022	n = 15 devices, c = 0.				
Temp cycling 3/	1051	Test condition C, 25 cycles. n = 22 devices, c = 0.				
Heremetic seal Fine leak Gross leak	1071	n = 22 devices, c = 0.				
Electrical measurements		Table I, subgroup 2.				
Bond strength 3/	2037	Precondition T_A = +250°C at t = 24 hours or T_A = +300°C at t = 2 hours n = 11 wires, c = 0.				
Decap internal visual (design verification)	2075	n = 4, c = 0.				
Subgroup 2						
Thermal impedance	3131	See 4.3.2.	$Z_{\theta JX}$			°C/W
Collector to base cutoff current	3036	Bias condition D; V_{CB} = 60 V dc.	I_{CBO1}		10	µA dc
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = 5 V dc.	I_{EBO1}		10	µA dc
Breakdown voltage, collector to emitter	3011	Bias condition. D; I_C = 10 mA dc pulsed (see 4.5.1).	$V_{(BR)CEO}$	60		V dc
Collector to base cutoff current	3036	Bias condition D; V_{CB} = 50 V dc.	I_{CBO2}		10	nA dc

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - Continued.						
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = 3.5 V dc.	I_{EBO2}		50	nA dc
Forward-current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 0.1 mA dc.	h_{FE1}			
2N3485A 2N3486A				40 75		
Forward-current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 1.0 mA dc.	h_{FE2}			
2N3485A 2N3486A				40 100		
Forward-current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 10 mA dc.	h_{FE3}			
2N3485A 2N3486A				40 100		
Forward-current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 150 mA dc pulsed (see 4.5.1).	h_{FE4}			
2N3485A 2N3486A				40 100	120 300	
Forward-current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 500 mA dc pulsed (see 4.5.1).	h_{FE5}			
2N3485A 2N3486A				40 50		
Saturation voltage and resistance	3071	I_C = 150 mA dc; I_B = 15 mA dc; pulsed (see 4.5.1).	$V_{CE(SAT)1}$		0.4	V dc
Saturation voltage and resistance	3071	I_C = 500 mA dc; I_B = 50 mA dc; pulsed (see 4.5.1).	$V_{CE(SAT)2}$		1.6	V dc

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - Continued.						
Base-emitter voltage (saturated)	3066	Test condition A; I_C = 150 mA dc; I_B = 15 mA dc; pulsed (see 4.5.1).	$V_{BE(SAT)1}$		1.3	V dc
Base-emitter voltage (saturated)	3066	Test condition A; I_C = 500 mA dc; I_B = 50 mA dc; pulsed (see 4.5.1).	$V_{BE(SAT)2}$		2.6	V dc
Subgroup 3						
High-temperature operation		T_A = +150°C.				
Collector-base cutoff current		Bias condition D; V_{CB} = 50 V dc.	I_{CBO3}		10	µAdc
Low-temperature operation		T_A = -55°C.				
Forward-current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 1.0 mA dc.	h_{FE6}			
2N3485A 2N3486A				20 40		
Subgroup 4						
Small signal short circuit forward current transfer ratio	3206	V_{CE} = 10 V dc; I_C = 1 mA dc; f = 1 kHz.	h_{fe}			
2N3485A 2N3486A				40 100		
Magnitude of small signal short-circuit forward-current transfer ratio	3306	V_{CE} = 20 V dc; I_C = 50 mA dc; f = 100 MHz.	$\|h_{fe}\|$	2.0	10	
Open circuit output capacitance	3236	V_{CB} = 10 V dc; I_E = 0; 100 kHz ≤ f ≤ 1 MHz.	C_{obo}		8	pF

See footnotes at end of table.

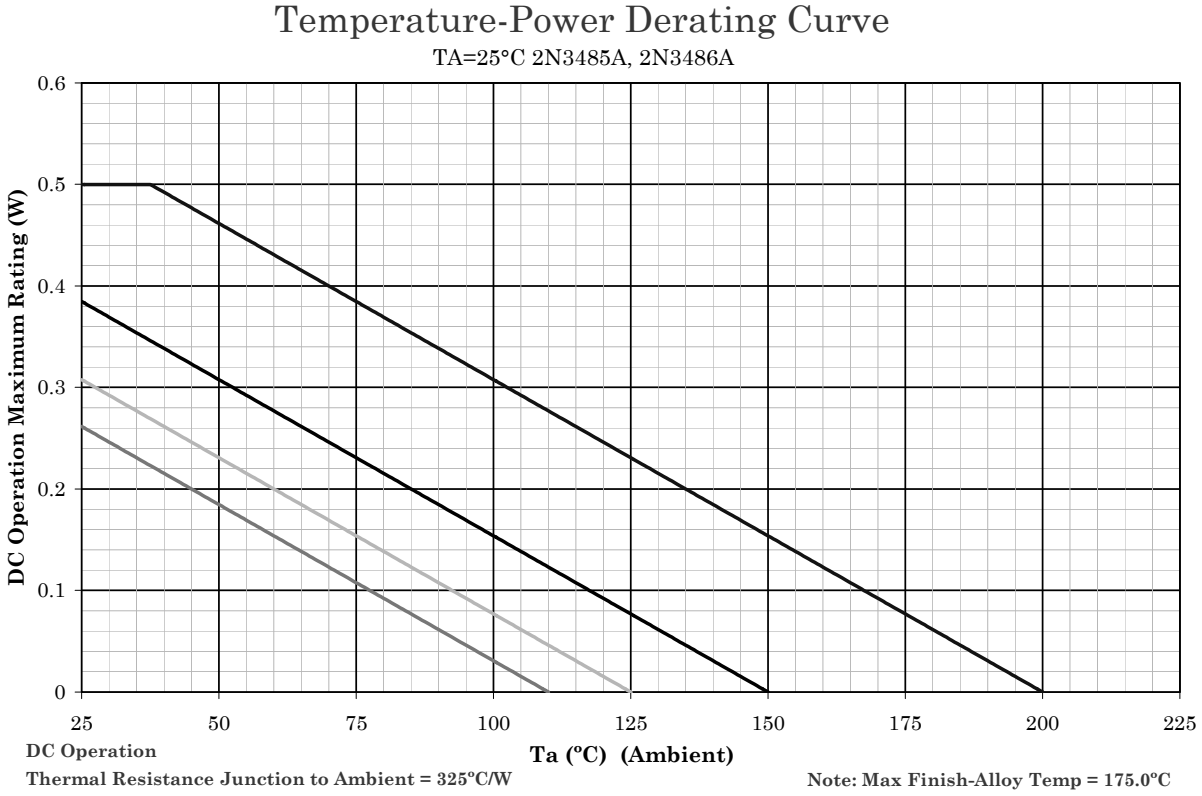
* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 4 - Continued.						
Input capacitance (output open-circuited)	3240	V_{EB} = 2.0 V dc; I_C = 0; 100 kHz ≤ f ≤ 1 MHz.	C_{ibo}		30	pF
Turn-on time		(See figure 6)	t_{on}		45	ns
Turn-off time		(See figure 7)	t_{off}			ns
2N3485A 2N3486A					175 200	
Pulse response (nonsaturated)		(See figure 8)	$t_{on} + t_{off}$		18	ns
Subgroup 5, 6, and 7						
Not applicable						

1/ For sampling plan see MIL-PRF-19500.
2/ For resubmission of failed table I, subgroup 1, double the sample size of the failed test or sequence of tests. A failure in group A, subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.
3/ Separate samples may be used. Subgroup 1 may be performed simultaneously.
4/ Not required for laser marked devices.

* TABLE II. Group E inspection (all quality levels) - for qualification or re-qualification only.

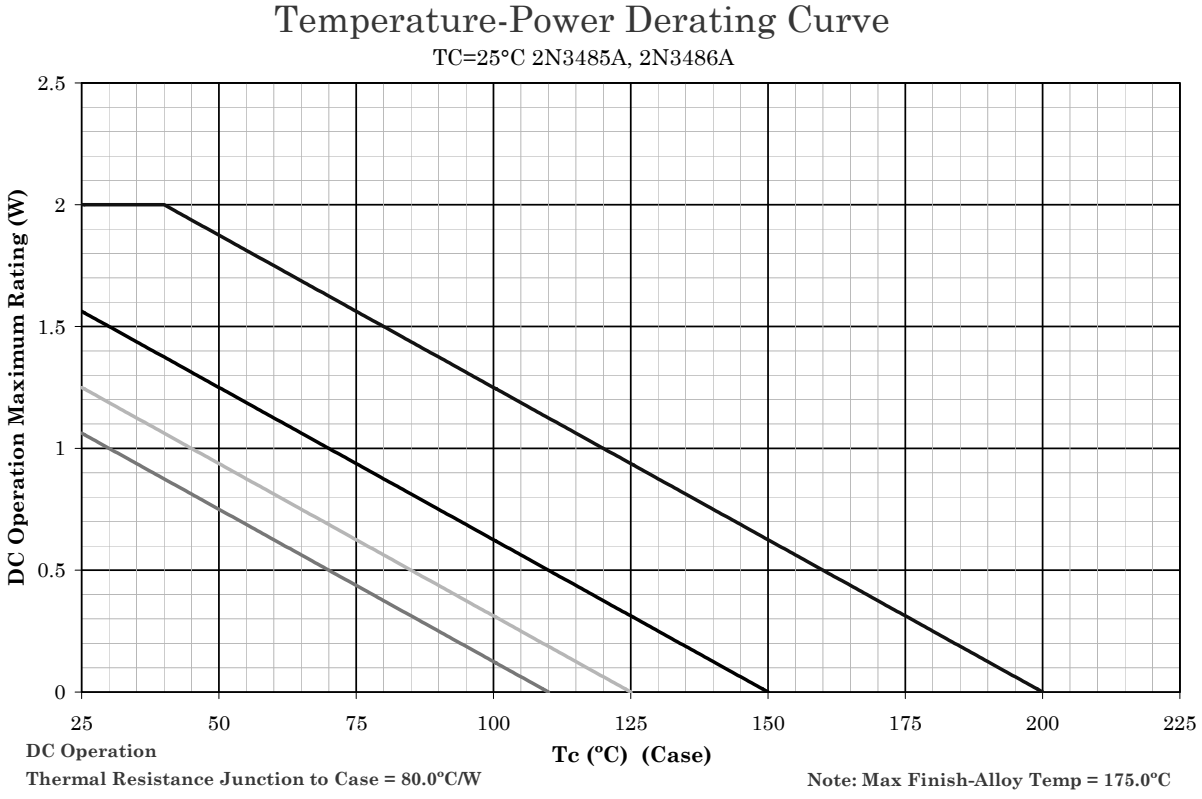
Inspection	MIL-STD-750		Qualification
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles.	
Hermetic seal			
Fine leak Gross leak	1071		
Electrical measurements		See table I, subgroup 2 and 4.5.2 herein.	
Subgroup 2			45 devices c = 0
Intermittent life	1037	Intermittent operation life : V_{CB} = 10 V dc, 6,000 cycles. Adjust device current, or power, to achieve a minimum ΔT_J of +100°C.	
Electrical measurements		See table I, subgroup 2 and 4.5.2 herein.	
Subgroup 4			
Thermal impedance curves		See MIL-PRF-19500.	Sample size N/A
Subgroup 5			
Not applicable			
Subgroup 6			3 devices c= 0
ESD	1020		
Subgroup 8			45 devices c = 0
Reverse stability	1033	Condition B.	



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq$, 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

* FIGURE 2. Derating for 2N3485A, and 2N3486A ($R_{\theta JA}$) (TO-46).

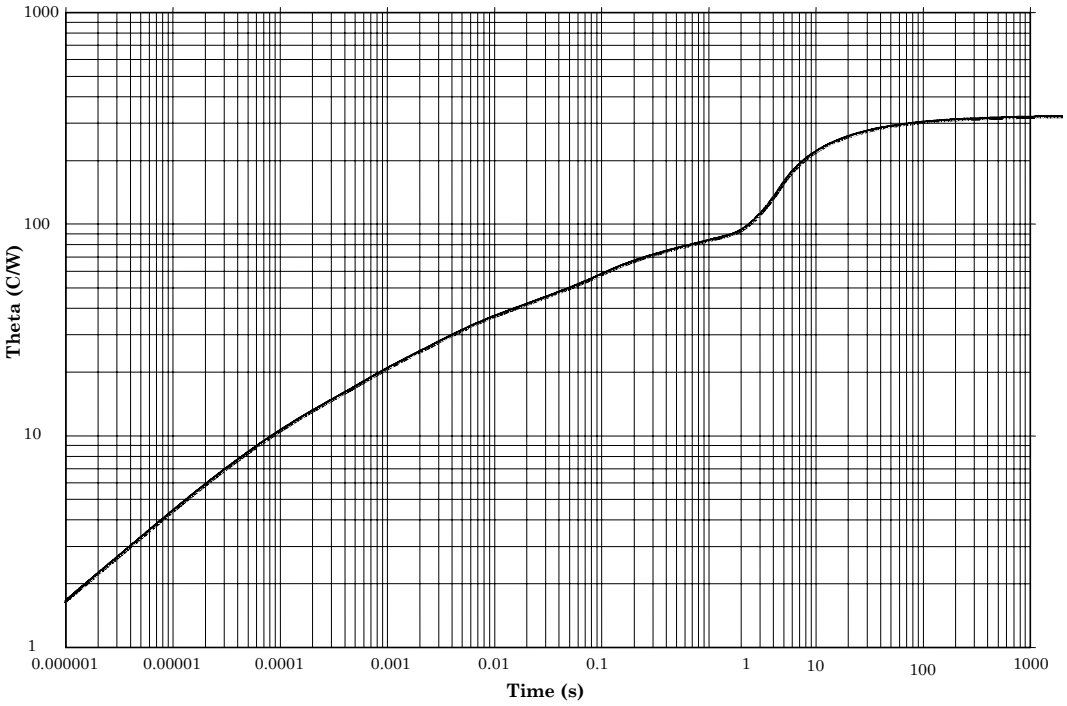


NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq$, 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

* FIGURE 3. Derating for 2N3485A, and 2N3486A ($R_{\theta JC}$) (TO-46).

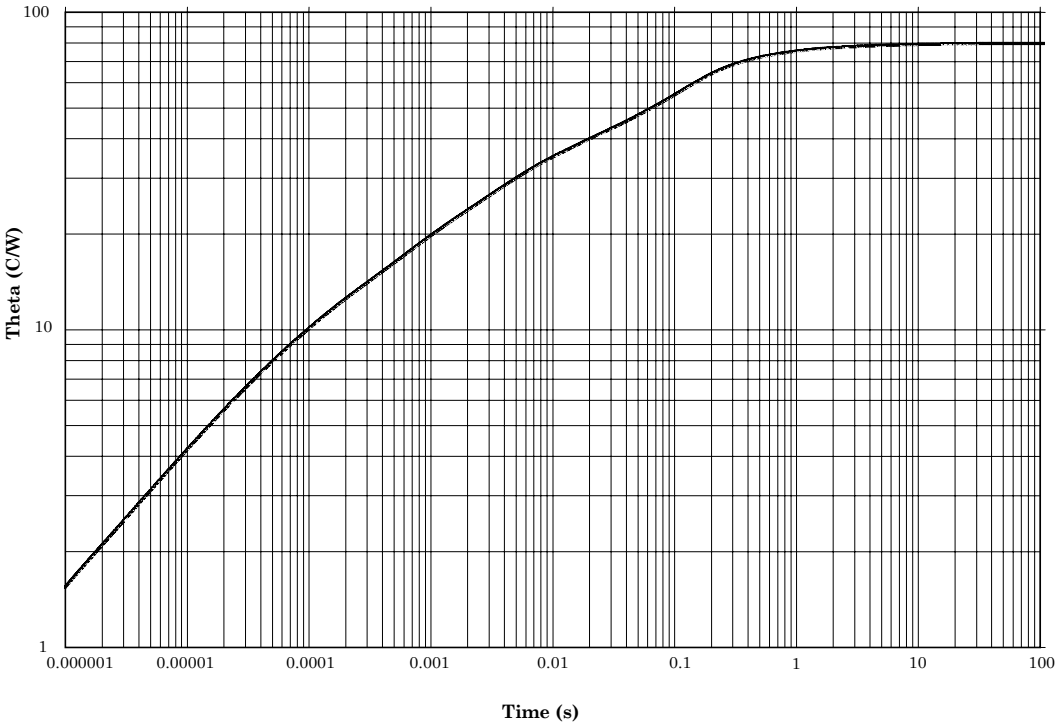
Maximum Thermal Impedance



T_A = +25°C at Pdiss = 500mW (Thermal Resistance $R_{\theta JA}$ = 325°C/W at 500mW)

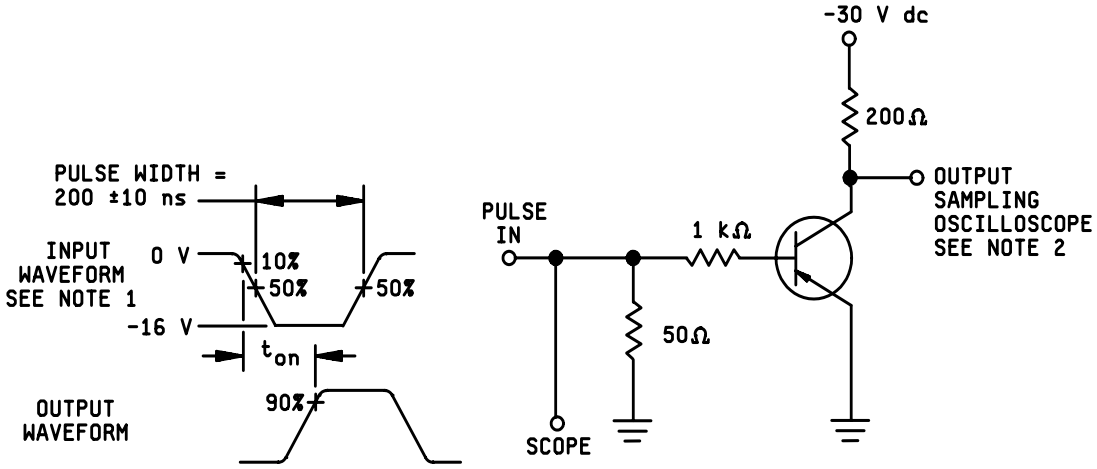
FIGURE 4. Thermal impedance graph ($R_{\theta JA}$) for 2N3485A, and 2N3486A (TO-46).

Maximum Thermal Impedance



Tc = +25°C. thermal resistance $R_{\theta JC}$ = 80C/W at Tc +25°C.

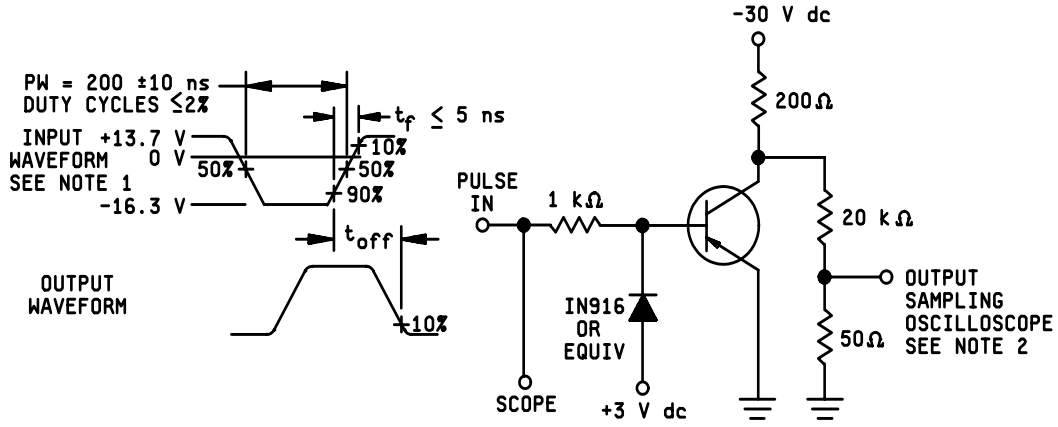
FIGURE 5. Thermal impedance graph ($R_{\theta JC}$) for 2N3485A, and 2N3486A (TO-46).



NOTES:

1. The rise time (t_r) and fall time (t_f) of the applied pulse shall be ≤ 2.0 ns; duty cycle ≤ 2 percent; generator source impedance shall be 50 ohms.
2. Output sampling oscilloscope: $Z_{in} \geq 100$ kΩ; $C_{in} \leq$ RPF; rise time ≤ 0.2 ns.

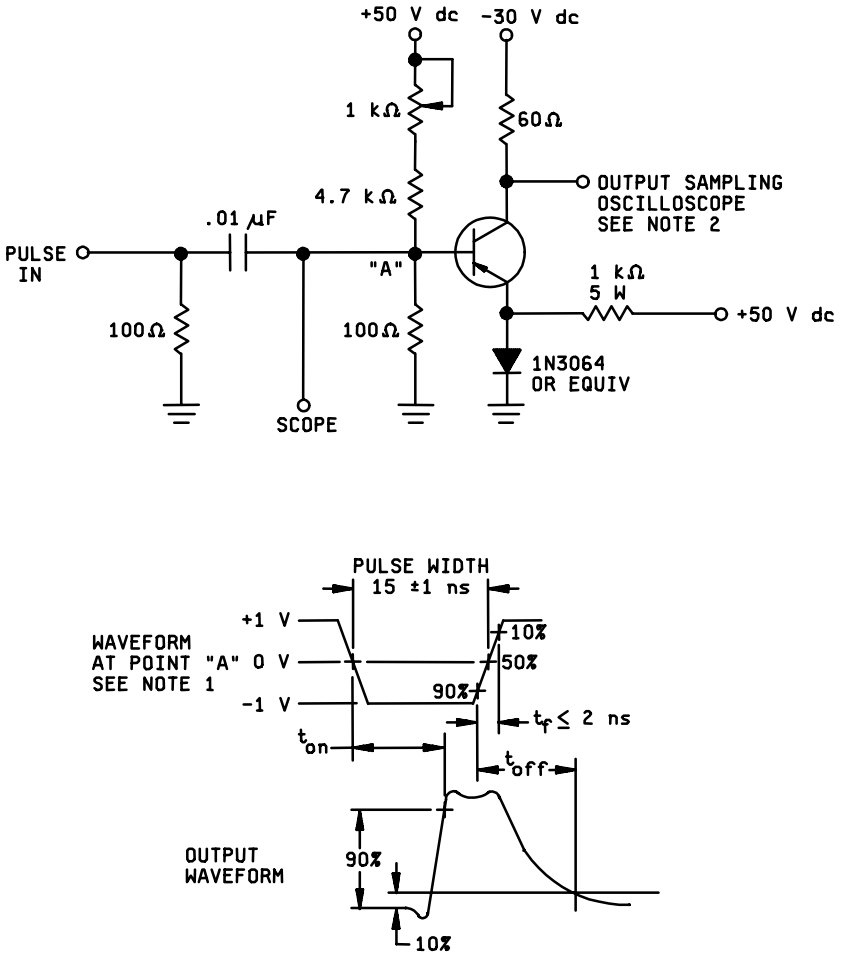
FIGURE 6. Saturated turn-on switching time test circuit.



NOTES:

1. The rise time (t_r) and fall time (t_f) of the applied pulse shall be ≤ 2.0 ns; duty cycle ≤ 2 percent; generator source impedance shall be 50 ohms.
2. Output sampling oscilloscope: $Z_{in} \geq 100$ kΩ; $C_{in} \leq$ RPF; rise time ≤ 0.2 ns.

FIGURE 7. Saturated turn-off switching time test circuit.



NOTES:

1. The rise time (t_r) and fall time (t_f) of the applied pulse shall be ≤ 2.0 ns; duty cycle ≤ 2 percent; generator source impedance shall be 50 ohms.
2. Output sampling oscilloscope: $Z_{in} \geq 100$ kΩ; $C_{in} \leq$ RPF; rise time ≤ 0.2 ns.

FIGURE 8. Nonsaturated turn-on switching time test circuit.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The notes specified in MIL-PRF-19500 are applicable to this specification.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. Product assurance level and type designator.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil.

6.4 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 11
DLA - CC

Review activities:
Army - AV, MI, SM
Navy - AS, MC
Air Force - 19, 71, 99

Preparing activity:
DLA - CC

(Project 5961-2006-042)

* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at http://assist.daps.dla.mil .