Preliminary

3.3V LVPECL 1:4 Clock Fanout Buffer AK8181E

Features

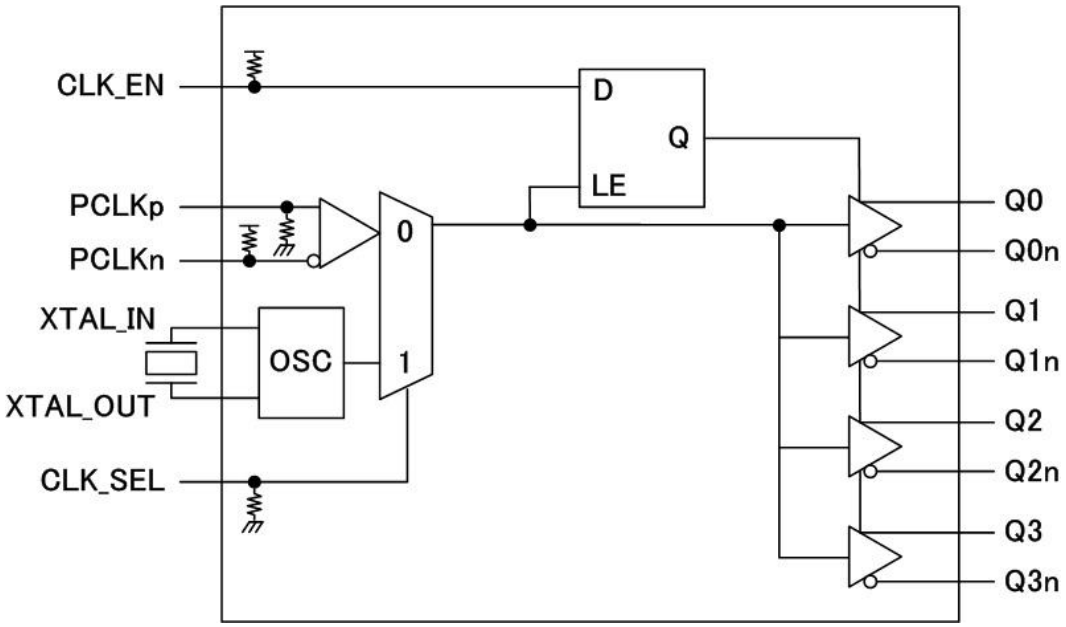
- Four differential 3.3V LVPECL outputs
- Selectable crystal or differential clock inputs
- Clock output frequency up to 650MHz
- Translates any single-ended input signal to 3.3V LVPECL levels with resistor bias on PCLKn input
- Output skew : 10ps (typical)
- Part-to-part skew : 150ps (maximum)
- Propagation delay : 0.9ns (typical)
- Additive phase jitter(RMS):
  PCLKp/n@156.25MHz : 0.04ps (typical)
  XTAL@50MHz : 0.14ps (typical)
- Operating Temperature Range: -40 to +85℃
- Package: 20-pin TSSOP (Pb free)
- Pin compatible with ICS8533I-31

Description

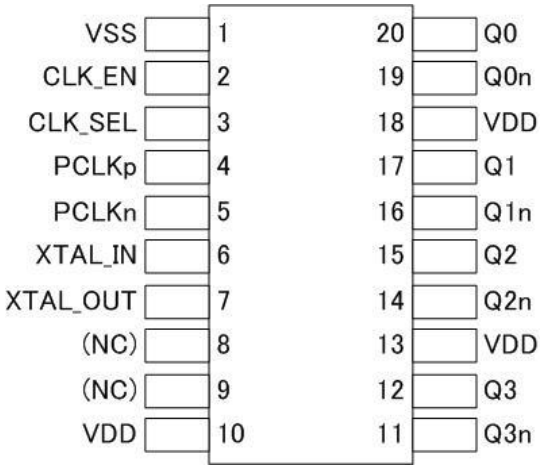
The AK8181E is a member of AKM's LVPECL clock fanout buffer family designed for telecom, networking and computer applications, requiring a range of clocks with high performance and low skew. The AK8181E distributes 4 buffered clocks.

AK8181E are derived from AKM's long-term-experienced clock device technology, and enable clock output to perform low skew. The AK8181E is available in a 20-pin TSSOP package.

Block Diagram



Pin Descriptions



Package: 20-Pin TSSOP(Top View)

Pin No.	Pin Name	Pin Type	Pullup Down	Description
1	VSS	PWR	---	Negative power supply
2	CLK_EN	IN	Pull up	Synchronizing clock output enable (LVCMOS/LVTTL) Pin is connected to VDD by internal resistor. (typ. 51kΩ) High(Open): clock outputs follow clock input. Low: Q outputs are forced low, Qn outputs are forced high.
3	CLK_SEL	IN	Pull down	CLK Select Input (LVCMOS/LVTTL) Pin is connected to VSS by internal resistor. (typ. 51kΩ) High: selects XTAL inputs Low(Open): selects PCLKp/n inputs
4	PCLKp	IN	Pull down	Non-inverting differential clock input Pin is connected to VSS by internal resistor. (typ. 51kΩ)
5	PCLKn	IN	Pull up	Inverting differential clock input Pin is connected to VDD by internal resistor. (typ. 51kΩ)
6	XTAL_IN	IN	---	Crystal oscillator interface
7	XTAL_OUT	IN	---	Crystal oscillator interface
8,	NC	--	---	No connect
9	NC	--	---	No connect
10	VDD	PWR	---	Positive power supply
11, 12	Q3n, Q3	OUT	---	Differential clock output (LVPECL)
13	VDD	PWR	---	Power supply
14, 15	Q2n, Q2	OUT	---	Differential clock output (LVPECL)
16, 17	Q1n, Q1	OUT	---	Differential clock output (LVPECL)
18	VDD	PWR	---	Positive power supply
19, 20	Q0n, Q0	OUT	---	Differential clock output (LVPECL)

Ordering Information

Part Number	Marking	Shipping Packaging	Package	Temperature Range
AK8181E	AK8181E	Tape and Reel	20-pin TSSOP	-40 to 85 °C

Absolute Maximum Rating

Over operating free-air temperature range unless otherwise noted (1)

Items	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3 to 4.6	V
Input voltage	Vin	VSS-0.5 to VDD+0.5	V
Input current (any pins except supplies)	I_{IN}	±10	mA
Storage temperature	Tstg	-55 to 150	°C

Note

(1) Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

(2) VSS=0V

ESD Sensitive Device

This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKM recommends that this device is handled with appropriate precautions.

Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating temperature	Ta		-40		85	°C
Supply voltage (1)	VDD	VDD±5%	3.135	3.3	3.465	V

(1) Power of 3.3V requires to be supplied from a single source. A decoupling capacitor of 0.1μF for power supply line should be located close to each VDD pin.

Pin Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{IN}			4		pF
Input Pullup Resistor	R_{PU}			51		kΩ
Input Pulldown Resistor	R_{PD}			51		kΩ

Power Supply Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Supply Current	I_{DD}	PCLKp/n = input 650MHz XTAL = open		32		mA
		XTAL = input 50MHz PCLKp/n = open		35		mA

DC Characteristics (LVCMOS/LVTTL)

All specifications at VDD= 3.3V±5%, Ta: -40 to +85℃, unless otherwise noted

Parameter		Symbol	Conditions	MIN	TYP	MAX	Unit
Input High Voltage		V_{IH}		2.0		VDD+0.3	V
Input Low Voltage		V_{IL}		-0.3		0.8	V
Input High Current	CLK_SEL	I_H	Vin=VDD=3.465V			150	µA
	CLK_EN		Vin=VDD=3.465V			5	µA
Input Low Current	CLK_SEL	I_L	Vin=VSS, VDD=3.465V	-5			µA
	CLK_EN		Vin=VSS, VDD=3.465V	-150			µA

DC Characteristics (Differential)

All specifications at VDD= 3.3V±5%, Ta: -40 to +85℃, unless otherwise noted

Parameter		Symbol	Conditions	MIN	TYP	MAX	Unit
Input High Current	PCLKp	I_H	Vin=VDD=3.465V			150	µA
	PCLKn		Vin=VDD=3.465V			5	µA
Input Low Current	PCLKp	I_L	Vin=VSS, VDD=3.465V	-5			µA
	PCLKn		Vin=VSS, VDD=3.465V	-150			µA
Peak-to-Peak Input Voltage		V_{PP}		0.15		1.3	V
Common Mode Input Voltage (1) (2)		V_{CMR}		VSS+0.5		VDD-0.85	V

(1) For single ended applications, the maximum input voltage for PCLKp and PCLKn is VDD+0.3V.

(2) Common mode voltage is defined as V_{IH}.

DC Characteristics (LVPECL)

All specifications at VDD= 3.3V±5%, Ta: -40 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output High Voltage (3)	V_{OH}		VDD-1.4		VDD-0.9	V
Output Low Voltage (3)	V_{OL}		VDD-2.0		VDD-1.7	V
Peak-to-Peak Output Voltage Swing	V_{SWING}		0.6		1.0	V

(3) Outputs terminated with 50Ω to VDD-2V.

AC Characteristics

All specifications at VDD= 3.3V±5%, Ta: -40 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output Frequency	f_{OUT}				650	MHz
Propagation Delay (1)	t_{PD}			0.9		ns
Output Skew (2) (3)	$t_{sk(O)}$			10		ps
Part-to-Part Skew (3) (4)	t_{skPP}				150	ps
Buffer Additive Jitter, RMS (5)	t_{jit}	PCLKp/n 156.25MHz (12kHz – 20MHz)		0.04		ps
		XTAL 50MHz (12kHz – 20MHz)		0.14		ps
Output Rise/Fall Time (5)	t_r, t_f	20% to 80%	200		600	ps
Output Duty Cycle	DC_{OUT}	PCLKp/n		50		%

All parameters measured at f ≤ 650MHz unless noted otherwise.

The cycle to cycle jitter on the input will equal the jitter on the output. The part does not add jitter.

(1) Measured from the differential input crossing point to the differential output crossing point.

(2) Defined as skew between outputs at the same supply voltage and with equal load conditions.

(3) This parameter is defined in accordance with JEDEC Standard 65.

(4) Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

(5) Design Value

Crystal Characteristics

All specifications at VDD= 3.3V±5%, VSS=0V, Ta: -40 to +85°C, unless otherwise noted

Parameter	Conditions	MIN	TYP	MAX	Unit
Mode of Oscillation		Fundamental			
Frequency		12		50	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

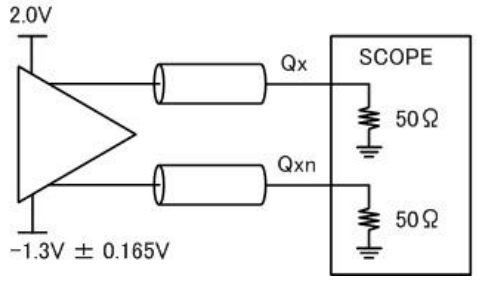


Figure 1 3.3V Output Load Test Circuit

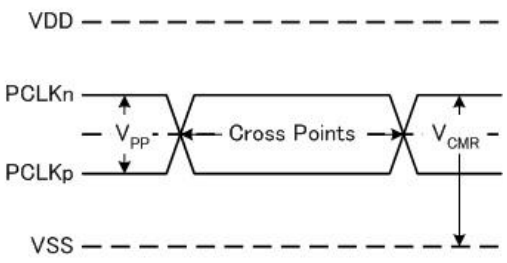


Figure 2 Differential Input Level

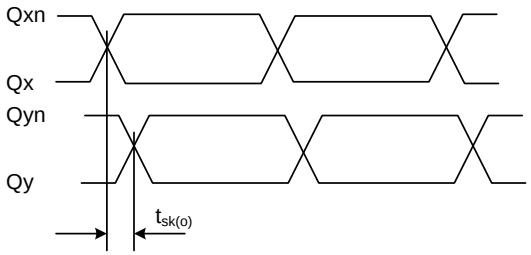


Figure 3 Output Skew

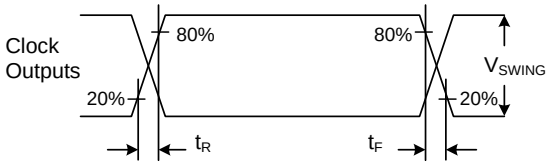


Figure 4 Output Rise/Fall Time

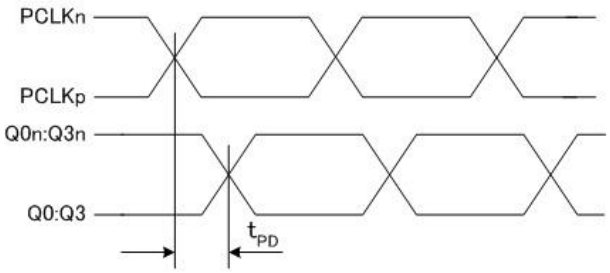


Figure 5 Propagation Delay

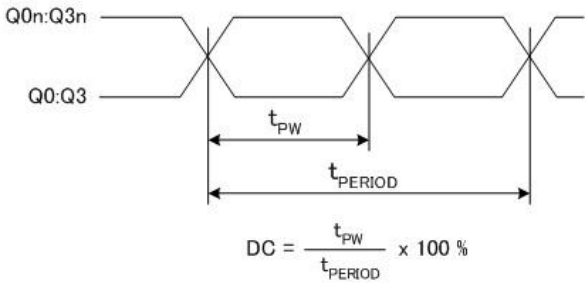


Figure 6 Output Duty/ Pulse Width/ Period

Function Table

The following table shows the inputs/outputs clock state configured through the control pins.

Table 1: Control Input Function Table

Inputs			Outputs	
CLK_EN	**CLK_SEL**	**Selected Source**	**Q0:Q3**	**Q0n:Q3n**
0	0 (Open)	PCLKp/n	Disabled: Low	Disabled: High
0	1	XTAL	Disabled: Low	Disabled: High
1 (Open)	0 (Open)	PCLKp/n	Enabled	Enabled
1 (Open)	1	XTAL	Enabled	Enabled

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock or crystal oscillator edge as shown in Figure 7. In the active mode, the state of the outputs are a function of the PCLKp/n and XTAL inputs as described in Table 2.

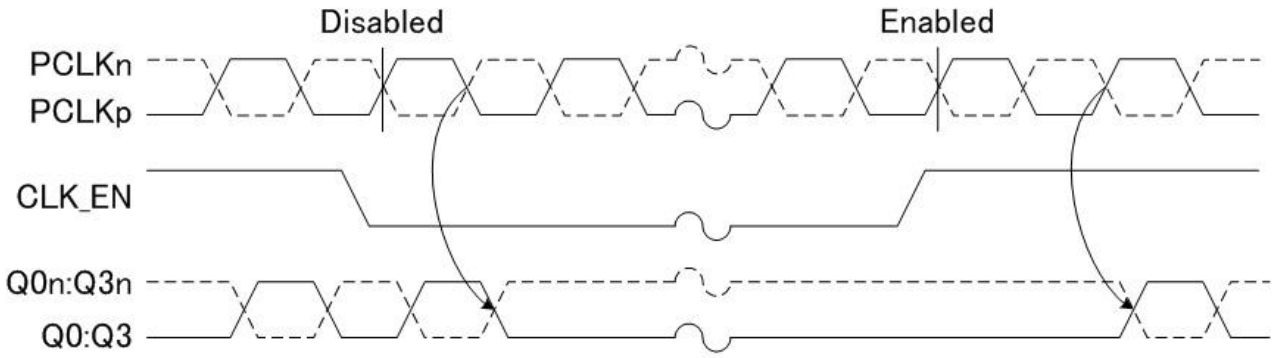


Figure 7 CLK_EN Timing Diagram

Table 2 Clock Input Function Table

Inputs		Outputs		Input to Output	Polarity
PCLKp	**PCLKn**	**Q0:Q3**	**Q0n:Q3n**		
0	1	Low	High	Differential to Differential	Non Inverting
1	0	High	Low	Differential to Differential	Non Inverting
0	Biased (1)	Low	High	Single Ended to Differential	Non Inverting
1	Biased (1)	High	Low	Single Ended to Differential	Non Inverting
Biased (1)	0	High	Low	Single Ended to Differential	Inverting
Biased (1)	1	Low	High	Single Ended to Differential	Inverting

(1) Please refer to the application Information section, “Wiring the Differential Input to Accept Single Ended Levels”.

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure.8 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = VDD/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and VDD = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

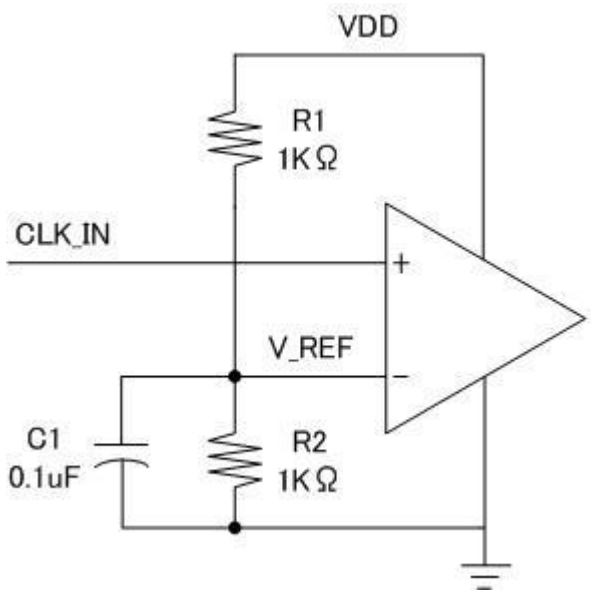
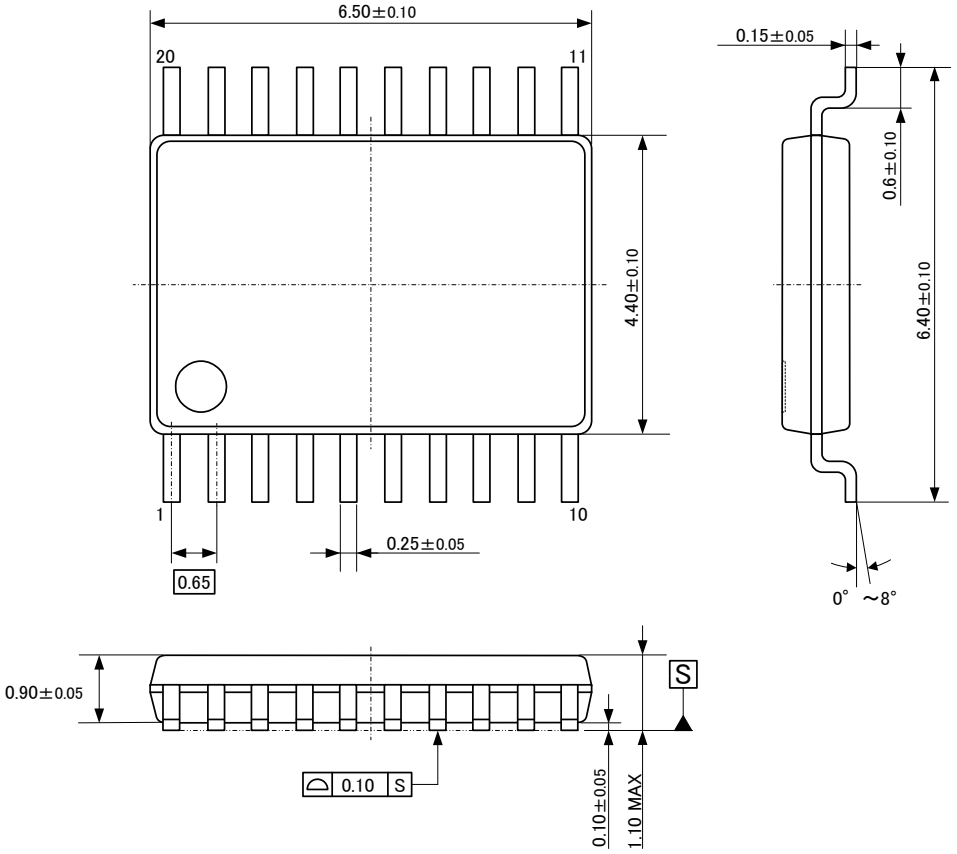


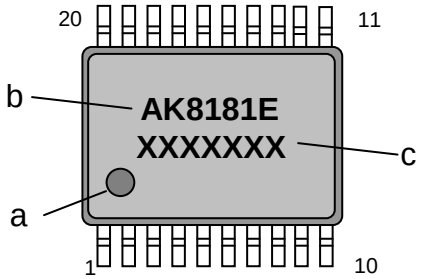
Figure 8 Single Ended Signal Driving Differential Input

Package Information

- **Mechanical data : 20pin TSSOP**

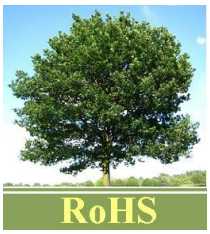


- **Marking**



a: #1 Pin Index
b: Part number
c: Date code (7 digits)

- **RoHS Compliance**



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(*) RoHS compliant products from AKM are identified with “Pb free” letter indication on product label posted on the anti-shield bag and boxes.

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