ProASIC3L Low Power Flash FPGAs with Flash*Freeze Technology

INTRODUCTION

The ProASIC3L family of Microchip flash FPGAs dramatically reduces dynamic power consumption by 40% and static power by 50% compared to the equivalent ProASIC3 device. These power savings are coupled with performance, density, true single-chip, 1.2 V to 1.5 V core and I/O operation as low as 1.2 V, reprogrammability, and advanced features.

Using Microchip's proven Flash*Freeze technology enables users to shut off dynamic power instantaneously and switch the device to static mode without the need to switch off clocks or power supplies while retaining internal states of the device. This greatly simplifies power management on a board done through I/Os and clocks. In addition, optimized software tools using power-driven layout provide instant push-button power reduction.

Nonvolatile flash technology gives ProASIC3L devices the advantage of being a secure, low-power, single-chip solution that is Instant On. ProASIC3L offers dramatic dynamic power savings giving the FPGA users flexibility to combine low power with high performance.

These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

ProASIC3L devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry (CCC) based on an integrated phase-locked loop (PLL). ProASIC3L devices support devices from 250 k system gates to 3 million system gates with up to 504 kbits of true dual-port SRAM and 620 user I/Os.

M1 ProASIC3L devices support the high-performance, 32-bit Cortex-M1 processor developed by ARM for implementation in FPGAs. ARM Cortex-M1 is a soft processor that is fully implemented in the FPGA fabric. It has a three-stage pipeline that offers a good balance between low-power consumption and speed when implemented in an M1 ProASIC3L device. The processor runs the ARMv6-M instruction set, has a configurable nested interrupt controller, and can be implemented with or without the debug block. ARM Cortex-M1 is available for free from Microchip for use in M1 ProASIC3L FPGAs.

The ARM-enabled devices have Microchip SoC Products Group ordering numbers that begin with M1 and do not support AES decryption.

FEATURES AND BENEFITS

Low Power

- Dramatic Reduction in Dynamic and Static Power Savings
- 1.2 V to 1.5 V Core and I/O Voltage Support for Low Power
- Low Power Consumption in Flash*Freeze Mode Allows for Instantaneous Entry to / Exit from Low-Power Flash*Freeze Mode
- Supports Single-Voltage System Operation
- Low-Impedance Switches

High Capacity

- 250,000 to 3,000,000 System Gates
- Up to 504 kbits of True Dual-Port SRAM
- Up to 620 User I/Os

Reprogrammable Flash Technology

- 130-nm, 7-Layer Metal (6 Copper), Flash-Based CMOS Process
- Instant On Level 0 Support

- Single-Chip Solution
- Retains Programmed Design when Powered Off

High Performance

- 350 MHz (1.5 V systems) and 250 MHz (1.2 V systems) System Performance
- 3.3 V, 66 MHz, 66-Bit PCI (1.5 V systems) and 66 MHz, 32-Bit PCI (1.2 V systems)

In-System Programming (ISP) and Security

- ISP Using On-Chip 128-Bit Advanced Encryption Standard (AES) Decryption via JTAG (IEEE 1532–compliant)
- FlashLock® to Secure FPGA Contents

High-Performance Routing Hierarchy

- Segmented, Hierarchical Routing and Clock Structure
- High-Performance, Low-Skew Global Network
- Architecture Supports Ultra-High Utilization

Advanced and Pro (Professional) I/Os

- 700 Mbps DDR, LVDS-Capable I/Os
- 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V Mixed-Voltage Operation
- Bank-Selectable I/O Voltages—up to 8 Banks per Chip
- Single-Ended I/O Standards: LVTTL, LVCMOS 3.3 V / 2.5 V / 1.8 V / 1.5 V / 1.2 V, 3.3 V PCI / 3.3 V PCI-X, and LVCMOS 2.5 V / 5.0 V Input
- Differential I/O Standards: LVPECL, LVDS, B-LVDS, and M-LVDS
- Voltage-Referenced I/O Standards: GTL+ 2.5 V / 3.3 V, GTL 2.5 V / 3.3 V, HSTL Class I and II, SSTL2 Class I and II, SSTL3 Class I and II (A3PE3000L only)
- Wide Range Power Supply Voltage Support per JESD8-B, Allowing I/Os to Operate from 2.7 V to 3.6 V
- Wide Range Power Supply Voltage Support per JESD8-12, Allowing I/Os to Operate from 1.14 V to 1.575 V
- I/O Registers on Input, Output, and Enable Paths
- Hot-Swappable and Cold-Sparing I/Os Programmable Output Slew Rate and Drive Strength
- Programmable Input Delay (A3PE3000L only)
- Schmitt Trigger Option on Single-Ended Inputs (A3PE3000L)
- Weak Pull-Up/-Down
- IEEE 1149.1 (JTAG) Boundary Scan Test
- Pin-Compatible Packages across the ProASIC®3L Family (except PQ208)

Clock Conditioning Circuit (CCC) and PLL

- Six CCC Blocks, One with Integrated PLL (ProASIC3L) and All with Integrated PLL (ProASIC3EL)
- Configurable Phase Shift, Multiply/Divide, Delay Capabilities, and External Feedback
- Wide Input Frequency Range 1.5 MHz to 250 MHz (1.2 V systems) and 350 MHz (1.5 V systems))

SRAMs and FIFOs

- Variable-Aspect-Ratio 4,608-Bit RAM Blocks (×1, ×2, ×4, ×9, and ×18 organizations available)
- True Dual-Port SRAM (except ×18)
- 24 SRAM and FIFO Configurations with Synchronous Operation:
  - 250 MHz: For 1.2 V systems
  - 350 MHz: For 1.5 V systems

ARM® Processor Support in ProASIC3L FPGAs

- ARM Cortex™-M1 Soft Processor Available with or without Debug

TABLE 1: PROASIC3 LOW-POWER PRODUCT FAMILY

ProASIC3L Devices	A3P600L	A3P1000L	A3PE3000L
ARM Cortex-M1 Devices [1]	**M1A3P600L**	**M1A3P1000L**	**M1A3PE3000L**
System Gates	600,000	1,000,000	3,000,000
VersaTiles (D-flip-flops)	13,824	24,576	75,264
RAM Kbits (1,024 bits)	108	144	504
4,608-Bit Blocks	24	32	112
FlashROM Kbits	1	1	1
Secure (AES) ISP [2]	Yes	Yes	Yes
Integrated PLL in CCCs [3]	1	1	6
VersaNet Globals	18	18	18
I/O Banks	4	4	8
Maximum User I/Os	235	177	620
Package Pins VQFP PQFP FBGA	 FG144, FG484	 FG144, FG256	 PQ208 [3] FG324, FG484, FG896

Note 1: Refer to the *Cortex-M1* product brief for more information.

2: AES is not available for ARM Cortex-M1 ProASIC3L devices.

3: For the A3PE3000L, the PQ208 package has six CCCs and two PLLs.

I/OS PER PACKAGE[1]

ProASIC3L Low-Power Devices	A3P600L		A3P1000L		A3PE3000L	
ARM Cortex-M1 Devices	M1A3P600L		M1A3P1000L		M1A3PE3000L [2]	
Package	I/O Type					
	Single-Ended I/O [3]	Differential I/O Pairs	Single-Ended I/O [3]	Differential I/O Pairs	Single-Ended I/O [3]	Differential I/O Pairs
VQ100	–	–	–	–	–	–
PQ208	–	–	–	–	147	65
FG144	97	25	97	25		
FG256	–	–	177	44	–	–
FG324	–	–	–	–	221	110
FG484	235	60	–	–	341	168
FG896	–	–	–	–	620	310

Note 1: When considering migrating your design to a lower- or higher-density device, refer to the packaging section of the datasheet to ensure you are complying with design and board migration requirements.

2: ARM Cortex-M1 support is TBD on this device.

3: Each used differential I/O pair reduces the number of single-ended I/Os available by two.

4: FG256 and FG484 are footprint-compatible packages.

5: "G" indicates RoHS-compliant packages. Refer to ProASIC3L Ordering Information for the location of the "G" in the part number.

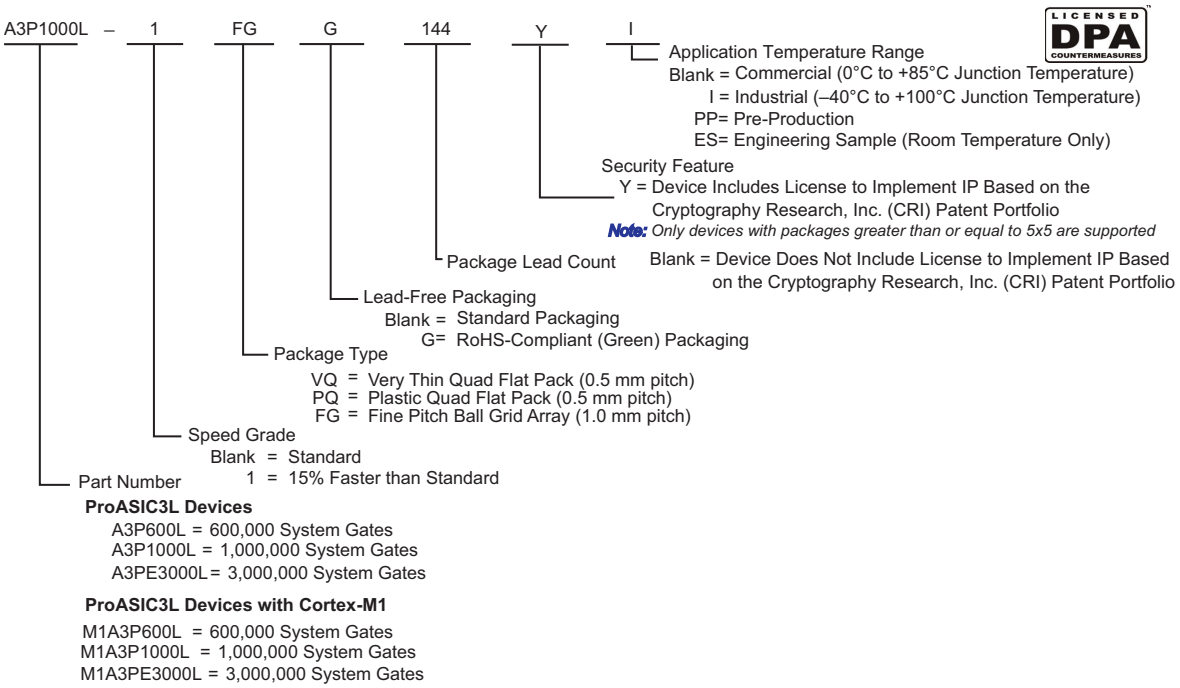
6: For A3PE3000L devices, the usage of certain I/O standards is limited as follows:
– SSTL3(I) and (II): up to 40 I/Os per north or south bank
– LVPECL / GTL+ 3.3 V / GTL 3.3 V: up to 48 I/Os per north or south bank
– SSTL2(I) and (II) / GTL+ 2.5 V/ GTL 2.5 V: up to 72 I/Os per north or south bank

7: When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not as a regular I/O, the number of single-ended user I/Os available is reduced by one.

TABLE 2: PROASIC3L FPGAS PACKAGE SIZES DIMENSIONS

Package	VQ100	PQ208	FG144	FG256	FG324	FG484	FG896
Length × Width (mm\mm)	14 × 14	28 × 28	13 × 13	17 × 17	19 × 19	23 × 23	31 × 31
Nominal Area (mm^2)	196	784	169	289	361	529	961
Pitch (mm)	0.5	0.5	1.0	1.0	1.0	1.0	1.0
Height (mm)	1.00	3.40	1.45	1.60	1.63	2.23	2.23

PROASIC3L ORDERING INFORMATION



TEMPERATURE GRADE OFFERINGS

Package	A3P600L	A3P1000L	A3PE3000L
ARM Cortex-M1 Devices	**M1A3P600L**	**M1A3P1000L**	**M1A3PE3000L**
VQ100	–	–	
PQ208	–	–	C, I
FG144	C, I	C, I	
FG256	–	C, I	
FG324	–	–	C, I
FG484	C, I	–	C, I
FG896	–	–	C, I

Note 1: C = Commercial temperature range: 0°C to 70°C ambient temperature.

2: I = Industrial temperature range: –40°C to 85°C ambient temperature.

SPEED GRADE AND TEMPERATURE GRADE MATRIX

Temperature Grade	Std.	–1
C [1]	3	3
I [2]	3	3

Note 1: C = Commercial temperature range: 0°C to 70°C ambient temperature.

2: I = Industrial temperature range: –40°C to 85°C ambient temperature.

PROASIC3L DEVICE STATUS

ProASIC3L Devices	Status	M1 ProASIC3L Devices	Status
A3P250L	Production	-	-
A3P600L	Production	M1A3P600L	Production
A3P1000L	Production	M1A3P1000L	Production
A3PE3000L	Production	M1A3PE3000L	Production

Contact your local Microchip SoC Products Group representative for device availability:
http://www.microsemi.com/soc/contact/default.aspx

1.0 FEATURES OF PROASIC3L DEVICE FAMILY

The following sections describe important feature of the ProASIC3L Low Power Flash Family Devices.

1.1 Flash*Freeze Technology

The ProASIC3L devices offer Microchip's proven Flash*Freeze technology, which allows instantaneous switching from an active state to a static state. ProASIC3L devices do not need additional components to turn off I/Os or clocks while retaining the design information, SRAM content, and registers. Flash*Freeze technology is combined with in-system programmability, which enables users to quickly and easily upgrade and update their designs in the final stages of manufacturing or in the field. The ability of ProASIC3L devices to support a wide range core voltage (1.2 V to 1.5 V) allows for an even greater reduction in power consumption, which enables low total system power.

When the ProASIC3L device enters Flash*Freeze mode, the device automatically shuts off the clocks and inputs to the FPGA core; when the device exits Flash*Freeze mode, all activity resumes and data is retained.

The availability of low-power modes, combined with a reprogrammable, single-chip, single-voltage solution, make ProASIC3L devices suitable for low-power data transfer and manipulation in portable media, secure communications, radio applications as well as high performance portable, industrial, test, scientific, and medical applications.

1.2 Flash Advantages

1.2.1 LOW POWER

The ProASIC3L family of Microchip flash-based FPGAs provide a low-power advantage, and when coupled with high performance, enables designers to make power-smart choices using a single-chip, reprogrammable, and Instant On device.

ProASIC3L devices offer 40% dynamic power and 50% static power savings compared to the equivalent ProASIC3 device by reducing the core operating voltage to 1.2 V. In addition, the Power Driven Layout (PDL) feature in Libero® System-on-Chip (SoC) offers up to 30% additional power reduction over the standard timing-driven place-and-route (TDPR). With Flash*Freeze technology, ProASIC3L devices are able to retain device SRAM and logic while dynamic power is reduced to a minimum, without the need to stop clock or power supplies. Combining these features provides a low-power, feature-rich and high-performance solution.

1.2.2 SECURITY

Nonvolatile, flash-based ProASIC3L devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. ProASIC3L devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

ProASIC3L devices utilize a 128-bit flash-based lock and a separate AES key to provide the highest level of protection in the FPGA industry for programmed intellectual property and configuration data. In addition, all FlashROM data in ProASIC3L devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. AES was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. ProASIC3L devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. ProASIC3L devices with AES-based security provide a high level of protection for remote field updates over public networks such as the Internet, and are designed to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves.

Security, built into the FPGA fabric, is an inherent component of the ProASIC3L family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The ProASIC3L family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with industry-standard security, making remote ISP possible. A ProASIC3L device provides the best available security for programmable logic designs.

1.2.3 SINGLE CHIP

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based ProASIC3L FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

1.2.4 INSTANT ON

Flash-based ProASIC3L devices support Level 0 of the Instant On classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The Instant On feature of flash-based ProASIC3L devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the ProASIC3L device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based ProASIC3L devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

1.2.5 REDUCED COST OF OWNERSHIP

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, flash-based ProASIC3L devices allow all functionality to be Instant On; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The ProASIC3L family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the ProASIC3L family a cost-effective ASIC replacement solution, manipulation in portable media and secure communications, radio applications as well as high performance portable Industrial, test, scientific and medical applications.

1.2.6 FIRM-ERROR IMMUNITY

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of ProASIC3L flash-based FPGAs. Once it is programmed, the flash cell configuration element of ProASIC3L FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

1.3 Advanced Flash Technology

The ProASIC3L family offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130-nm LVCMOS process with 7 layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

1.4 Advanced Architecture

The proprietary ProASIC3L architecture provides granularity comparable to standard-cell ASICs. The ProASIC3L device consists of five distinct and programmable architectural features (Figure 1-1 and Figure 1-2):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory
- Extensive CCCs and PLLs
- I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the ProASIC3L core tile, as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable, allows for efficient use of the FPGA fabric.

The VersaTile capability is unique to the ProASIC family of third-generation-architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

FIGURE 1-1: PROASIC3L DEVICE ARCHITECTURE OVERVIEW WITH FOUR I/O BANKS (A3P600L, AND A3P1000L)

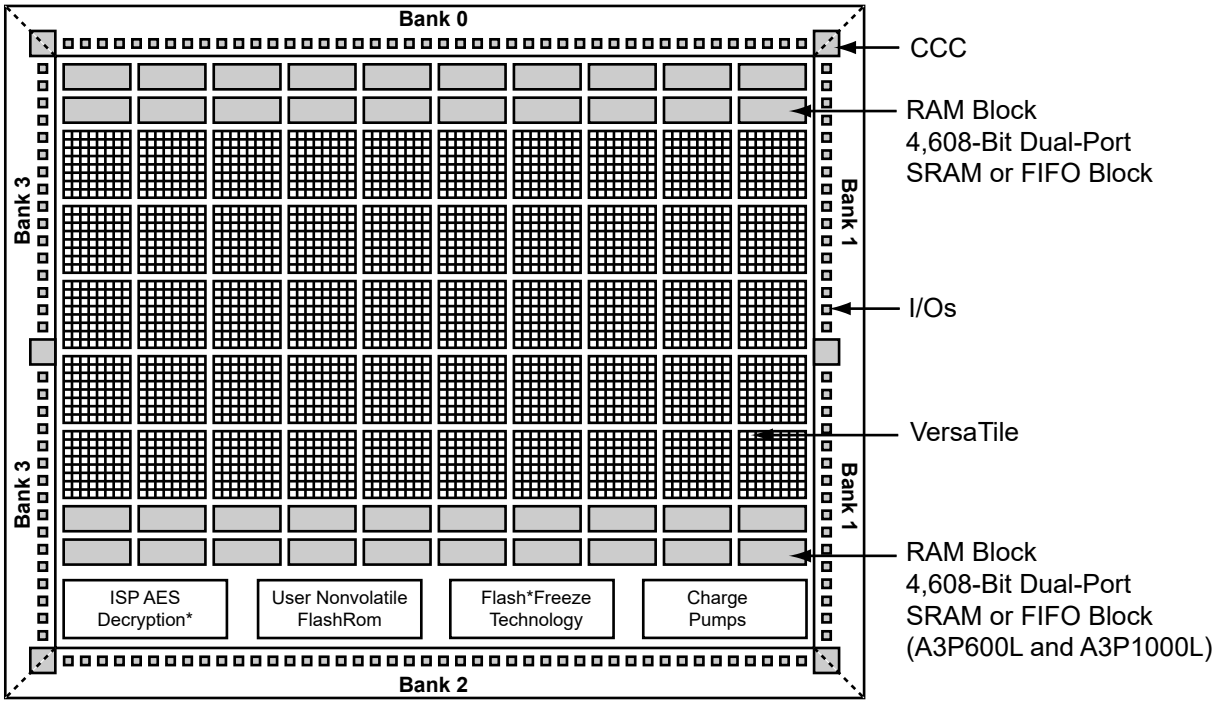
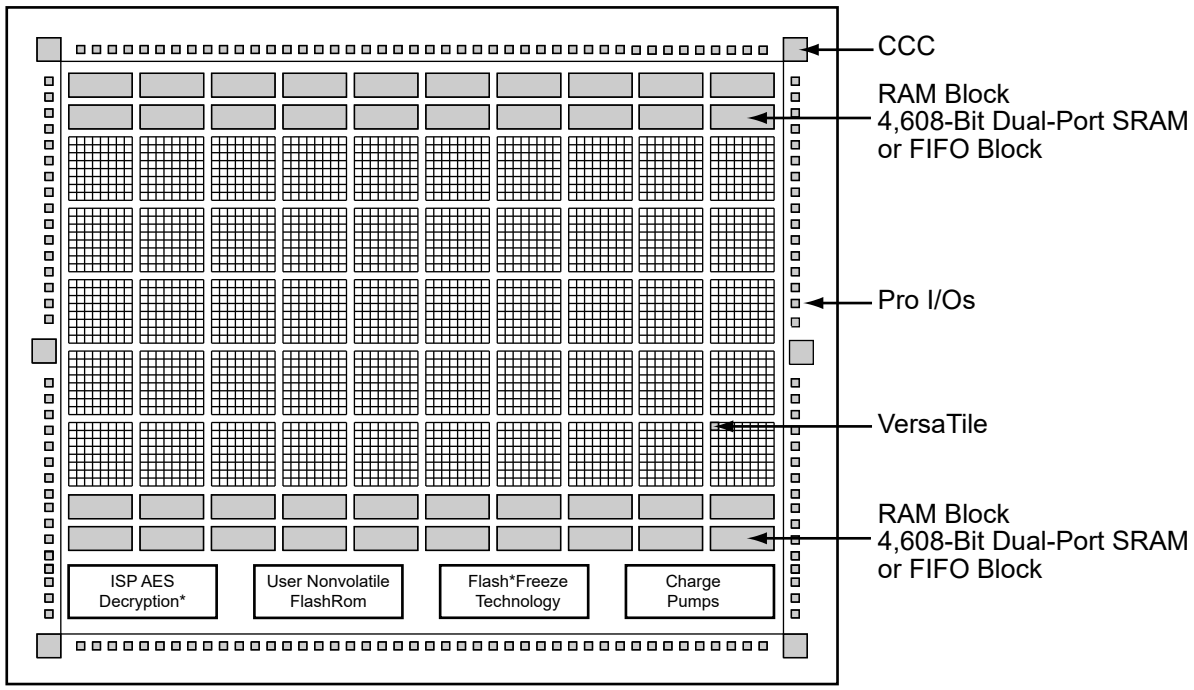


FIGURE 1-2: PROASIC3EL DEVICE ARCHITECTURE OVERVIEW



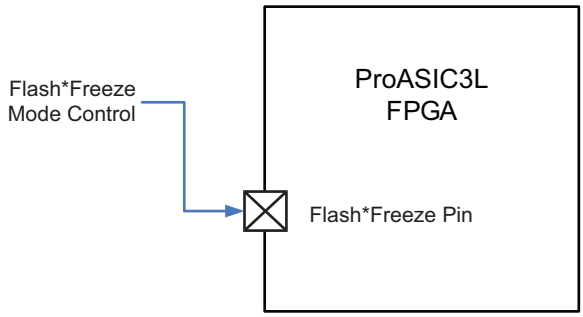
1.5 Flash*Freeze Technology

The ProASIC3L devices offer MicrochipMicrochip's proven Flash*Freeze technology, which enables designers to instantaneously shut off dynamic power consumption while retaining all SRAM and register information. Flash*Freeze technology enables the user to quickly (within 1 µs) enter and exit Flash*Freeze mode by activating the Flash*Freeze (FF) pin while all power supplies are kept at their original values. In addition, I/Os and global I/Os can still be driven and

can be toggling without impact on power consumption; clocks can still be driven or can be toggling without impact on power consumption; and the device retains all core registers, SRAM information, and states. I/O states are tristated during Flash*Freeze mode or can be set to a certain state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLL. Flash*Freeze technology allows the user to switch to active mode on demand, thus simplifying the power management of the device.

The FF pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. It is also possible to use the FF pin as a regular I/O if Flash*Freeze mode usage is not planned, which is advantageous because of the inherent low-power static and dynamic capabilities of the ProASIC3L device. Refer to Figure 1-3 for an illustration of entering/exiting Flash*Freeze mode.

FIGURE 1-3: PROASIC3L FLASH*FREEZE MODE



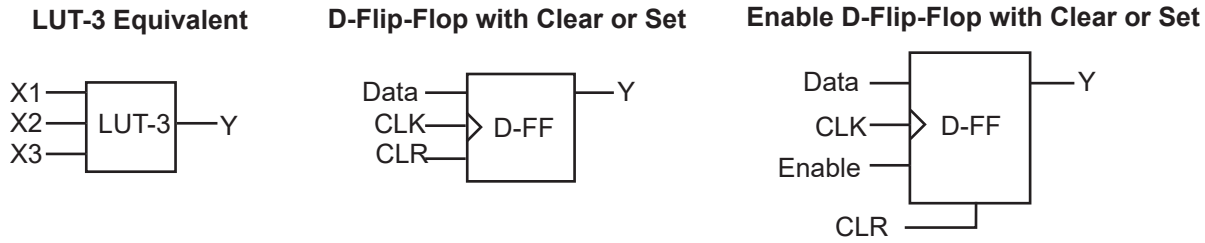
1.5.1 VERSATILES

The ProASIC3L core consists of VersaTiles, which have been enhanced beyond the ProASIC[PLUS]® core tiles. The ProASIC3L VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-4 for VersaTile configurations.

FIGURE 1-4: VERSATILE CONFIGURATIONS



1.5.2 USER NONVOLATILE FLASHROM

ProASIC3L devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet Protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard ProASIC3L IEEE 1532 JTAG programming interface.The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks, as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The ProASIC3L development software solutions, Libero SoC and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

1.5.3 SRAM AND FIFO

ProASIC3L devices have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

1.5.4 PLL AND CCC

ProASIC3L devices provide designers with flexible clock conditioning circuit (CCC) capabilities. Each member of the ProASIC3L family contains six CCCs. One CCC (center west side) has a PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides. One CCC (center west side) has a PLL.

All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz up to 250 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz up to 250 MHz
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration.
- Output duty cycle = 50% ± 1.5% or better
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used
- Maximum acquisition time is 300 µs
- Exceptional tolerance to input period jitter— allowable input jitter is up to 1.5 ns
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × 250 MHz / f_{OUT_CCC}

1.5.5 GLOBAL CLOCKING

ProASIC3L devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

1.5.6 I/OS WITH ADVANCED I/O STANDARDS

The ProASIC3L family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V wide range, and 3.3 V). ProASIC3L FPGAs support different I/O standards, including single-ended, differential, and voltage-referenced (ProASIC3EL only). The I/Os are organized into banks, with two, four, or eight (ProASIC3EL only) banks per device. The configuration of these banks determines the I/O standards supported (Table 1-1). For ProASIC3EL, each I/O bank is subdivided into VREF minibanks, which are used by voltage-referenced I/Os. VREF minibanks contain 8 to 18 I/Os. All the I/Os in a given minibank share a common VREF line. Therefore, if any I/O in a given VREF minibank is configured as a VREF pin, the remaining I/Os in that minibank will be able to use that reference voltage.

***Table 1-1* • I/O Standards Supported**

I/O Bank Type	Device and Bank Location	I/O Standards Supported			
		LVTTL/ LVCMOS	PCI/ PCI-X	LVPECL, LVDS, B-LVDS, M-LVDS	GTL+ 2.5 V/3.3 V, GTL 2.5 V/ 3.3 V, HSTL I and II, SSTL2 I and II, SSTL3 I and II
Pro I/Os	A3PE3000L	3	3	3	3
Advanced I/Os	A3P600L, A3P1000L	3	3	3	Not supported

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-data-rate applications (e.g., PCI 66 MHz, bidirectional SSTL 2 and 3, Class I and II)
- Double-data-Rate applications (e.g., DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications, and DDR 200 MHz SRAM using bidirectional HSTL Class II).

ProASIC3L banks support LVPECL, LVDS, B-LVDS, and M-LVDS. B-LVDS and M-LVDS can support up to 20 loads.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

1.6 Wide Range I/O Support

ProASIC3L devices support JEDEC-defined wide range I/O operation. ProASIC3L devices support both the JESD8-B specification, covering 3 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V, and JESD8-12 with its 1.2 V nominal, supporting an effective operating range of 1.14 V to 1.575 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

1.7 Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User's Guide* for more information.

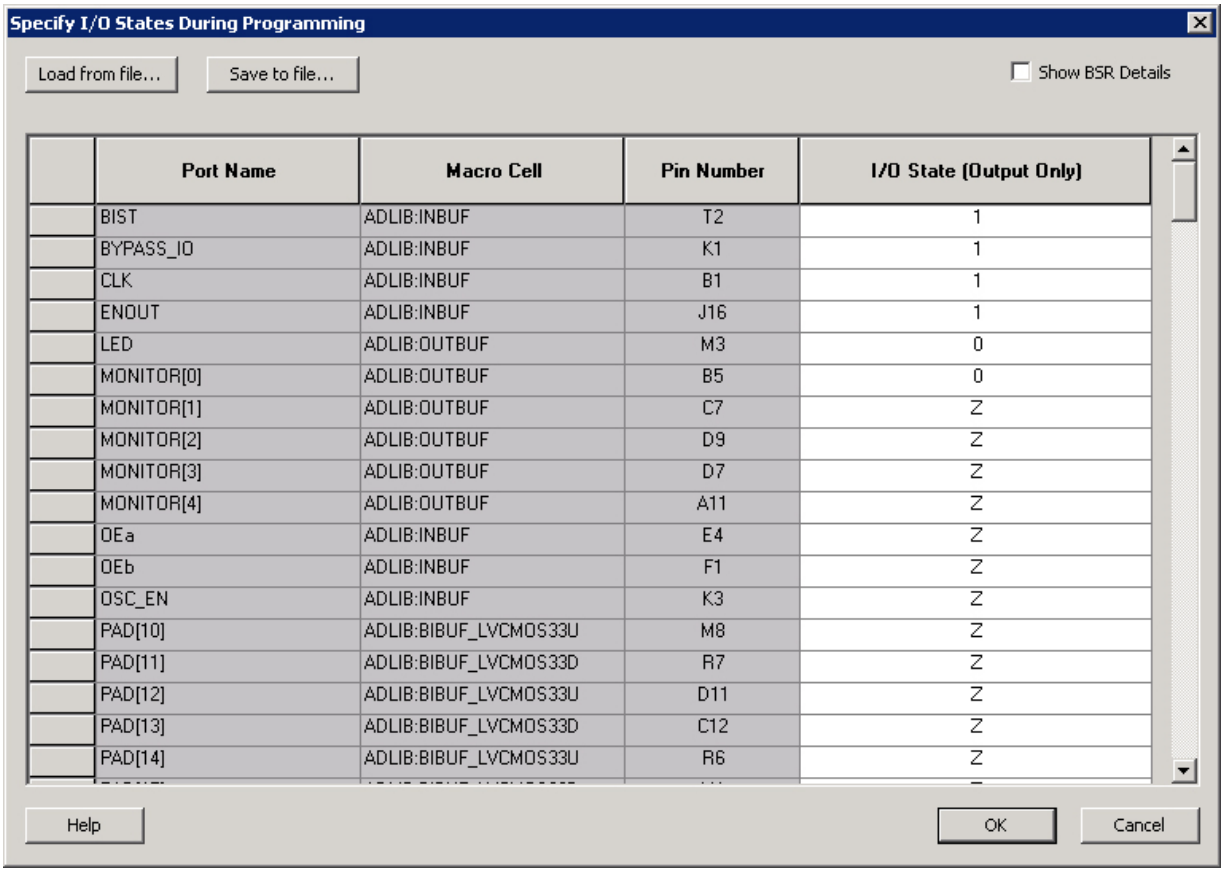
PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the **Specify I/O States During Programming** button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-5).

5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:
   - 1 – I/O is set to drive out logic High
   - 0 – I/O is set to drive out logic Low
   - Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming
   - Z -Tri-State: I/O is tristated
6. Click OK to return to the FlashPoint – Programming File Generator window.

I/O States during programming are saved to the ADB and resulting programming files after completing programming file generation.

FIGURE 1-5: I/O STATES DURING PROGRAMMING WINDOW



2.0 PROASIC3L DC AND SWITCHING CHARACTERISTICS

2.1 General Specifications

2.1.1 OPERATING CONDITIONS

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 is not implied.

TABLE 2-1: ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPUMP	Programming voltage	–0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	–0.3 to 1.65	V
VCCI and VMV [2]	DC I/O buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
T_{STG} [3]	Storage temperature	–65 to +150	°C
T_J [3]	Junction temperature	+125	°C

Note 1: The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-4.

2: VMV pins must be connected to the corresponding VCCI pins. See the section VMVx I/O Supply Voltage (quiet) for further information.

3: For flash programming and retention maximum limits, refer to Table 2-3, and for recommended operating limits, refer to Table 2-2.

TABLE 2-2: RECOMMENDED OPERATING CONDITIONS [1]

Symbol	Parameter		Commercial	Industrial	Units
T_A	Ambient temperature		0 to +70	–40 to +85	°C
T_J	Junction Temperature		0 to + 85	–40 to +100	°C
VCC [2]	1.2 V–1.5 V wide range core voltage [3]		1.14 to 1.575	1.14 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP [5]	Programming voltage	Programming Mode [4]	3.15 to 3.45	3.15 to 3.45	V
		Operation [5]	0 to 3.6	0 to 3.6	V
VCCPLL [6]	Analog power supply (PLL)	1.2 V–1.5 V wide range core voltage [3]	1.14 to 1.575	1.14 to 1.575	V
VCCI and VMV [7]	1.2 V DC supply voltage[8]		1.14 to 1.26	1.14 to 1.26	V
	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V wide range DC supply voltage[9]		2.7 to 3.6	2.7 to 3.6	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V

TABLE 2-2: RECOMMENDED OPERATING CONDITIONS [1]

Symbol	Parameter	Commercial	Industrial	Units

Note 1: All parameters representing voltages are measured with respect to GND unless otherwise specified.

2: The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-14. VCCI should be at the same voltage within a given I/O bank.

3: All ProASIC3L devices must be programmed with the VCC core voltage at 1.5 V.

4: The programming temperature range supported is $T_{ambient}$ = 0°C to 85°C.

5: VPUMP can be left floating during normal operation (not programming mode).

6: VCCPLL pins should be tied to VCC pins. See the section VCCPLA/B/C/D/E/F PLL Supply Voltage for further information.

7: VMV pins must be connected to the corresponding VCCI pins. See the section VMVx I/O Supply Voltage (quiet) for further information.

8: For ProASIC®3L devices, VCCI ≥ VCC.

9: 3.3 V wide range is compliant to the JESD8-A specification and supports 3.0 V VCCI operation.

TABLE 2-3: FLASH PROGRAMMING LIMITS – RETENTION, STORAGE, AND OPERATING TEMPERATURE[1]

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T_{STG} (°C) [2]	Maximum Operating Junction Temperature T_J (°C) [2]
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

Note 1: This is a stress rating only; functional operation at any condition other than those indicated is not implied.

2: These limits apply for program/data retention only. Refer to Table 2-1 and Table 2-2 for device operating conditions and absolute limits.

TABLE 2-4: OVERSHOOT AND UNDERSHOOT LIMITS [1]

VCCI	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Note 1: Based on reliability requirements at junction temperature at 85°C.

2: The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.

3: This table does not provide PCI overshoot/undershoot limits.

2.1.2 I/O POWER-UP AND SUPPLY VOLTAGE THRESHOLDS FOR POWER-ON RESET (COMMERCIAL AND INDUSTRIAL)

Sophisticated power-up management circuitry is designed into every ProASIC3 device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1 and Figure 2-2.

There are five regions to consider during power-up.

ProASIC3 I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points (Figure 2-1 and Figure 2-2).

2. VCCI > VCC – 0.75 V (typical)
3. Chip is in the operating mode.

VCCI **Trip Point:**
Ramping up: 0.6 V < trip_point_up < 1.2 V
Ramping down: 0.5 V < trip_point_down < 1.1 V

VCC **Trip Point:**
Ramping up: 0.6 V < trip_point_up < 1.1 V
Ramping down: 0.5 V < trip_point_down < 1 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

2.1.2.1 PLL Behavior at Brownout Condition

Microchip recommends using monotonic power supplies or voltage regulators to ensure proper powerup behavior. Power ramp-up should be monotonic at least until VCC and VCCPLX exceed brownout activation levels. The VCC activation level is specified as 1.1 V worst-case (see Figure 2-1 and Figure 2-2 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels (0.75 V ± 0.25 V), the PLL output lock signal goes low and/or the output clock is lost. Refer to the "Power-Up/-Down Behavior of Low-Power Flash Devices" chapter of the *ProASIC3L FPGA Fabric User's Guide* for information on clock and lock recovery.

2.1.2.2 Internal Power-Up Activation Sequence

1. Core
2. Input buffers

Output buffers, after 200 ns delay from input buffer activation.

FIGURE 2-1: V5 DEVICES – I/O STATE AS A FUNCTION OF VCCI AND VCC VOLTAGE LEVELS

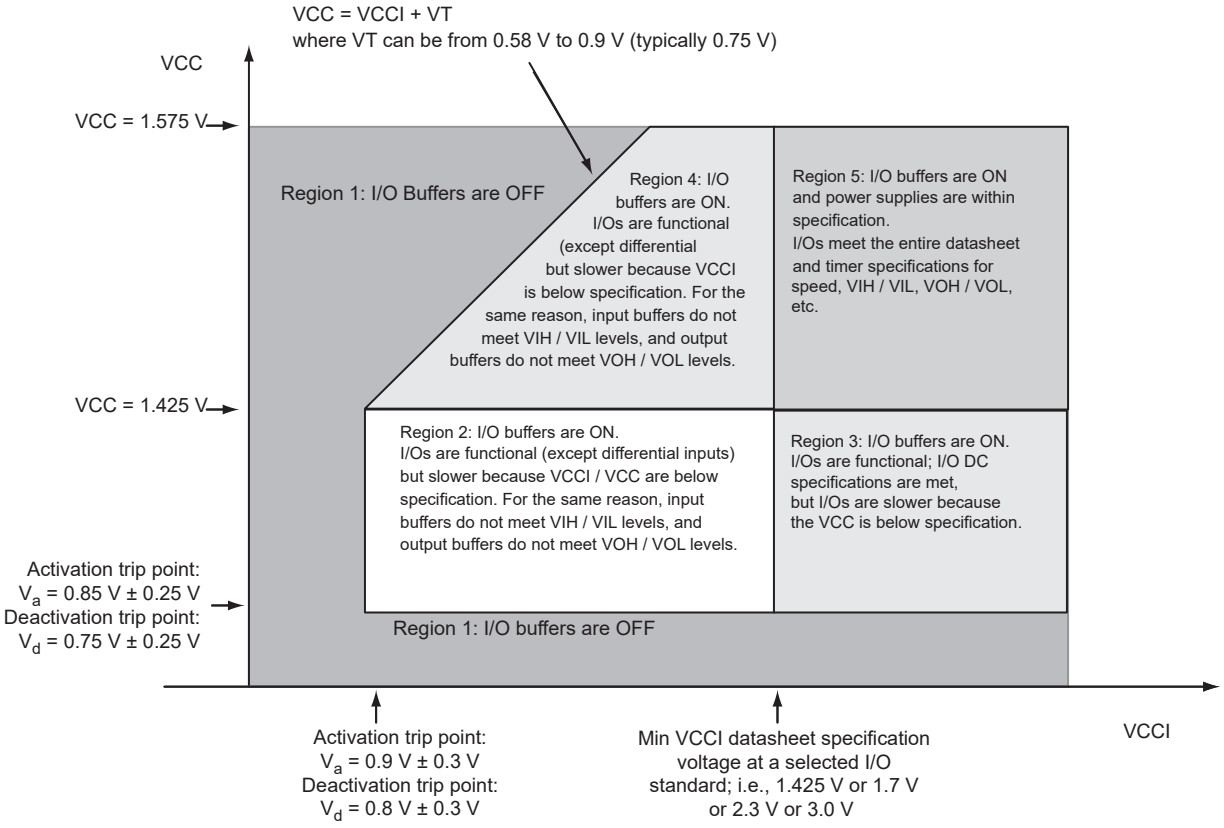
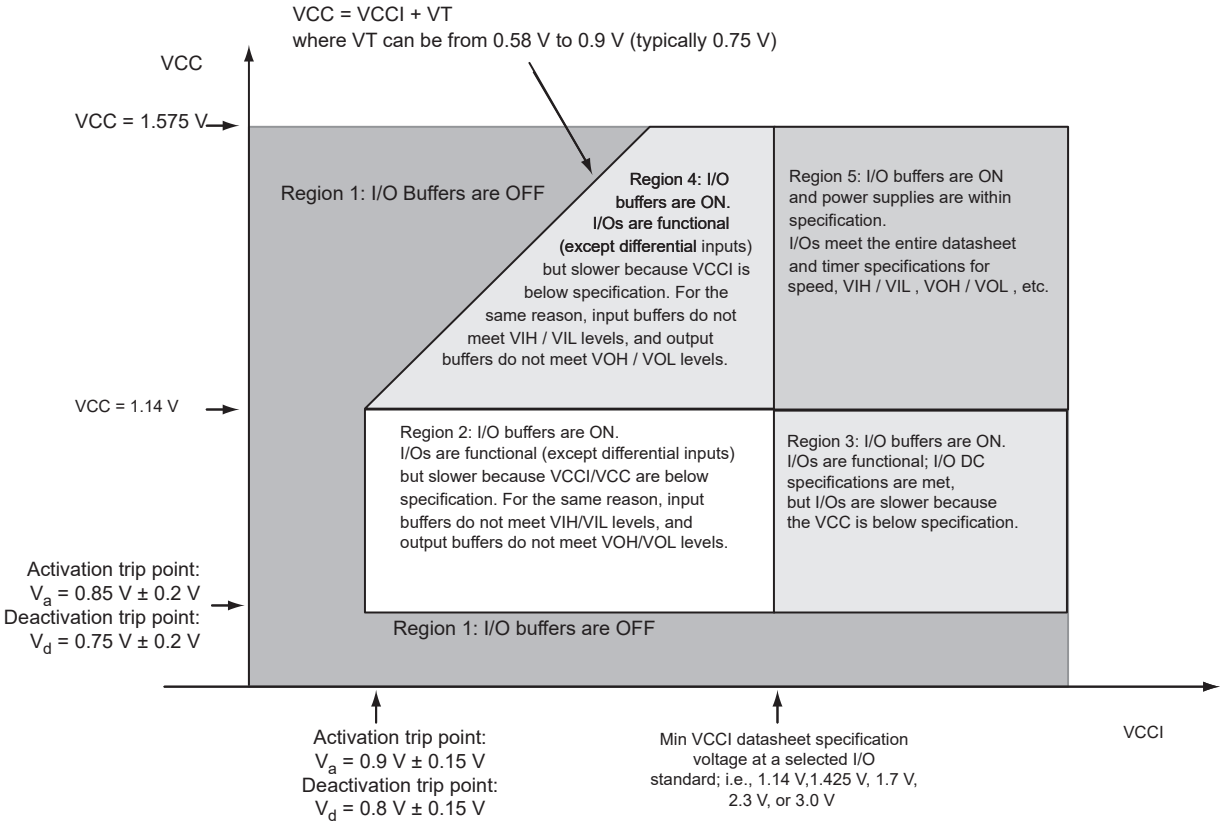


FIGURE 2-2: V5 DEVICES – I/O STATE AS A FUNCTION OF VCCI AND VCC VOLTAGE LEVELS



2.1.3 THERMAL CHARACTERISTICS

2.1.3.1 Introduction

The temperature variable in the Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction temperature to be higher than the ambient temperature.

EQ 1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A$$

EQ 1

where:

T_A = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Table 2-5.

P = Power dissipation

2.1.3.2 Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja}. The thermal characteristics for θ_{ja} are shown for two air flow rates. The absolute maximum junction temperature is 100°C. EQ 2 shows a sample calculation of the absolute maximum power dissipation allowed for a 484-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. } (°C) - \text{Max. ambient temp. } (°C)}{\theta_{ja}(°C/W)} = \frac{100°C - 70°C}{20.5°C/W} = 1.463 \text{ W}$$

EQ 2

TABLE 2-5: PACKAGE THERMAL RESISTIVITIES

Package Type	Device	Pin Count	θ_{jc}	θ_{ja}			Units
				Still Air	200 ft./min.	500 ft./min.	
Very Thin Quad Flat Pack (VQFP)	All devices	100	10.0	35.3	29.4	27.1	C/W
Plastic Quad Flat Pack (PQFP)	All devices	208	8.0	26.1	22.5	20.8	C/W
PQFP with embedded heatspreader	A3P1000L	208	3.8	16.2	13.3	11.9	C/W
Fine Pitch Ball Grid Array (FBGA)	A3P600L	144	8.3	35.8	30.2	28.3	C/W
	A3P1000L	144	6.3	31.6	26.2	24.2	C/W
	A3P1000L	256	6.6	28.1	24.4	22.7	C/W
	AGLE3000	324	TBD	TBD	TBD	TBD	C/W
	A3P600L	484	9.5	27.5	21.9	20.2	C/W
	A3PE3000L	484	4.7	20.6	15.7	14.0	C/W
	A3PE3000L	896	2.4	13.6	10.4	9.4	C/W

2.1.3.3 Temperature and Voltage Derating Factors

TABLE 2-6: TEMPERATURE AND VOLTAGE DERATING FACTORS FOR TIMING DELAYS (NORMALIZED TO T_J = 70°C, VCC = 1.14 V)

Array Voltage VCC (V)	Junction Temperature (°C)					
	–40°C	0°C	25°C	70°C	85°C	110°C
1.14	0.90	0.94	0.96	1.00	1.01	1.03
1.2	0.87	0.90	0.92	0.96	0.97	0.99
1.26	0.83	0.86	0.88	0.92	0.93	0.85
1.3	0.81	0.84	0.86	0.90	0.91	0.93
1.35	0.78	0.81	0.83	0.87	0.88	0.89
1.4	0.75	0.78	0.80	0.83	0.84	0.86
1.425	0.74	0.77	0.78	0.82	0.83	0.85
1.5	0.70	0.72	0.74	0.77	0.79	0.80
1.575	0.67	0.70	0.72	0.75	0.76	0.77

2.2 Calculating Power Dissipation

2.2.1 QUIESCENT SUPPLY CURRENT

Quiescent supply current (I_{DD}) calculation depends on multiple factors, including operating voltages (VCC, VCCI, and VJTAG), operating temperature, system clock frequency, and power mode usage. Microchip recommends using the Power Calculator and SmartPower software estimation tools to evaluate the projected static and active power based on the user design, power mode usage, operating voltage, and temperature.

TABLE 2-7: POWER SUPPLY STATE PER MODE

Modes/Power Supplies	Power Supply Configurations				
	VCC	VCCPLL	VCCI	VJTAG	VPUMP
Flash*Freeze	On	On	On	On	On/off/floating
Sleep	Off	Off	On	Off	Off
Shutdown	Off	Off	Off	Off	Off
No Flash*Freeze	On	On	On	On	On/off/floating

Note: Off: Power Supply level = 0 V

TABLE 2-8: QUIESCENT SUPPLY CURRENT (IDD) CHARACTERISTICS, PROASIC3L FLASH*FREEZE MODE*

	Core Voltage	A3P600L	A3P1000L	A3PE3000L	Units
Typical (25°C)	1.2 V	0.55	0.88	2.75	mA
	1.5 V	0.83	1.33	4.2	mA

Note: * IDD includes VCC, VPUMP, VCCI, VJTAG, and VCCPLL currents.

TABLE 2-9: QUIESCENT SUPPLY CURRENT (IDD) CHARACTERISTICS, PROASIC3L SLEEP MODE*

ICCI Current	Core Voltage	A3P600L	A3P1000L	A3PE3000L	Units
VCCI/VJTAG = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	1.7	µA
VCCI/VJTAG = 1.5 V (per bank) Typical (25°C)	1.2 V/1.5 V	1.8	1.8	1.8	µA
VCCI/VJTAG = 1.8 V (per bank) Typical (25°C)	1.2 V/1.5 V	1.9	1.9	1.9	µA

TABLE 2-9: QUIESCENT SUPPLY CURRENT (IDD) CHARACTERISTICS, PROASIC3L SLEEP MODE*

ICCI Current	Core Voltage	A3P600L	A3P1000L	A3PE3000L	Units
VCCI/VJTAG = 2.5 V (per bank) Typical (25°C)	1.2 V/1.5 V	2.2	2.2	2.2	µA
VCCI/VJTAG = 3.3 V (per bank) Typical (25°C)	1.2 V/1.5 V	2.5	2.5	2.5	µA

*IDD = N_{BANKS} * ICCI

TABLE 2-10: QUIESCENT SUPPLY CURRENT (IDD) CHARACTERISTICS, SHUTDOWN MODE

	Core Voltage	A3PE3000L	Units
Typical (25°C)	1.2 V/1.5 V	0	µA

TABLE 2-11: QUIESCENT SUPPLY CURRENT (IDD) CHARACTERISTICS, NO FLASH*FREEZE MODE[1]

	Core Voltage	A3P600L	A3P1000L	A3PE3000L	Units
ICCA Current[2]					
Typical (25°C)	1.2 V	0.55	0.88	2.75	mA
	1.5 V	0.83	1.33	4.2	mA
ICCI or IJTAG Current					
VCCI/VJTAG = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	1.7	µA
VCCI/VJTAG = 1.5 V (per bank) Typical (25°C)	1.2 V/1.5 V	1.8	1.8	1.8	µA
VCCI/VJTAG = 1.8 V (per bank) Typical (25°C)	1.2 V/1.5 V	1.9	1.9	1.9	µA
VCCI/VJTAG = 2.5 V (per bank) Typical (25°C)	1.2 V/1.5 V	2.2	2.2	2.2	µA
VCCI/VJTAG = 3.3 V (per bank) Typical (25°C)	1.2 V/1.5 V	2.5	2.5	2.5	µA

Note 1: *IDD = N_{BANKS} * ICCI+ICCA. JTAG counts as one bank when powered.

2: Includes VCC and VPUMP and VCCPLL currents.

2.2.2 POWER PER I/O PIN

TABLE 2-12: SUMMARY OF I/O INPUT BUFFER POWER (PER PIN) – DEFAULT I/O SOFTWARE SETTINGS (APPLICABLE TO PRO I/O BANKS)

	VCCI (V)	Static Power PDC6 (mW)[1]	Dynamic Power PAC9 (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL/LVCMOS	3.3	–	16.34
3.3 V LVTTL/LVCMOS – Schmitt trigger	3.3	–	24.49
2.5 V LVCMOS	2.5	–	4.71
2.5 V LVCMOS – Schmitt trigger	2.5	–	6.13
1.8 V LVCMOS	1.8	–	1.66
1.8 V LVCMOS – Schmitt trigger	1.8	–	1.78
1.5 V LVCMOS (JESD8-11)	1.5	–	1.01
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	–	0.97
1.2 V LVCMOS	1.2	–	0.60
1.2 V LVCMOS – Schmitt trigger	1.2	–	0.53
3.3 V PCI	3.3	–	17.76
3.3 V PCI – Schmitt trigger	3.3	–	19.10
3.3 V PCI-X	3.3	–	17.76
3.3 V PCI-X – Schmitt trigger	3.3	–	19.10
Voltage-Referenced			
3.3 V GTL	3.3	2.90	7.07
2.5 V GTL	2.5	2.13	3.62
3.3 V GTL+	3.3	2.81	2.97
2.5 V GTL+	2.5	2.57	2.55
HSTL (I)	1.5	0.17	0.85
HSTL (II)	1.5	0.17	0.85
SSTL2 (I)	2.5	1.38	3.30
SSTL2 (II)	2.5	1.38	3.30
SSTL3 (I)	3.3	3.21	8.08
SSTL3 (II)	3.3	3.21	8.08
Differential			
LVDS	2.5	2.26	0.95
LVPECL	3.3	5.71	1.62

Note 1: PDC6 is the static power (where applicable) measured on VCCI.

2: PAC9 is the total dynamic power measured on VCCI.

TABLE 2-13: SUMMARY OF I/O INPUT BUFFER POWER (PER PIN) – DEFAULT I/O SOFTWARE SETTINGS[1] (APPLICABLE TO ADVANCED I/O BANKS)

	VCCI (V)	Static Power PDC6 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	16.22
2.5 V LVCMOS	2.5	–	4.65
1.8 V LVCMOS	1.8	–	1.65
1.5 V LVCMOS (JESD8-11)	1.5	–	0.98

TABLE 2-13: SUMMARY OF I/O INPUT BUFFER POWER (PER PIN) – DEFAULT I/O SOFTWARE SETTINGS[1] (APPLICABLE TO ADVANCED I/O BANKS)

	VCCI (V)	Static Power PDC6 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
1.2 V LVCMOS	1.2	–	0.61
3.3 V PCI	3.3	–	17.64
3.3 V PCI-X	3.3	–	17.64
Differential			
LVDS	2.5	2.26	0.95
LVPECL	3.3	5.72	1.63

Note 1: Dynamic power consumption is given for standard load and software default drive strength and output slew.

2: P_{DC6} is the static power (where applicable) measured on VCCI.

3: P_{AC10} is the total dynamic power measured on VCCI.

TABLE 2-14: SUMMARY OF I/O INPUT BUFFER POWER (PER PIN) – DEFAULT I/O SOFTWARE SETTINGS (APPLICABLE TO STANDARD PLUS I/O BANKS)

	VCCI (V)	Static Power PDC6 (mW)[1]	Dynamic Power PAC9 (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	16.23
2.5 V LVCMOS	2.5	–	4.66
1.8 V LVCMOS	1.8	–	1.64
1.5 V LVCMOS (JESD8-11)	1.5	–	0.99
1.2 V LVCMOS	1.2	–	0.58
3.3 V PCI	3.3	–	17.64
3.3 V PCI-X	3.3	–	17.64

Note 1: PDC6 is the static power (where applicable) measured on VCCI.

2: PAC9 is the total dynamic power measured on VCCI.

TABLE 2-15: SUMMARY OF I/O OUTPUT BUFFER POWER (PER PIN) – DEFAULT I/O SOFTWARE SETTINGS [1] (APPLICABLE TO PRO I/OS)

	C_{LOAD} (pF)	VCCI (V)	Static Power PDC7 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL/LVCMOS	5	3.3	–	148.00
2.5 V LVCMOS	5	2.5	–	83.23
1.8 V LVCMOS	5	1.8	–	54.58
1.5 V LVCMOS (JESD8-11)	5	1.5	–	37.05
1.2 V LVCMOS	5	1.2	–	17.94
3.3 V PCI	10	3.3	–	204.61
3.3 V PCI-X	10	3.3	–	204.61
Voltage-Referenced				
3.3 V GTL	10	3.3	–	24.08
2.5 V GTL	10	2.5	–	13.52
3.3 V GTL+	10	3.3	–	24.10

TABLE 2-15: SUMMARY OF I/O OUTPUT BUFFER POWER (PER PIN) – DEFAULT I/O SOFTWARE SETTINGS [1] (APPLICABLE TO PRO I/OS)

	C_{LOAD} (pF)	VCCI (V)	Static Power PDC7 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
2.5 V GTL+	10	2.5	–	13.54
HSTL (I)	20	1.5	7.08	26.22
HSTL (II)	20	1.5	13.88	27.22
SSTL2 (I)	30	2.5	16.69	105.56
SSTL2 (II)	30	2.5	25.91	116.60
SSTL3 (I)	30	3.3	26.02	114.87
SSTL3 (II)	30	3.3	42.21	131.76
Differential				
LVDS	–	2.5	7.70	89.62
LVPECL	–	3.3	19.42	168.02

Note 1: Dynamic power consumption is given for standard load and software default drive strength and output slew.

2: PDC7 is the static power (where applicable) measured on VCCI.

3: PAC10 is the total dynamic power measured on VCCI.

TABLE 2-16: SUMMARY OF I/O OUTPUT BUFFER POWER (PER PIN) – DEFAULT I/O SOFTWARE SETTINGS [1] (APPLICABLE TO ADVANCED I/O BANKS)

	C_{LOAD} (pF)	VCCI (V)	Static Power PDC7 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	5	3.3	–	141.97
2.5 V LVCMOS	5	2.5	–	79.98
1.8 V LVCMOS	5	1.8	–	52.26
1.5 V LVCMOS (JESD8-11)	5	1.5	–	35.62
1.2 V LVCMOS	5	1.2	–	21.29
3.3 V PCI	10	3.3	–	201.02
3.3 V PCI-X	10	3.3	–	201.02
Differential				
LVDS	–	2.5	7.74	89.71
LVPECL	–	3.3	19.54	167.54

Note 1: Dynamic power consumption is given for standard load and software default drive strength and output slew.

2: PDC7 is the static power (where applicable) measured on VCCI.

3: PAC10 is the total dynamic power measured on VCCI.

TABLE 2-17: SUMMARY OF I/O OUTPUT BUFFER POWER (PER PIN) – DEFAULT I/O SOFTWARE SETTINGS [1] (Applicable to Standard Plus I/O Banks)

	C_{LOAD} (pF)	VCCI (V)	Static Power PDC7 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	5	3.3	–	125.97
2.5 V LVCMOS	5	2.5	–	70.82
1.8 V LVCMOS	5	1.8	–	36.39

TABLE 2-17: SUMMARY OF I/O OUTPUT BUFFER POWER (PER PIN) – DEFAULT I/O SOFTWARE SETTINGS [1] (Applicable to Standard Plus I/O Banks)

	C_{LOAD} (pF)	VCCI (V)	Static Power PDC7 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
1.5 V LVCMOS (JESD8-11)	5	1.5	–	25.34
1.2 V LVCMOS	5	1.2	–	16.24
3.3 V PCI	10	3.3	–	184.92
3.3 V PCI-X	10	3.3	–	184.92

Note 1: Dynamic power consumption is given for standard load and software default drive strength and output slew.

2: PDC7 is the static power (where applicable) measured on VCCI.

3: PAC10 is the total dynamic power measured on VCCI.

2.2.3 POWER CONSUMPTION OF VARIOUS INTERNAL RESOURCES

TABLE 2-18: DIFFERENT COMPONENTS CONTRIBUTING TO DYNAMIC POWER CONSUMPTION IN PROASIC3L DEVICES AT 1.2 V VCC

Parameter	Definition	Device Specific Dynamic Power (µW/MHz)		
		A3PE3000 L	A3P1000 L	A3P600 L
PAC1	Clock contribution of a Global Rib	12.61	9.28	8.19
PAC2	Clock contribution of a Global Spine	2.66	1.59	1.19
PAC3	Clock contribution of a VersaTile row	0.56	0.52	
PAC4	Clock contribution of a VersaTile used as a sequential module	0.07		
PAC5	First contribution of a VersaTile used as a sequential module	0.05		
PAC6	Second contribution of a VersaTile used as a sequential module	0.19		
PAC7	Contribution of a VersaTile used as a combinatorial Module	0.11		
PAC8	Average contribution of a routing net	0.45		
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-12. through Table 2-14.		
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-15 through Table 2-17.		
PAC11	Average contribution of a RAM block during a read operation	25.00		
PAC12	Average contribution of a RAM block during a write operation	30.00		
PAC13	Dynamic contribution for PLL	1.74		

Note: *For a different output load, drive strength, or slew rate, Microchip recommends using the Microchip power spreadsheet calculator or SmartPower tool in Libero SoC.

TABLE 2-19: DIFFERENT COMPONENTS CONTRIBUTING TO DYNAMIC POWER CONSUMPTION IN PROASIC3L DEVICES AT 1.5 V VCC

Parameter	Definition	Device Specific Dynamic Power (µW/MHz)		
		A3PE3000 L	A3P1000 L	A3P600 L
PAC1	Clock contribution of a Global Rib	19.7	14.50	12.80
PAC2	Clock contribution of a Global Spine	4.16	2.48	1.85
PAC3	Clock contribution of a VersaTile row	0.88	0.81	
PAC4	Clock contribution of a VersaTile used as a sequential module	0.12		
PAC5	First contribution of a VersaTile used as a sequential module	0.07		
PAC6	Second contribution of a VersaTile used as a sequential module	0.29		
PAC7	Contribution of a VersaTile used as a combinatorial Module	0.29		
PAC8	Average contribution of a routing net	0.70		
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-12. through Table 2-14.		
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-15 through Table 2-17.		
PAC11	Average contribution of a RAM block during a read operation	25.00		

TABLE 2-19: DIFFERENT COMPONENTS CONTRIBUTING TO DYNAMIC POWER CONSUMPTION IN PROASIC3L DEVICES AT 1.5 V VCC

Parameter	Definition	Device Specific Dynamic Power (µW/MHz)		
		A3PE3000 L	A3P1000 L	A3P600 L
PAC12	Average contribution of a RAM block during a write operation	30.00		
PAC13	Dynamic contribution for PLL	2.60		

Note: *For a different output load, drive strength, or slew rate, Microchip recommends using the Microchip power spreadsheet calculator or SmartPower tool in Libero SoC.

TABLE 2-20: DIFFERENT COMPONENTS CONTRIBUTING TO THE STATIC POWER CONSUMPTION IN PROASIC3L DEVICES

Parameter	Definition	Device Specific Dynamic Power (µW)		
		A3PE3000L	A3P1000L	A3P600L
PDC1	Array static power in Active mode	See Table 2-11.		
PDC2	Array static power in Static (Idle) mode	See Table 2-9.		
PDC3	Array static power in Flash*Freeze mode	See Table 2-8.		
PDC4	Static PLL contribution at 1.2 V core (operating mode only)	1.42 mW		
	Static PLL contribution at 1.5 V core (operating mode only)	2.55 mW		
PDC5	Bank quiescent power (VCCI-dependent)	See Table 2-8, Table 2-9, Table 2-11.		
PDC6	I/O input pin static power (standard-dependent)	See Table 2-12 through Table 2-14.		
PDC7	I/O output pin static power (standard-dependent)	See Table 2-15 through Table 2-17.		

Note: *For a different output load, drive strength, or slew rate, Microchip recommends using the Microchip power spreadsheet calculator or SmartPower tool in Libero SoC.

2.2.4 POWER CALCULATION METHODOLOGY

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-21.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-22.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-22. The calculation should be repeated for each clock domain defined in the design.

2.2.4.1 Methodology

2.2.4.1.1 Total Power Consumption—P_{TOTAL}

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

2.2.4.1.2 Total Static Power Consumption—P_{STAT}

P_{STAT} = (PDC1 or PDC2 or PDC3) + N_{BANKS}* PDC5 + N_{INPUTS}* PDC6 + $N_{OUTPUTS}$* PDC7

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

N_{BANKS} is the number of I/O banks powered in the design.

2.2.4.1.3 Total Dynamic Power Consumption—P_{DYN}

P_{DYN} = P_{CLOCK} + $P_{S\text{-}CELL}$ + $P_{C\text{-}CELL}$ + P_{NET} + P_{INPUTS} + $P_{OUTPUTS}$ + P_{MEMORY} + P_{PLL}

2.2.4.1.4 Global Clock Contribution—P_{CLOCK}

P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + $N_{S\text{-}CELL}$ * PAC4) * F_{CLK}

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the *ProASIC3L FPGA Fabric User's Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the *ProASIC3L FPGA Fabric User's Guide*.

F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

PAC1, PAC2, PAC3, and PAC4 are device-dependent.

2.2.4.1.5 Sequential Cells Contribution—$P_{S\text{-}CELL}$

$P_{S\text{-}CELL}$ = $N_{S\text{-}CELL}$ * (PAC5 + α_1 / 2 * PAC6) * F_{CLK}

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-21.

F_{CLK} is the global clock signal frequency.

2.2.4.1.6 Combinatorial Cells Contribution—$P_{C\text{-}CELL}$

$P_{C\text{-}CELL}$ = $N_{C\text{-}CELL}$* α_1 / 2 * PAC7 * F_{CLK}

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-21.

F_{CLK} is the global clock signal frequency.

2.2.4.1.7 Routing Net Contribution—P_{NET}

P_{NET} = ($N_{S\text{-}CELL}$ + $N_{C\text{-}CELL}$) * α_1 / 2 * PAC8 * F_{CLK}

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-21.

F_{CLK} is the global clock signal frequency.

2.2.4.1.8 I/O Input Buffer Contribution—P_{INPUTS}

P_{INPUTS} = N_{INPUTS} * α_2 / 2 * PAC9 * F_{CLK}

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-21.

F_{CLK} is the global clock signal frequency.

2.2.4.1.9 I/O Output Buffer Contribution—$P_{OUTPUTS}$

$P_{OUTPUTS}$ = $N_{OUTPUTS}$ * α_2 / 2 * β_1 * PAC10 * F_{CLK}

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-21.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-22.

F_{CLK} is the global clock signal frequency.

2.2.4.1.10 RAM Contribution—P_{MEMORY}

$P_{MEMORY} = PAC11 * N_{BLOCKS} * F_{READ\text{-}CLOCK} * \beta_2 + PAC12 * N_{BLOCK} * F_{WRITE\text{-}CLOCK} * \beta_3$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in Table 2-22.

2.2.4.1.11 PLL Contribution—P_{PLL}

$P_{PLL} = PDC4 + PAC13 * F_{CLKOUT}$

F_{CLKOUT} is the output clock frequency.[1]

2.2.4.2 Guidelines

2.2.4.2.1 Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . + 0.78125%) / 8

2.2.4.2.2 Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

TABLE 2-21: TOGGLE RATE GUIDELINES RECOMMENDED FOR POWER CALCULATION

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

TABLE 2-22: ENABLE RATE GUIDELINES RECOMMENDED FOR POWER CALCULATION

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%

1. *If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC13} * F_{CLKOUT}$ product) to the total PLL contribution.*

2.3 User I/O Characteristics

2.3.1 TIMING MODEL

FIGURE 2-3: TIMING MODEL (OPERATING CONDITIONS: –1 SPEED, COMMERCIAL TEMPERATURE RANGE (TJ = 70°C), WORST-CASE VCC = 1.14 V)

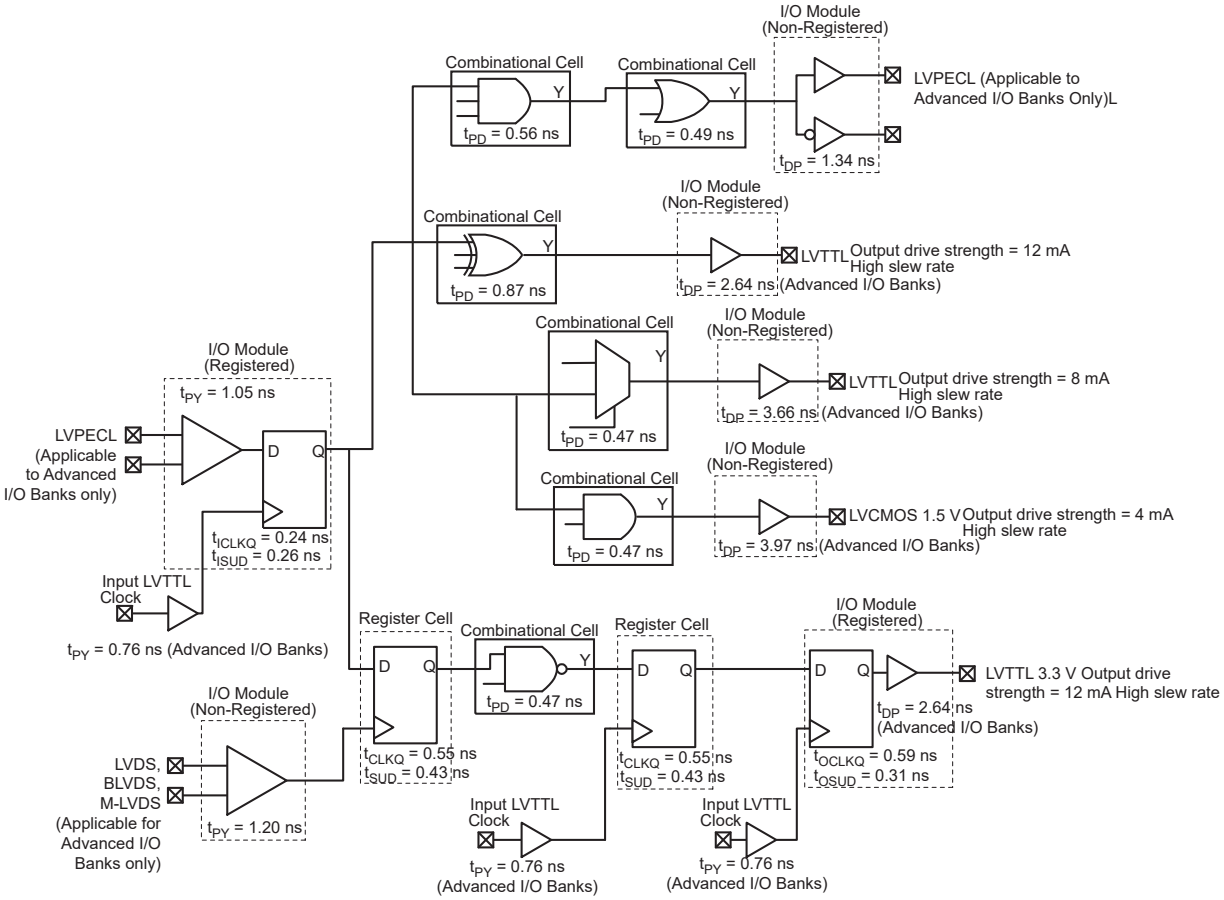
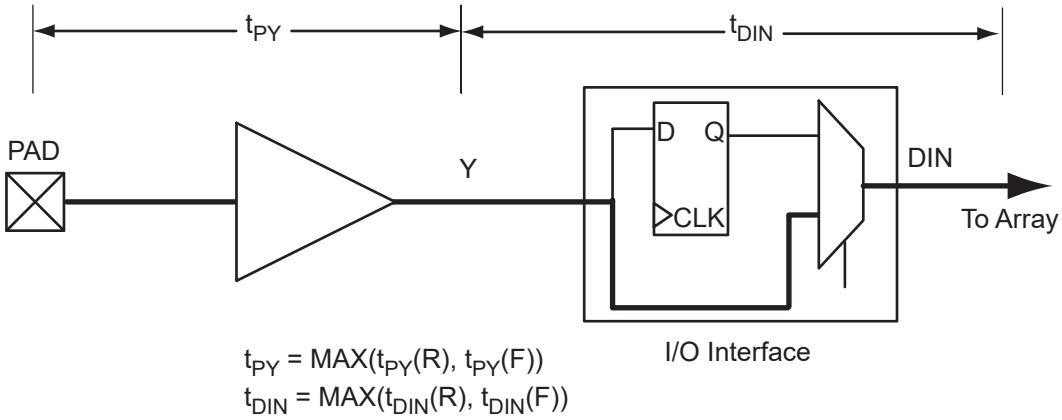


FIGURE 2-4: INPUT BUFFER TIMING MODEL AND DELAYS (EXAMPLE)



$t_{PY} = MAX(t_{PY}(R), t_{PY}(F))$
$t_{DIN} = MAX(t_{DIN}(R), t_{DIN}(F))$

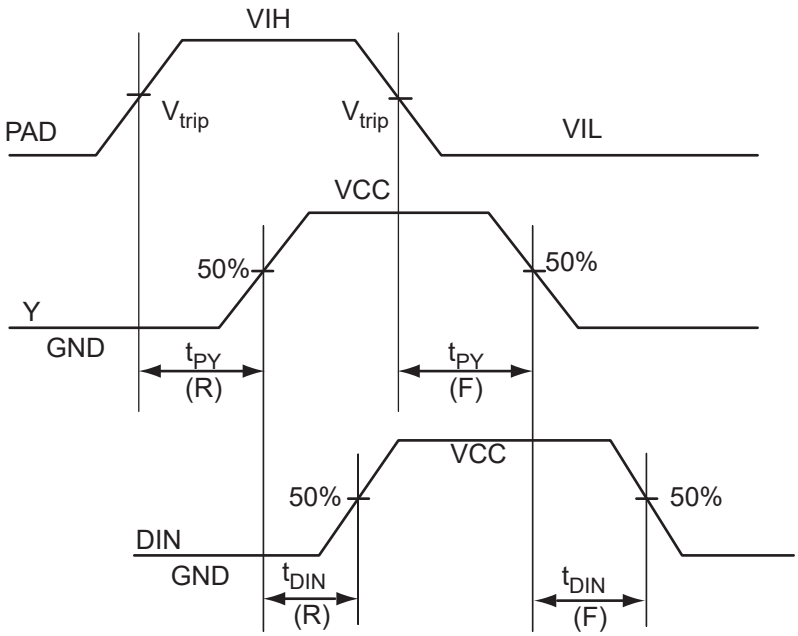


FIGURE 2-5: OUTPUT BUFFER MODEL AND DELAYS (EXAMPLE)

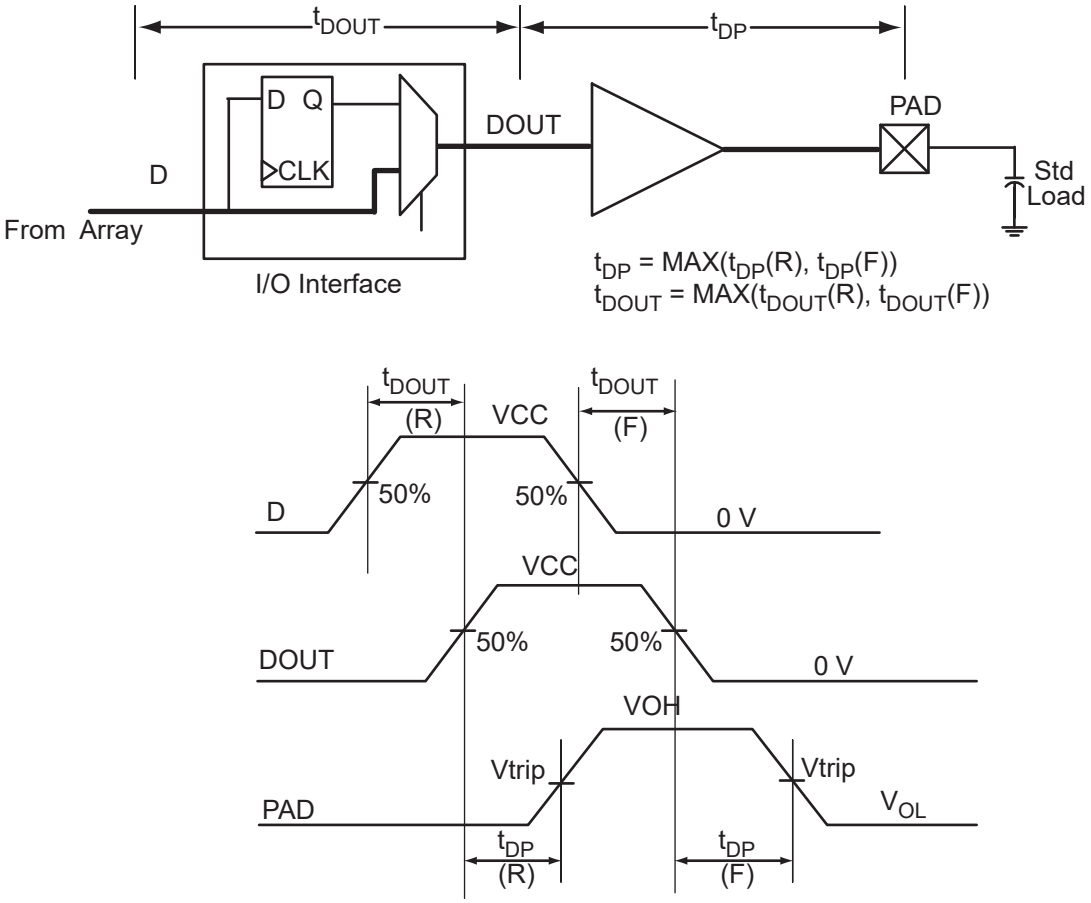
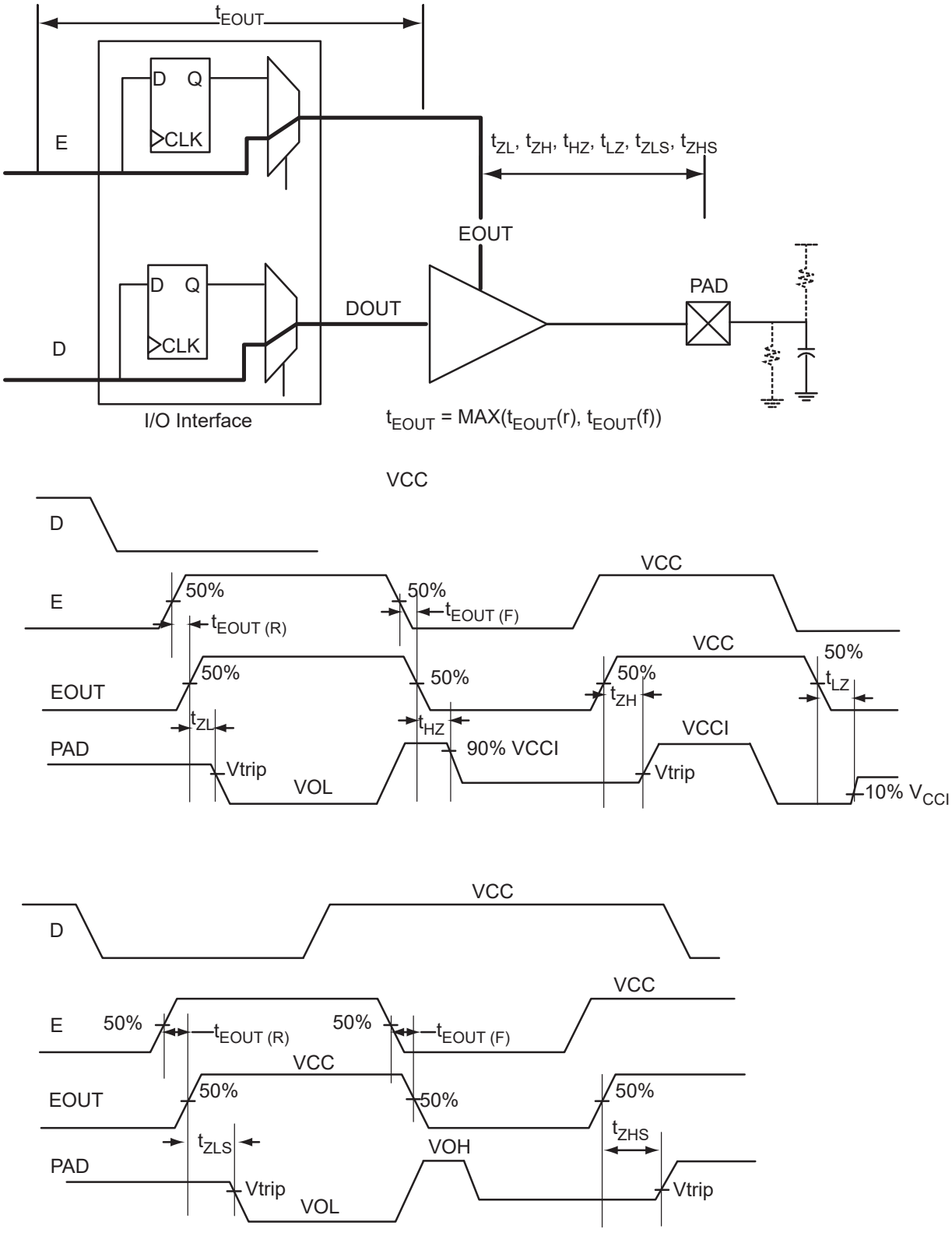


FIGURE 2-6: TRISTATE OUTPUT BUFFER TIMING MODEL AND DELAYS (EXAMPLE)



2.3.2 OVERVIEW OF I/O PERFORMANCE

2.3.2.1 Summary of I/O DC Input and Output Levels – Default I/O Software Settings

TABLE 2-23: SUMMARY OF MAXIMUM AND MINIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO COMMERCIAL AND INDUSTRIAL CONDITIONS—SOFTWARE DEFAULT SETTINGS (APPLICABLE TO PRO I/O BANKS)

I/O Standard	Drive Strength (mA)	Equiv. Software Default Drive Strength Option[1]	Slew Rate	VIL		VIH		VOL	VOH	IOL[3]	IOH[3]
				Min. V	Max. V	Min. V	Max.[2] V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	– 0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVCMOS Wide Range[4]	100 µA	12 mA	High	– 0.3	0.8	2	3.6	0.2	VCCI – 0.2	0.1	0.1
2.5 V LVCMOS	12 mA	12 mA	High	– 0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	12 mA	High	– 0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	12	12
1.5 V LVCMOS	12 mA	12 mA	High	– 0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	12	12
1.2 V LVCMOS	2 mA	2 mA	High	– 0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	2	2
1.2 V LVCMOS Wide Range[5]	100 µA	2 mA	High	– 0.3	0.3 * VCCI	0.7 * VCCI	1.575	0.1	VCCI – 0.1	0.1	0.1
3.3 V PCI	Per PCI Specification										
3.3 V PCI-X	Per PCI-X Specification										
3.3 V GTL	20 mA[6]	20 mA[6]	High	– 0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	–	20	20
2.5 V GTL	20 mA[6]	20 mA[6]	High	– 0.3	VREF – 0.05	VREF + 0.05	2.7	0.4	–	20	20
3.3 V GTL+	35 mA	35 mA	High	– 0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	35	35
2.5 V GTL+	33 mA	33 mA	High	– 0.3	VREF – 0.1	VREF + 0.1	2.7	0.6	–	33	33
HSTL (I)	8 mA	8 mA	High	– 0.3	VREF – 0.1	VREF + 0.1	1.575	0.4	VCCI – 0.4	8	8
HSTL (II)	15 mA[6]	15 mA[6]	High	– 0.3	VREF – 0.1	VREF + 0.1	1.575	0.4	VCCI – 0.4	15	15
SSTL2 (I)	15 mA	15 mA	High	– 0.3	VREF – 0.1	VREF + 0.1	2.7	0.54	VCCI – 0.62	15	15
SSTL2 (II)	18 mA	18 mA	High	– 0.3	VREF – 0.1	VREF + 0.1	2.7	0.35	VCCI – 0.43	18	18

TABLE 2-23: SUMMARY OF MAXIMUM AND MINIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO COMMERCIAL AND INDUSTRIAL CONDITIONS—SOFTWARE DEFAULT SETTINGS (APPLICABLE TO PRO I/O BANKS)

I/O Standard	Drive Strength (mA)	Equiv. Software Default Drive Strength Option[1]	Slew Rate	VIL		VIH		VOL	VOH	IOL[3]	IOH[3]
				Min. V	Max. V	Min. V	Max.[2] V	Max. V	Min. V	mA	mA
SSTL3 (I)	14 mA	14 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.7	VCCI – 1.1	14	14
SSTL3 (II)	21 mA	21 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.5	VCCI – 0.9	21	21

Note 1: Please note that 1.2V LVCMOS and 3.3V LVCMOS wide range is applicable to 100uA drive strength only. The configuration will NOT operate at the equivalent software.

2: Maximum VIH is 3.6 V for all I/O standards with hot-insertion is enabled.

3: Currents are measured at 85°C junction temperature.

4: All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.

5: All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.

6: Output drive strength is below JEDEC specification.

7: Output slew rate can be extracted using the IBIS models.

TABLE 2-24: SUMMARY OF MAXIMUM AND MINIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO COMMERCIAL AND INDUSTRIAL CONDITIONS—SOFTWARE DEFAULT SETTINGS (APPLICABLE TO ADVANCED I/O BANKS)

I/O Standard	Drive Strength	Equiv. Software Default Drive Strength Option[1]	Slew Rate	VIL		VIH		VOL	VOH	IOL[2]	IOH[2]
				Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVCMOS Wide Range[3]	100 µA	12 mA	High	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	0.1	0.1
2.5 V LVCMOS	12 mA	12 mA	High	–0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	12	12
1.5 V LVCMOS	12 mA	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	12	12

TABLE 2-24: SUMMARY OF MAXIMUM AND MINIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO COMMERCIAL AND INDUSTRIAL CONDITIONS—SOFTWARE DEFAULT SETTINGS (APPLICABLE TO ADVANCED I/O BANKS)

I/O Standard	Drive Strength	Equiv. Software Default Drive Strength Option[1]	Slew Rate	VIL		VIH		VOL	VOH	IOL[2]	IOH[2]
				Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
1.2 V LVCMOS	2 mA	2 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	2	2
1.2 V LVCMOS Wide Range[4,5]	100 µA	2 mA	High	–0.3	0.3 * VCCI	0.7 * VCCI	1.575	0.1	VCCI – 0.1	0.1	0.1
3.3 V PCI	Per PCI specifications										
3.3 V PCI-X	Per PCI-X specifications										

Note 1: Please note that 1.2 V LVCMOS and 3.3 V LVCMOS wide range is applicable to 100 µA drive strength only. The configuration will NOT operate at the equivalent software.

2: Currents are measured at 85°C junction temperature.

3: All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.

4: All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.

5: Applicable to devices operating at VCCI ≥ VCC.

6: Output slew rate can be extracted using the IBIS models.

TABLE 2-25: SUMMARY OF MAXIMUM AND MINIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO COMMERCIAL AND INDUSTRIAL CONDITIONS—SOFTWARE DEFAULT SETTINGS (APPLICABLE TO STANDARD PLUS I/O BANKS)

I/O Standard	Drive Strength	Equiv. Software Default Drive Strength Option[1]	Slew Rate	VIL		VIH		VOL	VOH	IOL[2]	IOH[2]
				Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVCMOS Wide Range[3]	100 µA	12 mA	High	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	0.1	0.1
2.5 V LVCMOS	12 mA	12 mA	High	–0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8 V LVCMOS	8 mA	8 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	8	8

TABLE 2-25: SUMMARY OF MAXIMUM AND MINIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO COMMERCIAL AND INDUSTRIAL CONDITIONS—SOFTWARE DEFAULT SETTINGS (APPLICABLE TO STANDARD PLUS I/O BANKS)

I/O Standard	Drive Strength	Equiv. Software Default Drive Strength Option[1]	Slew Rate	VIL		VIH		VOL	VOH	IOL[2]	IOH[2]
				Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
1.5 V LVC-MOS	4 mA	4 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4
1.2 V LVC-MOS[4]	2 mA	2 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	2	2
1.2 V LVCMOS Wide Range[4,5]	100 µA	2 mA	High	–0.3	0.3 * VCCI	0.7 * VCCI	1.575	0.1	VCCI – 0.1	0.1	0.1
3.3 V PCI	Per PCI specifications										
3.3 V PCI-X	Per PCI-X specifications										

Note 1: Please note that 1.2 V LVCMOS and 3.3 V LVCMOS wide range is applicable to 100 µA drive strength only. The configuration will NOT operate at the equivalent software.

2: Currents are measured at 85°C junction temperature.

3: All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.

4: All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.

5: Applicable to devices operating at VCCI ≥ VCC.

6: Output slew rate can be extracted using the IBIS models.

TABLE 2-26: SUMMARY OF MAXIMUM AND MINIMUM DC INPUT LEVELS (APPLICABLE TO COMMERCIAL AND INDUSTRIAL CONDITIONS)

DC I/O Standard	Commercial[1]		Industrial[2]	
	IIL	IIH	IIL[3]	IIH[4]
	µA	µA	µA	µA
3.3 V LVTTL / 3.3 V LVCMOS	10	10	15	15
3.3 V LVCMOS Wide Range	10	10	15	15
2.5 V LVCMOS	10	10	15	15
1.8 V LVCMOS	10	10	15	15
1.5 V LVCMOS	10	10	15	15
1.2 V LVCMOS[5]	10	10	15	15

Note 1: Commercial range (0°C < T_A < 70°C)

2: Industrial range (–40°C < T_A < 85°C)

3: IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN <VIL.

4: IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

5: Applicable to devices operating at VCCI ≥ VCC.

TABLE 2-26: SUMMARY OF MAXIMUM AND MINIMUM DC INPUT LEVELS (APPLICABLE TO COMMERCIAL AND INDUSTRIAL CONDITIONS)

DC I/O Standard	Commercial[1]		Industrial[2]	
	IIL	IIH	IIL[3]	IIH[4]
	µA	µA	µA	µA
1.2 V LVCMOS Wide Range[5]	10	10	15	15
3.3 V PCI	10	10	15	15
3.3 V PCI-X	10	10	15	15
3.3 V GTL	10	10	15	15
2.5 V GTL	10	10	15	15
3.3 V GTL+	10	10	15	15
2.5 V GTL+	10	10	15	15
HSTL (I)	10	10	15	15
HSTL (II)	10	10	15	15
SSTL2 (I)	10	10	15	15
SSTL2 (II)	10	10	15	15
SSTL3 (I)	10	10	15	15
SSTL3 (II)	10	10	15	15

Note 1: Commercial range (0°C < T_A < 70°C)

2: Industrial range (–40°C < T_A < 85°C)

3: IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN <VIL.

4: IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

5: Applicable to devices operating at VCCI ≥ VCC.

2.3.2.2 Summary of I/O Timing Characteristics – Default I/O Software Settings

TABLE 2-27: SUMMARY OF AC MEASURING POINTS

Standard	Input Reference Voltage (VREF_TYP)	Board Termination Voltage (VTT_REF)	Measuring Trip Point (Vtrip)
3.3 V LVTTL / 3.3 V LVCMOS	–	–	1.4 V
3.3 V LVCMOS Wide Range	–	–	1.4 V
2.5 V LVCMOS	–	–	1.2 V
1.8 V LVCMOS	–	–	0.90 V
1.5 V LVCMOS	–	–	0.75 V
1.2 V LVCMOS *	–	–	0.6 V
1.2 V LVCMOS Wide Range*	–	–	0.6 V
3.3 V PCI	–	–	0.285 * VCCI (RR)
			0.615 * VCCI (FF))
3.3 V PCI-X	–	–	0.285 * VCCI (RR)
			0.615 * VCCI (FF)
3.3 V GTL	0.8 V	1.2 V	VREF
2.5 V GTL	0.8 V	1.2 V	VREF
3.3 V GTL+	1.0 V	1.5 V	VREF
2.5 V GTL+	1.0 V	1.5 V	VREF
HSTL (I)	0.75 V	0.75 V	VREF
HSTL (II)	0.75 V	0.75 V	VREF
SSTL2 (I)	1.25 V	1.25 V	VREF
SSTL2 (II)	1.25 V	1.25 V	VREF
SSTL3 (I)	1.5 V	1.485 V	VREF
SSTL3 (II)	1.5 V	1.485 V	VREF
LVDS	–	–	Cross point
LVPECL	–	–	Cross point

Note: *Applicable only to devices operating in the 1.2 V core range.

TABLE 2-28: I/O AC PARAMETER DEFINITIONS

Parameter	Parameter Definition
t_{DP}	Data to Pad delay through the Output Buffer
t_{PY}	Pad to Data delay through the Input Buffer
t_{DOUT}	Data to Output Buffer delay through the I/O interface
t_{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t_{DIN}	Input Buffer to Data delay through the I/O interface
t_{HZ}	Enable to Pad delay through the Output Buffer—High to Z
t_{ZH}	Enable to Pad delay through the Output Buffer—Z to High
t_{LZ}	Enable to Pad delay through the Output Buffer—Low to Z
t_{ZL}	Enable to Pad delay through the Output Buffer—Z to Low
t_{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to High
t_{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to Low

1.5 V DC Core Voltage

TABLE 2-29: SUMMARY OF I/O TIMING CHARACTERISTICS—SOFTWARE DEFAULT SETTINGS (–1 SPEED GRADE, COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST CASE VCC = 1.425V, WORST CASE VCCI, PRO I/O BANKS)

Standard	Drive Strength (mA)	Equiv. Software Default Drive Strength Option[1]	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	tEOUT (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	5	–	0.50	1.89	0.03	1.34	1.85	0.33	1.93	1.42	2.51	2.77	3.64	3.13	ns
3.3 V LVC-MOS Wide Range[1,2]	100 µA	12 mA	High	5	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
2.5 V LVCMOS	12 mA	12 mA	High	5	–	0.50	1.92	0.03	1.58	1.97	0.33	1.96	1.59	2.58	2.68	3.67	3.30	ns
1.8 V LVCMOS	12 mA	12 mA	High	5	–	0.50	2.14	0.03	1.53	2.17	0.33	2.18	1.76	2.86	3.24	3.89	3.47	ns
1.5 V LVCMOS	12 mA	12 mA	High	5	–	0.50	2.46	0.03	1.69	2.36	0.33	2.51	2.04	3.03	3.35	4.22	3.75	ns
3.3 V PCI	Per PCI spec.	–	High	5	25[3]	0.50	2.15	0.03	2.10	2.84	0.33	2.19	1.53	2.51	2.77	3.90	3.24	ns
3.3 V PCI-X	Per PCI-X spec.	–	High	10	25[3]	0.50	2.15	0.03	2.10	2.84	0.33	2.19	1.53	2.51	2.77	3.90	3.24	ns
3.3 V GTL	20 mA[5]	20 mA[5]	High	10	25	0.50	1.59	0.03	1.80	–	0.33	1.56	1.59	–	–	3.27	3.30	ns
2.5 V GTL	20 mA[5]	20 mA[5]	High	10	25	0.50	1.63	0.03	1.75	–	0.33	1.66	1.63	–	–	3.37	3.34	ns
3.3 V GTL+	35 mA	35 mA	High	10	25	0.50	1.57	0.03	1.80	–	0.33	1.60	1.57	–	–	3.31	3.29	ns
2.5 V GTL+	33 mA	33 mA	High	10	25	0.50	1.69	0.03	1.75	–	0.33	1.72	1.61	–	–	3.43	3.32	ns
HSTL (I)	8 mA	8 mA	High	20	25	0.50	2.43	0.03	2.12	–	0.33	2.48	2.41	–	–	4.19	4.12	ns
HSTL (II)	15 mA[5]	15 mA	High	20	50	0.50	2.32	0.03	2.12	–	0.33	2.36	2.08	–	–	4.07	3.79	ns

Note 1: The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.

3: Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 for connectivity. This resistor is not required during normal operation.

4: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

5: Output drive strength is below JEDEC specification.

TABLE 2-29: SUMMARY OF I/O TIMING CHARACTERISTICS—SOFTWARE DEFAULT SETTINGS (–1 SPEED GRADE, COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST CASE VCC = 1.425V, WORST CASE VCCI, PRO I/O BANKS)

Standard	Drive Strength (mA)	Equiv. Software Default Drive Strength Option[1]	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	tEOUT (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
SSTL2 (I)	15 mA	15 mA	High	30	25	0.50	1.63	0.03	1.61	–	0.33	1.66	1.41	–	–	1.66	1.41	ns
SSTL2 (II)	18 mA	18 mA	High	30	50	0.50	1.66	0.03	1.61	–	0.33	1.69	1.36	–	–	1.69	1.36	ns
SSTL3 (I)	14 mA	14 mA	High	30	25	0.50	1.77	0.03	1.54	–	0.33	1.80	1.41	–	–	1.80	1.41	ns
SSTL3 (II)	21 mA	21 mA	High	30	50	0.50	1.58	0.03	1.54	–	0.33	1.61	1.28	–	–	1.61	1.28	ns
LVDS	24 mA	24 mA	High	–	–	0.50	1.40	0.03	1.85	–	–	–	–	–	–	–	–	ns
LVPECL	24 mA	24 mA	High	–	–	0.50	1.40	0.03	1.67	–	–	–	–	–	–	–	–	ns

Note 1: The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.

3: Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 for connectivity. This resistor is not required during normal operation.

4: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

5: Output drive strength is below JEDEC specification.

TABLE 2-30: SUMMARY OF I/O TIMING CHARACTERISTICS—SOFTWARE DEFAULT SETTINGS (–1 SPEED GRADE, COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST CASE VCC = 1.425 V, WORST CASE VCCI, ADVANCED I/O BANKS)

I/O Standard	Drive Strength (mA)	Equiv. Software Default Drive Strength Option[1]	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	tEOUT (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	5	–	0.46	1.83	0.03	0.78	0.33	1.87	1.39	2.46	2.74	3.58	3.10	ns
3.3 V LVCMOS Wide Range[1,2]	100 µA	12 mA	High	5	–	–	–	–	–	–	–	–	–	–	–	–	ns
2.5 V LVCMOS	12 mA	12 mA	High	5	–	0.46	1.85	0.03	1.00	0.33	1.88	1.55	2.53	2.63	3.59	3.26	ns

TABLE 2-30: SUMMARY OF I/O TIMING CHARACTERISTICS—SOFTWARE DEFAULT SETTINGS (–1 SPEED GRADE, COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST CASE VCC = 1.425 V, WORST CASE VCCI, ADVANCED I/O BANKS)

I/O Standard	Drive Strength (mA)	Equiv. Software Default Drive Strength Option[1]	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	tEOUT (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
1.8 V LVCMOS	12 mA	12 mA	High	5	–	0.46	2.04	0.03	0.93	0.33	2.08	1.73	2.83	3.12	3.79	3.45	ns
1.5 V LVCMOS	12 mA	12 mA	High	5	–	0.46	2.33	0.03	1.10	0.33	2.37	2.01	3.02	3.22	4.08	3.72	ns
3.3 V PCI	Per PCI spec.	–	High	5	25[3]	0.46	2.05	0.03	0.66	0.33	2.09	1.49	2.46	2.74	3.80	3.21	ns
3.3 V PCI-X	Per PCI-X spec.	–	High	10	25[3]	0.46	2.05	0.03	0.64	0.33	2.09	1.49	2.46	2.74	3.80	3.21	ns
LVDS	24 mA	–	High	–	–	0.46	1.40	0.03	1.23	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
LVPECL	24 mA	–	High	–	–	0.46	1.38	0.03	1.08	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns

Note 1: The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.

3: Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 for connectivity. This resistor is not required during normal operation.

4: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-31: SUMMARY OF I/O TIMING CHARACTERISTICS—SOFTWARE DEFAULT SETTINGS (–1 SPEED GRADE, COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST CASE VCC = 1.425 V, WORST CASE VCCI = 3.0 V, STANDARD PLUS I/O BANKS)

I/O Standard	Drive Strength (mA)	Equiv. Software Default Drive Strength Option[1]	Slew Rate	Capacitive Load (pF)	External Resistor	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	5	–	0.46	1.56	0.03	0.77	0.33	1.59	1.20	2.14	2.47	3.30	2.91	ns
3.3 V LVCMOS Wide Range[1,2]	100 µA	12 mA	High	5	–	–	–	–	–	–	–	–	–	–	–	–	ns
2.5 V LVCMOS	12 mA	12 mA	High	5	–	0.46	1.59	0.03	0.99	0.33	1.61	1.32	2.16	2.38	3.33	3.03	ns

TABLE 2-31: SUMMARY OF I/O TIMING CHARACTERISTICS—SOFTWARE DEFAULT SETTINGS (–1 SPEED GRADE, COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST CASE VCC = 1.425 V, WORST CASE VCCI = 3.0 V, STANDARD PLUS I/O BANKS)

I/O Standard	Drive Strength (mA)	Equiv. Software Default Drive Strength Option[1]	Slew Rate	Capacitive Load (pF)	External Resistor	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
1.8 V LVCMOS	8 mA	8 mA	High	5	–	0.46	1.59	0.03	0.99	0.33	1.61	1.32	2.16	2.38	3.33	3.03	ns
1.5 V LVCMOS	4 mA	4 mA	High	5	–	0.46	2.15	0.03	1.09	0.33	2.19	1.82	2.32	2.40	3.90	3.53	ns
3.3 V PCI	Per PCI spec.	–	High	10	25[3]	0.46	1.77	0.03	0.65	0.33	1.80	1.31	2.14	2.47	3.51	3.02	ns
3.3 V PCI-X	Per PCI-X spec.	–	High	10	25[3]	0.46	1.77	0.03	0.64	0.33	1.80	1.31	2.14	2.47	3.51	3.02	ns

Note 1: The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.

3: Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 for connectivity. This resistor is not required during normal operation.

4: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

1.2 V DC Core Voltage

TABLE 2-32: SUMMARY OF I/O TIMING CHARACTERISTICS—SOFTWARE DEFAULT SETTINGS (–1 SPEED GRADE, COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST CASE VCC = 1.14 V, WORST CASE VCCI, PRO I/O BANKS)

Standard	Drive Strength (mA)	Equiv. Software Default Drive Strength Option[1]	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVC-MOS	12 mA	12 mA	High	5	–	0.66	1.89	0.04	1.34	1.85	0.43	1.93	1.42	2.51	2.77	3.64	3.13	ns
3.3 V LVC-MOS Wide Range[1,2]	100 µA	12 mA	High	5	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
2.5 V LVC-MOS	12 mA	12 mA	High	5	–	0.66	1.92	0.04	1.58	1.97	0.43	1.96	1.59	2.58	2.68	3.67	3.30	ns
1.8 V LVC-MOS	12 mA	12 mA	High	5	–	0.66	2.14	0.04	1.53	2.17	0.43	2.18	1.76	2.86	3.24	3.89	3.47	ns
1.5 V LVC-MOS	12 mA	12 mA	High	5	–	0.66	2.46	0.04	1.69	2.36	0.43	2.51	2.04	3.03	3.35	4.22	3.75	ns
1.2 V LVC-MOS	2 mA	2 mA	High	5	–	0.66	4.12	0.04	2.02	2.99	0.43	3.83	3.37	4.06	3.84	5.48	5.02	ns
1.2 V LVC-MOS Wide Range[1,3]	100 µA	2 mA	High	5	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
3.3 V PCI	Per PCI spec.	–	High	10	25[4]	0.66	2.15	0.04	2.10	2.84	0.43	2.19	1.53	2.51	2.77	3.90	3.24	ns
3.3 V PCI-X	Per PCI-X spec.	–	High	10	25[4]	0.66	2.15	0.04	2.10	2.84	0.43	2.19	1.53	2.51	2.77	3.90	3.24	ns
3.3 V GTL	20 mA[6]	–	High	10	25	0.66	1.59	0.04	1.80	–	0.43	1.56	1.59	–	–	3.27	3.30	ns
2.5 V GTL	20 mA[6]	–	High	10	25	0.66	1.63	0.04	1.75	–	0.43	1.66	1.63	–	–	3.37	3.34	ns

Note 1: The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.

3: All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.

4: Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 for connectivity. This resistor is not required during normal operation.

5: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

6: Output drive strength is below JEDEC specification.

TABLE 2-32: SUMMARY OF I/O TIMING CHARACTERISTICS—SOFTWARE DEFAULT SETTINGS (–1 SPEED GRADE, COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST CASE VCC = 1.14 V, WORST CASE VCCI, PRO I/O BANKS)

Standard	Drive Strength (mA)	Equiv. Software Default Drive Strength Option[1]	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V GTL+	35 mA	–	High	10	25	0.66	1.57	0.04	1.80	–	0.43	1.60	1.57	–	–	3.31	3.29	ns
2.5 V GTL+	33 mA	–	High	10	25	0.66	1.69	0.04	1.75	–	0.43	1.72	1.61	–	–	3.43	3.32	ns
HSTL (I)	8 mA	–	High	20	25	0.66	2.43	0.04	2.12	–	0.43	2.48	2.41	–	–	4.19	4.12	ns
HSTL (II)	15 mA[6]	–	High	20	50	0.66	2.32	0.04	2.12	–	0.43	2.36	2.08	–	–	4.07	3.79	ns
SSTL2 (I)	15 mA	–	High	30	25	0.66	1.63	0.04	1.61	–	0.43	1.66	1.41	–	–	1.66	1.41	ns
SSTL2 (II)	18 mA	–	High	30	50	0.66	1.66	0.04	1.61	–	0.43	1.69	1.36	–	–	1.69	1.36	ns
SSTL3 (I)	14 mA	–	High	30	25	0.66	1.77	0.04	1.54	–	0.43	1.80	1.41	–	–	1.80	1.41	ns
SSTL3 (II)	21 mA	–	High	30	50	0.66	1.58	0.04	1.54	–	0.43	1.61	1.28	–	–	1.61	1.28	ns
LVDS	24 mA	–	High	–	–	0.66	1.43	0.04	1.85	–	–	–	–	–	–	–	–	ns
LVPECL	24 mA	–	High	–	–	0.66	1.37	0.04	1.67	–	–	–	–	–	–	–	–	ns

Note 1: The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.

3: All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.

4: Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 for connectivity. This resistor is not required during normal operation.

5: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

6: Output drive strength is below JEDEC specification.

TABLE 2-33: SUMMARY OF I/O TIMING CHARACTERISTICS—SOFTWARE DEFAULT SETTINGS (–1 SPEED GRADE, COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST CASE VCC = 1.14 V, WORST CASE VCCI, ADVANCED I/O BANKS)

I/O Standard	Drive Strength (mA)	Equiv. Software Default Drive Strength Option[1]	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	tEOUT (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	5 pF	–	0.60	1.83	0.04	0.78	0.43	1.87	1.39	2.46	2.74	3.58	3.10	ns
3.3 V LVCMOS Wide Range[1,2]	100 µA	12 mA	High	5 pF	–	–	–	–	–	–	–	–	–	–	–	–	ns
2.5 V LVCMOS	12 mA	12 mA	High	5 pF	–	0.60	1.85	0.04	1.00	0.43	1.88	1.55	2.53	2.63	3.59	3.26	ns
1.8 V LVCMOS	12 mA	12 mA	High	5 pF	–	0.60	2.04	0.04	0.93	0.43	2.08	1.73	2.83	3.12	3.79	3.45	ns
1.5 V LVCMOS	12 mA	12 mA	High	5 pF	–	0.60	2.33	0.04	1.10	0.43	2.37	2.01	3.02	3.22	4.08	3.72	ns
1.2 V LVCMOS	2 mA	2 mA	High	5pF	–	0.60	3.17	0.04	1.55	0.43	2.11	1.76	2.38	2.46	3.76	3.41	ns
1.2 V LVCMOS Wide Range[1,3]	100 µA	2 mA	High	5 pF	–	–	–	–	–	–	–	–	–	–	–	–	ns
3.3 V PCI	Per PCI spec.	–	High	10 pF	25[4]	0.60	2.05	0.04	0.66	0.43	2.09	1.49	2.46	2.74	3.80	3.21	ns
3.3 V PCI-X	Per PCI-X spec.	–	High	10 pF	25[4]	0.60	2.05	0.04	0.64	0.43	2.09	1.49	2.46	2.74	3.80	3.21	ns
LVDS	24 mA	–	High	–	–	0.60	1.40	0.04	1.23	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
LVPECL	24 mA	–	High	–	–	0.60	1.38	0.04	1.08	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns

Note 1: The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.

3: All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.

4: Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 for connectivity. This resistor is not required during normal operation.

5: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-34: SUMMARY OF I/O TIMING CHARACTERISTICS—SOFTWARE DEFAULT SETTINGS (–1 SPEED GRADE, COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST CASE VCC = 1.14 V, WORST CASE VCCI = 3.0 V, STANDARD PLUS I/O BANKS)

I/O Standard	Drive Strength (mA)	Equiv. Software Default Drive Strength Option[1]	Slew Rate	Capacitive Load (pF)	External Resistor	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	tEOUT (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	5 pF	–	0.60	1.56	0.04	0.77	0.43	1.59	1.20	2.14	2.47	3.30	2.91	ns
3.3 V LVCMOS Wide Range[1,2]	100 µA	12 mA	High	5 pF	–	–	–	–	–	–	–	–	–	–	–	–	ns
2.5 V LVCMOS	12 mA	12 mA	High	5 pF	–	0.60	1.59	0.04	0.99	0.43	1.61	1.32	2.16	2.38	3.33	3.03	ns
1.8 V LVCMOS	8 mA	8 mA	High	5 pF	–	0.60	1.59	0.04	0.99	0.43	1.61	1.32	2.16	2.38	3.33	3.03	ns
1.5 V LVCMOS	4 mA	4 mA	High	5 pF	–	0.60	2.15	0.04	1.09	0.43	2.19	1.82	2.32	2.40	3.90	3.53	ns
1.2 V LVCMOS	2 mA	2 mA	High	5 pF	–	0.60	3.54	0.04	1.56	0.43	2.37	2.11	3.60	3.87	4.02	3.76	ns
1.2 V LVCMOS Wide Range[1,3]	100 µA	2 mA	High	5 pF	–	–	–	–	–	–	–	–	–	–	–	–	ns
3.3 V PCI	Per PCI spec.	–	High	10 pF	25[4]	0.60	1.77	0.04	0.65	0.43	1.80	1.31	2.14	2.47	3.51	3.02	ns
3.3 V PCI-X	Per PCI-X spec.	–	High	10 pF	25[4]	0.60	1.77	0.04	0.64	0.43	1.80	1.31	2.14	2.47	3.51	3.02	ns

Note 1: The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.

3: All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.

4: Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 for connectivity. This resistor is not required during normal operation.

5: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.3.3 DETAILED I/O DC CHARACTERISTICS

TABLE 2-35: INPUT CAPACITANCE

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	V_{IN} = 0, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	V_{IN} = 0, f = 1.0 MHz		8	pF

TABLE 2-36: I/O OUTPUT BUFFER MAXIMUM RESISTANCES[1] (APPLICABLE TO PRO I/OS)

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω) [2]	$R_{PULL\text{-}UP}$ (Ω) [3]
3.3 V LVTTL / 3.3 V LVCMOS	4 mA	100	300
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
3.3 V LVCMOS Wide Range	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	4 mA	100	200
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
1.2 V LVCMOS	2 mA	158	164
1.2 V LVCMOS Wide Range	100 µA	Same as regular 1.2 V LVCMOS	Same as regular 1.2 V LVCMOS
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75
3.3 V GTL	20 mA[4]	11	–
2.5 V GTL	20 mA[4]	14	–
3.3 V GTL+	35 mA	12	–
2.5 V GTL+	33 mA	15	–
HSTL (I)	8 mA	50	50
HSTL (II)	15 mA[4]	25	25
SSTL2 (I)	15 mA	27	31
SSTL2 (II)	18 mA	13	15
SSTL3 (I)	14 mA	44	69
SSTL3 (II)	21 mA	18	32

TABLE 2-36: I/O OUTPUT BUFFER MAXIMUM RESISTANCES[1] (APPLICABLE TO PRO I/OS)

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω) [2]	$R_{PULL\text{-}UP}$ (Ω) [3]

Note 1: These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at http://www.microsemi.com/soc/download/ibis/default.aspx.

2: $R_{(PULL\text{-}DOWN\text{-}MAX)}$ = (VOLspec) / IOLspec

3: $R_{(PULL\text{-}UP\text{-}MAX)}$ = (VCCImax – VOHspec) / IOHspec

4: Output drive strength is below JEDEC specification.

TABLE 2-37: I/O OUTPUT BUFFER MAXIMUM RESISTANCES[1] (APPLICABLE TO ADVANCED I/O BANKS)

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω) [2]	$R_{PULL\text{-}UP}$ (Ω) [3]
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
3.3 V LVCMOS Wide Range	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
1.8 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
1.2 V LVCMOS	2 mA	158	164
1.2 V LVCMOS Wide Range	100 µA	Same as regular 1.2 V LVCMOS	Same as regular 1.2 V LVCMOS
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

TABLE 2-37: I/O OUTPUT BUFFER MAXIMUM RESISTANCES[1] (APPLICABLE TO ADVANCED I/O BANKS)

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω) [2]	$R_{PULL\text{-}UP}$ (Ω) [3]

Note 1: These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCI}, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at http://www.microsemi.com/soc/download/ibis/default.aspx.

2: $R_{(PULL\text{-}DOWN\text{-}MAX)}$ = (VOLspec) / IOLspec

3: $R_{(PULL\text{-}UP\text{-}MAX)}$ = (VCCImax – VOHspec) / IOHspec

TABLE 2-38: I/O OUTPUT BUFFER MAXIMUM RESISTANCES[1] (APPLICABLE TO STANDARD PLUS I/O BANKS)

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω) [2]	$R_{PULL\text{-}UP}$ (Ω) [3]
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	25	75
3.3 V LVCMOS Wide Range	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
1.2 V LVCMOS	2 mA	158	164
1.2 V LVCMOS Wide Range	100 µA	Same as regular 1.2 V LVCMOS	Same as regular 1.2 V LVCMOS
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Note 1: These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at http://www.microsemi.com/soc/download/ibis/default.aspx.

2: $R_{(PULL\text{-}DOWN\text{-}MAX)}$ = (VOLspec) / IOLspec

3: $R_{(PULL\text{-}UP\text{-}MAX)}$ = (VCCImax – VOHspec) / IOHspec

TABLE 2-39: I/O WEAK PULL-UP/PULL-DOWN RESISTANCES (MINIMUM AND MAXIMUM WEAK PULL-UP/PULL-DOWN RESISTANCE VALUES)

VCCI	$R_{(WEAK\ PULL\text{-}UP)}$[1] (Ω)		$R_{(WEAK\ PULL\text{-}DOWN)}$[2] (Ω)	
	Min.	Max.	Min.	Max.
3.3 V	10 k	45 k	10 k	45 k
3.3 V (wide range I/Os)	10 k	45 k	10 k	45 k
2.5 V	11 k	55 k	12 k	74 k
1.8 V	18 k	70 k	17 k	110 k
1.5 V	19 k	90 k	19 k	140 k
1.2 V LVCMOS	25 k	110 k	25 k	150 k
1.2 V (wide range I/Os)	19 k	110 k	19 k	150 k

Note 1: $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)} = (VCCImax - VOHspec) / I_{(WEAK\ PULL\text{-}UP\text{-}MIN)}$

2: $R_{(WEAK\ PULL\text{-}DOWN\text{-}MAX)} = (VOLspec) / I_{(WEAK\ PULL\text{-}DOWN\text{-}MIN)}$

TABLE 2-40: I/O SHORT CURRENTS IOSH/IOSL (APPLICABLE TO PRO I/OS)

Standard	Drive Strength	IOSL (mA)*	IOSH (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
3.3 V LVCMOS Wide Range	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
1.2 V LVCMOS	2 mA	20	26
1.2 V LVCMOS Wide Range	100 µA	20	26
3.3 V PCI/PCIX	Per PCI/PCI-X Specification	Per PCI Curves	
3.3 V GTL	20 mA[2]	268	181
2.5 V GTL	20 mA[2]	169	124
3.3 V GTL+	35 mA	268	181
2.5 V GTL+	33 mA	169	124
HSTL (I)	8 mA	32	39
HSTL (II)	15 mA[2]	66	55
SSTL2 (I)	15 mA	83	87
SSTL2 (II)	18 mA	169	124
SSTL3 (I)	14 mA	51	54

Note 1: *TJ = 100°C

2: Output drive strength is below JEDEC specification.

TABLE 2-41: I/O SHORT CURRENTS IOSH/IOS$_L$ (APPLICABLE TO ADVANCED I/O BANKS)

Standard	Drive Strength	IOSL (mA)*	IOSH (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
3.3 V LVCMOS Wide Range	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
1.2 V LVCMOS	2 mA	20	26
1.2 V LVCMOS Wide Range	100 µA	20	26
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	103	109

Note: *T_J = 100°C

TABLE 2-42: I/O SHORT CURRENTS IOSH/IOSL (APPLICABLE TO STANDARD PLUS I/O BANKS)

	Drive Strength	IOSL (mA)*	IOSH (mA)*
3.3 V LVTTL / 3.3 V LVC-MOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	103	109
3.3 V LVCMOS Wide Range	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS

TABLE 2-42: I/O SHORT CURRENTS IOSH/IOSL (APPLICABLE TO STANDARD PLUS I/O BANKS)

	Drive Strength	IOSL (mA)*	IOSH (mA)*
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
	12 mA	65	74
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	35	44
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
1.2 V LVCMOS	2 mA	20	26
1.2 V LVCMOS Wide Range	100 µA	20	26
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	103	109

Note: T_J = 100°C

TABLE 2-43: SCHMITT TRIGGER INPUT HYSTERESIS, HYSTERESIS VOLTAGE VALUE (TYP) FOR SCHMITT MODE INPUT BUFFERS

Input Buffer Configuration	Hysteresis Value (typ.)
3.3 V LVTTL/LVCMOS/PCI/PCI-X (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV
1.2 V LVCMOS (Schmitt trigger mode)	40 mV

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3 V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

TABLE 2-44: DURATION OF SHORT CIRCUIT EVENT BEFORE FAILURE

Temperature	Time before Failure
–40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months

TABLE 2-45: I/O INPUT RISE TIME, FALL TIME, AND RELATED I/O RELIABILITY

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS	No requirement	10 ns *	20 years (110°C)
LVDS/B-LVDS/ M-LVDS/LVPECL	No requirement	10 ns *	10 years (100°C)

TABLE 2-45: I/O INPUT RISE TIME, FALL TIME, AND RELATED I/O RELIABILITY

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability

Note: *The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microchip recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.

2.3.4 SINGLE-ENDED I/O CHARACTERISTICS

2.3.4.1 3.3 V LVTTL / 3.3 V LVCMOS

Low voltage transistor–transistor Logic (LVTTL) is a general-purpose standard (EIA/JESD) for 3.3 V applications. This standard uses an LVTTL input buffer and push-pull output buffer. Furthermore, all LVCMOS 3.3 V software macros comply with LVCMOS 3.3 V wide range, as specified in the JESD8-A specification.

TABLE 2-46: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS (APPLICABLE TO PRO I/O BANKS)

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	10	10
12 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	132	127	10	10
16 mA	–0.3	0.8	2	3.6	0.4	2.4	24	24	268	181	10	10
24 mA	–0.3	0.8	2	3.6	0.4	2.4	24	24	27	25	10	10

Note 1: Currents are measured at 100°C junction temperature and maximum voltage.
2: Currents are measured at 85°C junction temperature.
3: Software default selection highlighted in gray.

TABLE 2-47: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS (APPLICABLE TO ADVANCED I/O BANKS)

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	10	10
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	132	127	10	10
24 mA	–0.3	0.8	2	3.6	0.4	2.4	24	24	268	181	10	10

Note 1: Currents are measured at 100°C junction temperature and maximum voltage.
2: Currents are measured at 85°C junction temperature.
3: Software default selection highlighted in gray.

TABLE 2-48: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS (APPLICABLE TO STANDARD PLUS I/O BANKS)

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	10	10
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	103	109	10	10

Note 1: Currents are measured at 100°C junction temperature and maximum voltage.

2: Currents are measured at 85°C junction temperature.

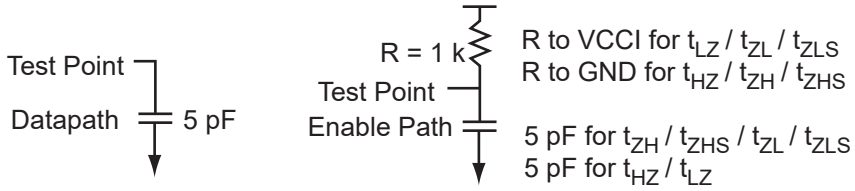
3: Software default selection highlighted in gray.

TABLE 2-49: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	3.3	1.4	5

*Measuring point = Vtrip. See Table 2-27 for a complete table of trip points.

FIGURE 2-7: AC LOADING



2.3.4.1.1 Timing Characteristics

1.5 V DC Core Voltage

TABLE 2-50: 3.3 V LVTTL / 3.3 V LVCMOS LOW SLEW – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 3.0 V, APPLICABLE TO PRO I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.59	5.48	0.04	1.58	2.17	0.38	5.58	4.40	2.42	2.20	7.60	6.42	ns
	–1	0.50	4.66	0.03	1.34	1.85	0.33	4.75	3.75	2.06	1.87	6.46	5.46	ns
8 mA	Std.	0.59	4.48	0.04	1.58	2.17	0.38	4.56	3.76	2.73	2.76	6.57	5.78	ns
	–1	0.50	3.81	0.03	1.34	1.85	0.33	3.88	3.20	2.33	2.35	5.59	4.91	ns
12 mA	Std.	0.59	3.77	0.04	1.58	2.17	0.38	3.84	3.28	2.95	3.12	5.85	5.29	ns
	–1	0.50	3.21	0.03	1.34	1.85	0.33	3.27	2.79	2.51	2.65	4.98	4.50	ns
16 mA	Std.	0.59	3.57	0.04	1.58	2.17	0.38	3.63	3.18	2.99	3.22	5.64	5.19	ns
	–1	0.50	3.03	0.03	1.34	1.85	0.33	3.09	2.70	2.54	2.74	4.80	4.41	ns
24 mA	Std.	0.59	3.46	0.04	1.58	2.17	0.38	3.52	3.19	3.05	3.57	5.54	5.20	ns
	–1	0.50	2.94	0.03	1.34	1.85	0.33	3.00	2.71	2.59	3.03	4.71	4.42	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-51: 3.3 V LVTTL / 3.3 V LVCMOS HIGH SLEW – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 3.0 V, APPLICABLE TO PRO I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.59	3.08	0.04	1.58	2.17	0.38	3.14	2.36	2.42	2.33	5.15	4.38	ns
	–1	0.50	2.62	0.03	1.34	1.85	0.33	2.67	2.01	2.06	1.98	4.38	3.72	ns
8 mA	Std.	0.59	2.53	0.04	1.58	2.17	0.38	2.58	1.89	2.74	2.89	4.59	3.90	ns
	–1	0.50	2.16	0.03	1.34	1.85	0.33	2.20	1.61	2.33	2.46	3.91	3.32	ns
12 mA	Std.	0.59	2.22	0.04	1.58	2.17	0.38	2.27	1.67	2.95	3.25	4.28	3.68	ns
	–1	0.50	1.89	0.03	1.34	1.85	0.33	1.93	1.42	2.51	2.77	3.64	3.13	ns
16 mA	Std.	0.59	2.17	0.04	1.58	2.17	0.38	2.21	1.63	3.00	3.35	4.23	3.64	ns
	–1	0.50	1.85	0.03	1.34	1.85	0.33	1.88	1.38	2.55	2.85	3.59	3.09	ns
24 mA	Std.	0.59	2.19	0.04	1.58	2.17	0.38	2.24	1.57	3.05	3.71	4.25	3.58	ns
	–1	0.50	1.87	0.03	1.34	1.85	0.33	1.90	1.33	2.59	3.16	3.61	3.05	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-52: 3.3 V LVTTL / 3.3 V LVCMOS LOW SLEW – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 3.0 V, APPLICABLE TO ADVANCED I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.54	5.11	0.04	0.91	0.38	5.21	4.33	2.38	2.21	7.22	6.34	ns
	–1	0.46	4.35	0.03	0.78	0.33	4.43	3.68	2.02	1.88	6.14	5.40	ns
6 mA	Std.	0.54	4.30	0.04	0.91	0.38	4.38	3.75	2.68	2.74	6.39	5.76	ns
	–1	0.46	3.66	0.03	0.78	0.33	3.73	3.19	2.28	2.33	5.44	4.90	ns

TABLE 2-52: 3.3 V LVTTL / 3.3 V LVCMOS LOW SLEW – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 3.0 V, APPLICABLE TO ADVANCED I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
8 mA	Std.	0.54	4.30	0.04	0.91	0.38	4.38	3.75	2.68	2.74	6.39	5.76	ns
	–1	0.46	3.66	0.03	0.78	0.33	3.73	3.19	2.28	2.33	5.44	4.90	ns
12 mA	Std.	0.54	3.68	0.04	0.91	0.38	3.75	3.32	2.89	3.07	5.76	5.33	ns
	–1	0.46	3.13	0.03	0.78	0.33	3.19	2.82	2.45	2.62	4.90	4.53	ns
16 mA	Std.	0.54	3.50	0.04	0.91	0.38	3.56	3.21	2.93	3.16	5.57	5.23	ns
	–1	0.46	2.97	0.03	0.78	0.33	3.03	2.73	2.49	2.69	4.74	4.45	ns
24 mA	Std.	0.54	3.39	0.04	0.91	0.38	3.45	3.25	2.99	3.50	5.47	5.26	ns
	–1	0.46	2.88	0.03	0.78	0.33	2.94	2.76	2.54	2.97	4.65	4.48	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-53: 3.3 V LVTTL / 3.3 V LVCMOS HIGH SLEW – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 3.0 V, APPLICABLE TO ADVANCED I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.54	2.90	0.04	0.91	0.38	2.96	2.28	2.38	2.35	4.97	4.29	ns
	–1	0.46	2.47	0.03	0.78	0.33	2.52	1.94	2.03	2.00	4.23	3.65	ns
6 mA	Std.	0.54	2.41	0.04	0.91	0.38	2.46	1.84	2.69	2.88	4.47	3.85	ns
	–1	0.46	2.05	0.03	0.78	0.33	2.09	1.57	2.29	2.45	3.80	3.28	ns
8 mA	Std.	0.54	2.41	0.04	0.91	0.38	2.46	1.84	2.69	2.88	4.47	3.85	ns
	–1	0.46	2.05	0.03	0.78	0.33	2.09	1.57	2.29	2.45	3.80	3.28	ns
12 mA	Std.	0.54	2.16	0.04	0.91	0.38	2.20	1.63	2.89	3.22	4.21	3.64	ns
	–-1	0.46	1.83	0.03	0.78	0.33	1.87	1.39	2.46	2.74	3.58	3.10	ns
16 mA	Std.	0.54	2.11	0.04	0.91	0.38	2.15	1.59	2.94	3.31	4.17	3.61	ns
	–-1	0.46	1.80	0.03	0.78	0.33	1.83	1.36	2.50	2.82	3.54	3.07	ns
24 mA	Std.	0.54	2.14	0.04	0.91	0.38	2.17	1.55	2.99	3.65	4.19	3.56	ns
	–1	0.46	1.82	0.03	0.78	0.33	1.85	1.32	2.54	3.11	3.56	3.03	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-54: 3.3 V LVTTL / 3.3 V LVCMOS LOW SLEW – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 3.0 V, APPLICABLE TO STANDARD PLUS I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.54	4.61	0.04	0.90	0.38	4.70	3.91	2.05	1.99	6.71	5.92	ns
	–1	0.46	3.92	0.03	0.77	0.33	4.00	3.32	1.74	1.69	5.71	5.04	ns
6 mA	Std.	0.54	3.80	0.04	0.90	0.38	3.87	3.40	2.32	2.47	5.88	5.41	ns
	–1	0.46	3.23	0.03	0.77	0.33	3.29	2.89	1.98	2.10	5.00	4.60	ns
8 mA	Std.	0.54	3.80	0.04	0.90	0.38	3.87	3.40	2.32	2.47	5.88	5.41	ns
	–1	0.46	3.23	0.03	0.77	0.33	3.29	2.89	1.98	2.10	5.00	4.60	ns
12 mA	Std.	0.54	3.22	0.04	0.90	0.38	3.28	3.00	2.51	2.77	5.30	5.01	ns
	–1	0.46	2.74	0.03	0.77	0.33	2.79	2.55	2.14	2.36	4.51	4.27	ns

TABLE 2-54: 3.3 V LVTTL / 3.3 V LVCMOS LOW SLEW – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 3.0 V, APPLICABLE TO STANDARD PLUS I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
16 mA	Std.	0.54	3.22	0.04	0.90	0.38	3.28	3.00	2.51	2.77	5.30	5.01	ns
	–1	0.46	2.74	0.03	0.77	0.33	2.79	2.55	2.14	2.36	4.51	4.27	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-55: 3.3 V LVTTL / 3.3 V LVCMOS HIGH SLEW – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 3.0 V, APPLICABLE TO STANDARD PLUS I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.54	2.51	0.04	0.90	0.38	2.56	2.01	2.05	2.10	4.57	4.02	ns
	–1	0.46	2.14	0.03	0.77	0.33	2.18	1.71	1.74	1.79	3.89	3.42	ns
6 mA	Std.	0.54	2.05	0.04	0.90	0.38	2.09	1.61	2.32	2.59	4.10	3.62	ns
	–1	0.46	1.74	0.03	0.77	0.33	1.78	1.37	1.97	2.20	3.49	3.08	ns
8 mA	Std.	0.54	2.05	0.04	0.90	0.38	2.09	1.61	2.32	2.59	4.10	3.62	ns
	–1	0.46	1.74	0.03	0.77	0.33	1.78	1.37	1.97	2.20	3.49	3.08	ns
12 mA	Std.	0.54	1.83	0.04	0.90	0.38	1.86	1.41	2.51	2.90	3.88	3.42	ns
	–1	0.46	1.56	0.03	0.77	0.33	1.59	1.20	2.14	2.47	3.30	2.91	ns
16 mA	Std.	0.54	1.83	0.04	0.90	0.38	1.86	1.41	2.51	2.90	3.88	3.42	ns
	–1	0.46	1.56	0.03	0.77	0.33	1.59	1.20	2.14	2.47	3.30	2.91	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

1.2 V DC Core Voltage

TABLE 2-56: 3.3 V LVTTL / 3.3 V LVCMOS LOW SLEW – APPLIES TO 1.2 V DC CORE VOLTAGE COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 3.0 V, APPLICABLE TO PRO I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.77	5.48	0.05	1.58	2.17	0.50	5.58	4.40	2.42	2.20	7.60	6.42	ns
	–1	0.66	4.66	0.04	1.34	1.85	0.43	4.75	3.75	2.06	1.87	6.46	5.46	ns
8 mA	Std.	0.77	4.48	0.05	1.58	2.17	0.50	4.56	3.76	2.73	2.76	6.57	5.78	ns
	–1	0.66	3.81	0.04	1.34	1.85	0.43	3.88	3.20	2.33	2.35	5.59	4.91	ns
12 mA	Std.	0.77	3.77	0.05	1.58	2.17	0.50	3.84	3.28	2.95	3.12	5.85	5.29	ns
	–1	0.66	3.21	0.04	1.34	1.85	0.43	3.27	2.79	2.51	2.65	4.98	4.50	ns
16 mA	Std.	0.77	3.57	0.05	1.58	2.17	0.50	3.63	3.18	2.99	3.22	5.64	5.19	ns
	–1	0.66	3.03	0.04	1.34	1.85	0.43	3.09	2.70	2.54	2.74	4.80	4.41	ns
24 mA	Std.	0.77	3.46	0.05	1.58	2.17	0.50	3.52	3.19	3.05	3.57	5.54	5.20	ns
	–1	0.66	2.94	0.04	1.34	1.85	0.43	3.00	2.71	2.59	3.03	4.71	4.42	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-57: 3.3 V LVTTL / 3.3 V LVCMOS HIGH SLEW – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 3.0 V, APPLICABLE TO PRO I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.77	3.08	0.05	1.58	2.17	0.50	3.14	2.36	2.42	2.33	5.15	4.38	ns
	–1	0.66	2.62	0.04	1.34	1.85	0.43	2.67	2.01	2.06	1.98	4.38	3.72	ns
8 mA	Std.	0.77	2.53	0.05	1.58	2.17	0.50	2.58	1.89	2.74	2.89	4.59	3.90	ns
	–1	0.66	2.16	0.04	1.34	1.85	0.43	2.20	1.61	2.33	2.46	3.91	3.32	ns
12 mA	Std.	0.77	2.22	0.05	1.58	2.17	0.50	2.27	1.67	2.95	3.25	4.28	3.68	ns
	–1	0.66	1.89	0.04	1.34	1.85	0.43	1.93	1.42	2.51	2.77	3.64	3.13	ns
16 mA	Std.	0.77	2.17	0.05	1.58	2.17	0.50	2.21	1.63	3.00	3.35	4.23	3.64	ns
	–1	0.66	1.85	0.04	1.34	1.85	0.43	1.88	1.38	2.55	2.85	3.59	3.09	ns
24 mA	Std.	0.77	2.19	0.05	1.58	2.17	0.50	2.24	1.57	3.05	3.71	4.25	3.58	ns
	–1	0.66	1.87	0.04	1.34	1.85	0.43	1.90	1.33	2.59	3.16	3.61	3.05	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-58: 3.3 V LVTTL / 3.3 V LVCMOS LOW SLEW – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 3.0 V, APPLICABLE TO ADVANCED I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.70	5.11	0.05	0.91	0.50	5.21	4.33	2.38	2.21	7.22	6.34	ns
	–1	0.60	4.35	0.04	0.78	0.43	4.43	3.68	2.02	1.88	6.14	5.40	ns
6 mA	Std.	0.70	4.30	0.05	0.91	0.50	4.38	3.75	2.68	2.74	6.39	5.76	ns
	–1	0.60	3.66	0.04	0.78	0.43	3.73	3.19	2.28	2.33	5.44	4.90	ns
8 mA	Std.	0.70	4.30	0.05	0.91	0.50	4.38	3.75	2.68	2.74	6.39	5.76	ns
	–1	0.60	3.66	0.04	0.78	0.43	3.73	3.19	2.28	2.33	5.44	4.90	ns

TABLE 2-58: 3.3 V LVTTL / 3.3 V LVCMOS LOW SLEW – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 3.0 V, APPLICABLE TO ADVANCED I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
12 mA	Std.	0.70	3.68	0.05	0.91	0.50	3.75	3.32	2.89	3.07	5.76	5.33	ns
	–1	0.60	3.13	0.04	0.78	0.43	3.19	2.82	2.45	2.62	4.90	4.53	ns
16 mA	Std.	0.70	3.50	0.05	0.91	0.50	3.56	3.21	2.93	3.16	5.57	5.23	ns
	–1	0.60	2.97	0.04	0.78	0.43	3.03	2.73	2.49	2.69	4.74	4.45	ns
24 mA	Std.	0.70	3.39	0.05	0.91	0.50	3.45	3.25	2.99	3.50	5.47	5.26	ns
	–1	0.60	2.88	0.04	0.78	0.43	2.94	2.76	2.54	2.97	4.65	4.48	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-59: 3.3 V LVTTL / 3.3 V LVCMOS HIGH SLEW – APPLIES TO 1.2 V DC CORE VOLTAGE, COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 3.0 V, APPLICABLE TO ADVANCED I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.70	2.90	0.05	0.91	0.50	2.96	2.28	2.38	2.35	4.97	4.29	ns
	–1	0.60	2.47	0.04	0.78	0.43	2.52	1.94	2.03	2.00	4.23	3.65	ns
6 mA	Std.	0.70	2.41	0.05	0.91	0.50	2.46	1.84	2.69	2.88	4.47	3.85	ns
	–1	0.60	2.05	0.04	0.78	0.43	2.09	1.57	2.29	2.45	3.80	3.28	ns
8 mA	Std.	0.70	2.41	0.05	0.91	0.50	2.46	1.84	2.69	2.88	4.47	3.85	ns
	–1	0.60	2.05	0.04	0.78	0.43	2.09	1.57	2.29	2.45	3.80	3.28	ns
12 mA	Std.	0.70	2.16	0.05	0.91	0.50	2.20	1.63	2.89	3.22	4.21	3.64	ns
	–-1	0.60	1.83	0.04	0.78	0.43	1.87	1.39	2.46	2.74	3.58	3.10	ns
16 mA	Std.	0.70	2.11	0.05	0.91	0.50	2.15	1.59	2.94	3.31	4.17	3.61	ns
	–-1	0.60	1.80	0.04	0.78	0.43	1.83	1.36	2.50	2.82	3.54	3.07	ns
24 mA	Std.	0.70	2.14	0.05	0.91	0.50	2.17	1.55	2.99	3.65	4.19	3.56	ns
	–1	0.60	1.82	0.04	0.78	0.43	1.85	1.32	2.54	3.11	3.56	3.03	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-60: 3.3 V LVTTL / 3.3 V LVCMOS LOW SLEW – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 3.0 V, APPLICABLE TO STANDARD PLUS I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.70	4.61	0.05	0.90	0.50	4.70	3.91	2.05	1.99	6.71	5.92	ns
	–1	0.60	3.92	0.04	0.77	0.43	4.00	3.32	1.74	1.69	5.71	5.04	ns
6 mA	Std.	0.70	3.80	0.05	0.90	0.50	3.87	3.40	2.32	2.47	5.88	5.41	ns
	–1	0.60	3.23	0.04	0.77	0.43	3.29	2.89	1.98	2.10	5.00	4.60	ns
8 mA	Std.	0.70	3.80	0.05	0.90	0.50	3.87	3.40	2.32	2.47	5.88	5.41	ns
	–1	0.60	3.23	0.04	0.77	0.43	3.29	2.89	1.98	2.10	5.00	4.60	ns
12 mA	Std.	0.70	3.22	0.05	0.90	0.50	3.28	3.00	2.51	2.77	5.30	5.01	ns
	–1	0.60	2.74	0.04	0.77	0.43	2.79	2.55	2.14	2.36	4.51	4.27	ns

TABLE 2-60: 3.3 V LVTTL / 3.3 V LVCMOS LOW SLEW – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 3.0 V, APPLICABLE TO STANDARD PLUS I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
16 mA	Std.	0.70	3.22	0.05	0.90	0.50	3.28	3.00	2.51	2.77	5.30	5.01	ns
	–1	0.60	2.74	0.04	0.77	0.43	2.79	2.55	2.14	2.36	4.51	4.27	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-61: 3.3 V LVTTL / 3.3 V LVCMOS HIGH SLEW – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 3.0 V, APPLICABLE TO STANDARD PLUS I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.70	2.51	0.05	0.90	0.50	2.56	2.01	2.05	2.10	4.57	4.02	ns
	–1	0.60	2.14	0.04	0.77	0.43	2.18	1.71	1.74	1.79	3.89	3.42	ns
6 mA	Std.	0.70	2.05	0.05	0.90	0.50	2.09	1.61	2.32	2.59	4.10	3.62	ns
	–1	0.60	1.74	0.04	0.77	0.43	1.78	1.37	1.97	2.20	3.49	3.08	ns
8 mA	Std.	0.70	2.05	0.05	0.90	0.50	2.09	1.61	2.32	2.59	4.10	3.62	ns
	–1	0.60	1.74	0.04	0.77	0.43	1.78	1.37	1.97	2.20	3.49	3.08	ns
12 mA	Std.	0.70	1.83	0.05	0.90	0.50	1.86	1.41	2.51	2.90	3.88	3.42	ns
	–1	0.60	1.56	0.04	0.77	0.43	1.59	1.20	2.14	2.47	3.30	2.91	ns
16 mA	Std.	0.70	1.83	0.05	0.90	0.50	1.86	1.41	2.51	2.90	3.88	3.42	ns
	–1	0.60	1.56	0.04	0.77	0.43	1.59	1.20	2.14	2.47	3.30	2.91	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.3.4.2 3.3 V LVCMOS Wide Range

TABLE 2-62: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS FOR LVCMOS 3.3 V WIDE RANGE (APPLICABLE TO PRO I/O BANKS)

3.3 V LVCMOS Wide Range	Equivalent Software Default Drive Strength Option[1]	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL	IIH
Drive Strength		Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	µA	µA	Max. mA[2]	Max. mA[2]	µA	µA
100 µA	2 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	25	27	10	10
100 µA	4 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	25	27	10	10
100 µA	6 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	51	54	10	10
100 µA	8 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	51	54	10	10
100 µA	12 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	103	109	10	10
100 µA	16 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	132	127	10	10
100 µA	24 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	268	181	10	10

Note 1: The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: Currents are measured at 85°C junction temperature.

3: All LVMCOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JDEC8-B specification.

4: Software default selection highlighted in gray.

TABLE 2-63: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS FOR LVCMOS 3.3 V WIDE RANGE (APPLICABLE TO ADVANCED I/O BANKS)

3.3 V LVCMOS Wide Range	Equivalent Software Default Drive Strength Option[1]	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL	IIH
Drive Strength		Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	µA	µA	Max. mA[2]	Max. mA[2]	µA	µA
100 µA	2 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	25	27	10	10
100 µA	4 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	25	27	10	10
100 µA	6 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	51	54	10	10
100 µA	8 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	51	54	10	10
100 µA	12 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	51	54	10	10
100 µA	16 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	103	109	10	10
100 µA	24 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	132	127	10	10

Note 1: The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: Currents are measured at 85°C junction temperature.

3: All LVMCOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JDEC8-B specification

4: Software default selection highlighted in gray.

TABLE 2-64: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS FOR LVCMOS 3.3 V WIDE RANGE (APPLICABLE TO STANDARD PLUS I/O BANKS)

3.3 V LVCMOS Wide Range	Equivalent Software Default Drive Strength Option[1]	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL	IIH
Drive Strength		Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	µA	µA	Max. mA[2]	Max. mA[2]	µA	µA
100 µA	2 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	25	27	10	10
100 µA	4 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	25	27	10	10
100 µA	6 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	51	54	10	10
100 µA	8 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	51	54	10	10
100 µA	12 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	103	109	10	10
100 µA	16 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	103	109	10	10

Note 1: The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: Currents are measured at 85°C junction temperature.

3: All LVMCOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JDEC8-B specification.

4: Software default selection highlighted in gray.

2.3.4.3 2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

TABLE 2-65: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS (APPLICABLE TO PRO I/OS)

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
4 mA	–0.3	0.7	1.7	2.7	0.7	1.7	4	4	16	18	10	10
8 mA	–0.3	0.7	1.7	2.7	0.7	1.7	8	8	32	37	10	10
12 mA	–0.3	0.7	1.7	2.7	0.7	1.7	12	12	65	74	10	10
16 mA	–0.3	0.7	1.7	2.7	0.7	1.7	16	16	83	87	10	10
24 mA	–0.3	0.7	1.7	2.7	0.7	1.7	24	24	169	124	10	10

Note 1: Currents are measured at 100°C junction temperature and maximum voltage.

2: Currents are measured at 85°C junction temperature.

3: Software default selection highlighted in gray.

TABLE 2-66: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS (APPLICABLE TO ADVANCED I/O BANKS)

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.7	1.7	2.7	0.7	1.7	2	2	16	18	10	10
4 mA	–0.3	0.7	1.7	2.7	0.7	1.7	4	4	16	18	10	10
6 mA	–0.3	0.7	1.7	2.7	0.7	1.7	6	6	32	37	10	10
8 mA	–0.3	0.7	1.7	2.7	0.7	1.7	8	8	32	37	10	10

TABLE 2-66: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS (APPLICABLE TO ADVANCED I/O BANKS)

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
12 mA	–0.3	0.7	1.7	2.7	0.7	1.7	12	12	65	74	10	10
16 mA	–0.3	0.7	1.7	2.7	0.7	1.7	16	16	83	87	10	10
24 mA	–0.3	0.7	1.7	2.7	0.7	1.7	24	24	169	124	10	10

Note 1: Currents are measured at 100°C junction temperature and maximum voltage.

2: Currents are measured at 85°C junction temperature.

3: Software default selection highlighted in gray.

TABLE 2-67: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS (APPLICABLE TO STANDARD PLUS I/O BANKS)

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.7	1.7	2.7	0.7	1.7	2	2	16	18	10	10
4 mA	–0.3	0.7	1.7	2.7	0.7	1.7	4	4	16	18	10	10
6 mA	–0.3	0.7	1.7	2.7	0.7	1.7	6	6	32	37	10	10
8 mA	–0.3	0.7	1.7	2.7	0.7	1.7	8	8	32	37	10	10
12 mA	–0.3	0.7	1.7	2.7	0.7	1.7	12	12	65	74	10	10

Note 1: Currents are measured at 100°C junction temperature and maximum voltage.

2: Currents are measured at 85°C junction temperature.

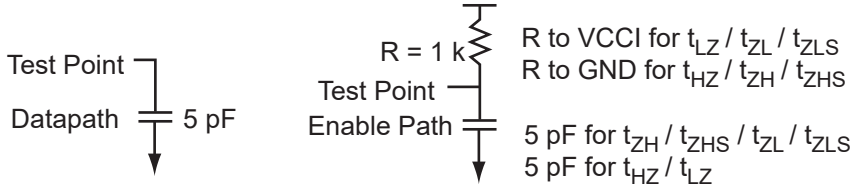
3: Software default selection highlighted in gray.

TABLE 2-68: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	2.5	1.2	5

Note: *Measuring point = Vtrip. See Table 2-27 for a complete table of trip points.

FIGURE 2-8: AC LOADING



1.5 V DC Core Voltage

TABLE 2-69: 2.5 V LVCMOS LOW SLEW – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 2.3 V, APPLICABLE TO PRO I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.59	6.24	0.04	1.86	2.31	0.38	6.36	5.30	2.45	1.98	8.37	7.31	ns
	–1	0.50	5.31	0.03	1.58	1.97	0.33	5.41	4.51	2.08	1.68	7.12	6.22	ns
8 mA	Std.	0.59	5.10	0.04	1.86	2.31	0.38	5.20	4.49	2.79	2.64	7.21	6.50	ns
	–1	0.50	4.34	0.03	1.58	1.97	0.33	4.42	3.82	2.37	2.24	6.13	5.53	ns
12 mA	Std.	0.59	4.29	0.04	1.86	2.31	0.38	4.37	3.91	3.03	3.05	6.39	5.92	ns
	–1	0.50	3.65	0.03	1.58	1.97	0.33	3.72	3.32	2.58	2.60	5.43	5.04	ns
16 mA	Std.	0.59	4.05	0.04	1.86	2.31	0.38	4.12	3.78	3.08	3.17	6.13	5.79	ns
	–1	0.50	3.44	0.03	1.58	1.97	0.33	3.51	3.22	2.62	2.70	5.22	4.93	ns
24 mA	Std.	0.59	3.94	0.04	1.86	2.31	0.38	4.01	3.80	3.15	3.60	6.03	5.81	ns
	–1	0.50	3.35	0.03	1.58	1.97	0.33	3.41	3.23	2.68	3.06	5.13	4.94	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-70: 2.5 V LVCMOS HIGH SLEW – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 2.3 V, APPLICABLE TO PRO I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.59	3.18	0.04	1.86	2.31	0.38	3.24	2.84	2.45	2.06	5.25	4.85	ns
	–1	0.50	2.71	0.03	1.58	1.97	0.33	2.76	2.42	2.08	1.75	4.47	4.13	ns
8 mA	Std.	0.59	2.61	0.04	1.86	2.31	0.38	2.65	2.19	2.79	2.73	4.67	4.20	ns
	–1	0.50	2.22	0.03	1.58	1.97	0.33	2.26	1.86	2.37	2.32	3.97	3.57	ns
12 mA	Std.	0.59	2.26	0.04	1.86	2.31	0.38	2.30	1.86	3.03	3.15	4.32	3.88	ns
	–1	0.50	1.92	0.03	1.58	1.97	0.33	1.96	1.59	2.58	2.68	3.67	3.30	ns
16 mA	Std.	0.59	2.20	0.04	1.86	2.31	0.38	2.24	1.80	3.08	3.26	4.26	3.82	ns
	–1	0.50	1.87	0.03	1.58	1.97	0.33	1.91	1.54	2.62	2.77	3.62	3.25	ns
24 mA	Std.	0.59	2.21	0.04	1.86	2.31	0.38	2.25	1.73	3.15	3.70	4.27	3.74	ns
	–1	0.50	1.88	0.03	1.58	1.97	0.33	1.92	1.47	2.68	3.14	3.63	3.18	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-71: 2.5 V LVCMOS LOW SLEW – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 2.3 V, APPLICABLE TO ADVANCED I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.54	5.79	0.04	1.18	0.38	5.90	5.18	2.41	1.98	7.91	7.19	ns
	–1	0.46	4.92	0.03	1.00	0.33	5.01	4.40	2.05	1.69	6.73	6.11	ns
6 mA	Std.	0.54	4.84	0.04	1.18	0.38	4.93	4.43	2.74	2.60	6.94	6.44	ns
	–1	0.46	4.11	0.03	1.00	0.33	4.19	3.77	2.33	2.21	5.90	5.48	ns
8 mA	Std.	0.54	4.84	0.04	1.18	0.38	4.93	4.43	2.74	2.60	6.94	6.44	ns
	–1	0.46	4.11	0.03	1.00	0.33	4.19	3.77	2.33	2.21	5.90	5.48	ns

TABLE 2-71: 2.5 V LVCMOS LOW SLEW – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 2.3 V, APPLICABLE TO ADVANCED I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
12 mA	Std.	0.54	4.13	0.04	1.18	0.38	4.21	3.92	2.97	2.99	6.22	5.93	ns
	–1	0.46	3.52	0.03	1.00	0.33	3.58	3.33	2.53	2.54	5.29	5.04	ns
16 mA	Std.	0.54	3.91	0.04	1.18	0.38	3.98	3.80	3.02	3.09	5.99	5.81	ns
	–1	0.46	3.32	0.03	1.00	0.33	3.39	3.23	2.57	2.63	5.10	4.94	ns
24 mA	Std.	0.54	3.85	0.04	1.18	0.38	3.87	3.85	3.09	3.48	5.88	5.87	ns
	–1	0.46	3.28	0.03	1.00	0.33	3.29	3.28	2.63	2.96	5.01	4.99	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-72: 2.5 V LVCMOS HIGH SLEW – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 2.3 V, APPLICABLE TO ADVANCED I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.54	2.97	0.04	1.18	0.38	3.03	2.74	2.41	2.07	5.04	4.75	ns
	–1	0.46	2.53	0.03	1.00	0.33	2.58	2.33	2.05	1.76	4.29	4.04	ns
6 mA	Std.	0.54	2.44	0.04	1.18	0.38	2.49	2.12	2.74	2.70	4.50	4.13	ns
	–1	0.46	2.08	0.03	1.00	0.33	2.12	1.80	2.33	2.30	3.83	3.51	ns
8 mA	Std.	0.54	2.44	0.04	1.18	0.38	2.49	2.12	2.74	2.70	4.50	4.13	ns
	–1	0.46	2.08	0.03	1.00	0.33	2.12	1.80	2.33	2.30	3.83	3.51	ns
12 mA	Std.	0.54	2.17	0.04	1.18	0.38	2.21	1.82	2.97	3.09	4.22	3.83	ns
	–1	0.46	1.85	0.03	1.00	0.33	1.88	1.55	2.53	2.63	3.59	3.26	ns
16 mA	Std.	0.54	2.12	0.04	1.18	0.38	2.16	1.76	3.03	3.19	4.17	3.78	ns
	–1	0.46	1.81	0.03	1.00	0.33	1.84	1.50	2.57	2.72	3.55	3.21	ns
24 mA	Std.	0.54	2.13	0.04	1.18	0.38	2.17	1.71	3.09	3.60	4.19	3.72	ns
	–1	0.46	1.81	0.03	1.00	0.33	1.85	1.45	2.63	3.06	3.56	3.16	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-73: 2.5 V LVCMOS LOW SLEW – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 2.3 V, APPLICABLE TO STANDARD PLUS I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.54	5.27	0.04	1.17	0.38	5.37	4.68	2.03	1.79	7.38	6.69	ns
	–1	0.46	4.49	0.03	0.99	0.33	4.57	3.98	1.73	1.52	6.28	5.69	ns
6 mA	Std.	0.54	4.32	0.04	1.17	0.38	4.40	4.03	2.33	2.35	6.42	6.04	ns
	–1	0.46	3.68	0.03	0.99	0.33	3.75	3.43	1.98	2.00	5.46	5.14	ns
8 mA	Std.	0.54	4.32	0.04	1.17	0.38	4.40	4.03	2.33	2.35	6.42	6.04	ns
	–1	0.46	3.68	0.03	0.99	0.33	3.75	3.43	1.98	2.00	5.46	5.14	ns
12 mA	Std.	0.54	3.66	0.04	1.17	0.38	3.73	3.56	2.54	2.71	5.74	5.57	ns
	–1	0.46	3.12	0.03	0.99	0.33	3.17	3.03	2.16	2.30	4.89	4.74	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-74: 2.5 V LVCMOS HIGH SLEW – APPLIES TO 1.5 V DC CORE VOLTAGE, COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 2.3 V, APPLICABLE TO STANDARD PLUS I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.54	2.60	0.04	1.17	0.38	2.65	2.39	2.03	1.87	4.66	4.40	ns
	–1	0.46	2.21	0.03	0.99	0.33	2.25	2.03	1.72	1.59	3.96	3.74	ns
6 mA	Std.	0.54	2.10	0.04	1.17	0.38	2.14	1.83	2.33	2.44	4.16	3.84	ns
	–1	0.46	1.79	0.03	0.99	0.33	1.82	1.56	1.98	2.07	3.54	3.27	ns
8 mA	Std.	0.54	2.10	0.04	1.17	0.38	2.14	1.83	2.33	2.44	4.16	3.84	ns
	–1	0.46	1.79	0.03	0.99	0.33	1.82	1.56	1.98	2.07	3.54	3.27	ns
12 mA	Std.	0.54	1.86	0.04	1.17	0.38	1.90	1.55	2.54	2.80	3.91	3.57	ns
	–1	0.46	1.59	0.03	0.99	0.33	1.61	1.32	2.16	2.38	3.33	3.03	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

1.2 V DC Core Voltage

TABLE 2-75: 2.5 V LVCMOS LOW SLEW – APPLIES TO 1.2 V DC CORE VOLTAGE, (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 2.3 V, APPLICABLE TO PRO I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.77	6.24	0.05	1.86	2.31	0.50	6.36	5.30	2.45	1.98	8.37	7.31	ns
	–1	0.66	5.31	0.04	1.58	1.97	0.43	5.41	4.51	2.08	1.68	7.12	6.22	ns
8 mA	Std.	0.77	5.10	0.05	1.86	2.31	0.50	5.20	4.49	2.79	2.64	7.21	6.50	ns
	–1	0.66	4.34	0.04	1.58	1.97	0.43	4.42	3.82	2.37	2.24	6.13	5.53	ns
12 mA	Std.	0.77	4.29	0.05	1.86	2.31	0.50	4.37	3.91	3.03	3.05	6.39	5.92	ns
	–1	0.66	3.65	0.04	1.58	1.97	0.43	3.72	3.32	2.58	2.60	5.43	5.04	ns
16 mA	Std.	0.77	4.05	0.05	1.86	2.31	0.50	4.12	3.78	3.08	3.17	6.13	5.79	ns
	–1	0.66	3.44	0.04	1.58	1.97	0.43	3.51	3.22	2.62	2.70	5.22	4.93	ns
24 mA	Std.	0.77	3.94	0.05	1.86	2.31	0.50	4.01	3.80	3.15	3.60	6.03	5.81	ns
	–1	0.66	3.35	0.04	1.58	1.97	0.43	3.41	3.23	2.68	3.06	5.13	4.94	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-76: 2.5 V LVCMOS HIGH SLEW – APPLIES TO 1.2 V DC CORE VOLTAGE, (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 2.3 V, APPLICABLE TO PRO I/OS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.77	3.18	0.05	1.86	2.31	0.50	3.24	2.84	2.45	2.06	5.25	4.85	ns
	–1	0.66	2.71	0.04	1.58	1.97	0.43	2.76	2.42	2.08	1.75	4.47	4.13	ns
8 mA	Std.	0.77	2.61	0.05	1.86	2.31	0.50	2.65	2.19	2.79	2.73	4.67	4.20	ns
	–1	0.66	2.22	0.04	1.58	1.97	0.43	2.26	1.86	2.37	2.32	3.97	3.57	ns
12 mA	Std.	0.77	2.26	0.05	1.86	2.31	0.50	2.30	1.86	3.03	3.15	4.32	3.88	ns
	–1	0.66	1.92	0.04	1.58	1.97	0.43	1.96	1.59	2.58	2.68	3.67	3.30	ns
16 mA	Std.	0.77	2.20	0.05	1.86	2.31	0.50	2.24	1.80	3.08	3.26	4.26	3.82	ns
	–1	0.66	1.87	0.04	1.58	1.97	0.43	1.91	1.54	2.62	2.77	3.62	3.25	ns
24 mA	Std.	0.77	2.21	0.05	1.86	2.31	0.50	2.25	1.73	3.15	3.70	4.27	3.74	ns
	–1	0.66	1.88	0.04	1.58	1.97	0.43	1.92	1.47	2.68	3.14	3.63	3.18	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-77: 2.5 V LVCMOS LOW SLEW – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 2.3 V, APPLICABLE TO ADVANCED I/OS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.70	5.79	0.05	1.18	0.50	5.90	5.18	2.41	1.98	7.91	7.19	ns
	–1	0.60	4.92	0.04	1.00	0.43	5.01	4.40	2.05	1.69	6.73	6.11	ns
6 mA	Std.	0.70	4.84	0.05	1.18	0.50	4.93	4.43	2.74	2.60	6.94	6.44	ns
	–1	0.60	4.11	0.04	1.00	0.43	4.19	3.77	2.33	2.21	5.90	5.48	ns
8 mA	Std.	0.70	4.84	0.05	1.18	0.50	4.93	4.43	2.74	2.60	6.94	6.44	ns
	–1	0.60	4.11	0.04	1.00	0.43	4.19	3.77	2.33	2.21	5.90	5.48	ns

TABLE 2-77: 2.5 V LVCMOS LOW SLEW – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 2.3 V, APPLICABLE TO ADVANCED I/OS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
12 mA	Std.	0.70	4.13	0.05	1.18	0.50	4.21	3.92	2.97	2.99	6.22	5.93	ns
	–1	0.60	3.52	0.04	1.00	0.43	3.58	3.33	2.53	2.54	5.29	5.04	ns
16 mA	Std.	0.70	3.91	0.05	1.18	0.50	3.98	3.80	3.02	3.09	5.99	5.81	ns
	–1	0.60	3.32	0.04	1.00	0.43	3.39	3.23	2.57	2.63	5.10	4.94	ns
24 mA	Std.	0.70	3.85	0.05	1.18	0.50	3.87	3.85	3.09	3.48	5.88	5.87	ns
	–1	0.60	3.28	0.04	1.00	0.43	3.29	3.28	2.63	2.96	5.01	4.99	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-78: 2.5 V LVCMOS HIGH SLEW – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 2.3 V, APPLICABLE TO ADVANCED I/OS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.70	2.97	0.05	1.18	0.50	3.03	2.74	2.41	2.07	5.04	4.75	ns
	–1	0.60	2.53	0.04	1.00	0.43	2.58	2.33	2.05	1.76	4.29	4.04	ns
6 mA	Std.	0.70	2.44	0.05	1.18	0.50	2.49	2.12	2.74	2.70	4.50	4.13	ns
	–1	0.60	2.08	0.04	1.00	0.43	2.12	1.80	2.33	2.30	3.83	3.51	ns
8 mA	Std.	0.70	2.44	0.05	1.18	0.50	2.49	2.12	2.74	2.70	4.50	4.13	ns
	–1	0.60	2.08	0.04	1.00	0.43	2.12	1.80	2.33	2.30	3.83	3.51	ns
12 mA	Std.	0.70	2.17	0.05	1.18	0.50	2.21	1.82	2.97	3.09	4.22	3.83	ns
	–1	0.60	1.85	0.04	1.00	0.43	1.88	1.55	2.53	2.63	3.59	3.26	ns
16 mA	Std.	0.70	2.12	0.05	1.18	0.50	2.16	1.76	3.03	3.19	4.17	3.78	ns
	–1	0.60	1.81	0.04	1.00	0.43	1.84	1.50	2.57	2.72	3.55	3.21	ns
24 mA	Std.	0.70	2.13	0.05	1.18	0.50	2.17	1.71	3.09	3.60	4.19	3.72	ns
	–1	0.60	1.81	0.04	1.00	0.43	1.85	1.45	2.63	3.06	3.56	3.16	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-79: 2.5 V LVCMOS LOW SLEW – APPLIES TO 1.2 V DC CORE VOLTAGE, (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 2.3 V, APPLICABLE TO STANDARD PLUS I/OS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.70	5.27	0.05	1.17	0.50	5.37	4.68	2.03	1.79	7.38	6.69	ns
	–1	0.60	4.49	0.04	0.99	0.43	4.57	3.98	1.73	1.52	6.28	5.69	ns
6 mA	Std.	0.70	4.32	0.05	1.17	0.50	4.40	4.03	2.33	2.35	6.42	6.04	ns
	–1	0.60	3.68	0.04	0.99	0.43	3.75	3.43	1.98	2.00	5.46	5.14	ns
8 mA	Std.	0.70	4.32	0.05	1.17	0.50	4.40	4.03	2.33	2.35	6.42	6.04	ns
	–1	0.60	3.68	0.04	0.99	0.43	3.75	3.43	1.98	2.00	5.46	5.14	ns
12 mA	Std.	0.70	3.66	0.05	1.17	0.50	3.73	3.56	2.54	2.71	5.74	5.57	ns
	–1	0.60	3.12	0.04	0.99	0.43	3.17	3.03	2.16	2.30	4.89	4.74	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-80: 2.5 V LVCMOS HIGH SLEW – APPLIES TO 1.2 V DC CORE VOLTAGE, (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 2.3 V, APPLICABLE TO STANDARD PLUS I/OS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.70	2.60	0.05	1.17	0.50	2.65	2.39	2.03	1.87	4.66	4.40	ns
	–1	0.60	2.21	0.04	0.99	0.43	2.25	2.03	1.72	1.59	3.96	3.74	ns
6 mA	Std.	0.70	2.10	0.05	1.17	0.50	2.14	1.83	2.33	2.44	4.16	3.84	ns
	–1	0.60	1.79	0.04	0.99	0.43	1.82	1.56	1.98	2.07	3.54	3.27	ns
8 mA	Std.	0.70	2.10	0.05	1.17	0.50	2.14	1.83	2.33	2.44	4.16	3.84	ns
	–1	0.60	1.79	0.04	0.99	0.43	1.82	1.56	1.98	2.07	3.54	3.27	ns
12 mA	Std.	0.70	1.86	0.05	1.17	0.50	1.90	1.55	2.54	2.80	3.91	3.57	ns
	–1	0.60	1.59	0.04	0.99	0.43	1.61	1.32	2.16	2.38	3.33	3.03	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.3.4.4 1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

TABLE 2-81: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS (APPLICABLE TO PRO I/OS)

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	2	2	9	11	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	4	4	17	22	10	10
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	6	6	35	44	10	10
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	8	8	45	51	10	10
12 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	12	12	91	74	10	10
16 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	16	16	91	74	10	10

Note 1: Currents are measured at 100°C junction temperature and maximum voltage.

2: Currents are measured at 85°C junction temperature.

3: Software default selection highlighted in gray.

TABLE 2-82: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS (APPLICABLE TO ADVANCED I/O BANKS)

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	2	2	9	11	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	4	4	17	22	10	10
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	6	6	35	44	10	10
8 mA	–0.3	0.35 * VCCI	0.65 * V_{CCI}	1.9	0.45	VCCI – 0.45	8	8	45	51	10	10
12 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	12	12	91	74	10	10

TABLE 2-82: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS (APPLICABLE TO ADVANCED I/O BANKS)

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
16 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	16	16	91	74	10	10

Note 1: Currents are measured at 100°C junction temperature and maximum voltage.

2: Currents are measured at 85°C junction temperature.

3: Software default selection highlighted in gray.

TABLE 2-83: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS (APPLICABLE TO STANDARD PLUS I/O I/O BANKS)

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	2	2	9	11	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	4	4	17	22	10	10
6 mA	–0.3	0.35 * VCCI	0.65 * V_{CCI}	1.9	0.45	VCCI – 0.45	6	6	35	44	10	10
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	8	8	35	44	10	10

Note 1: Currents are measured at 100°C junction temperature and maximum voltage.

2: Currents are measured at 85°C junction temperature.

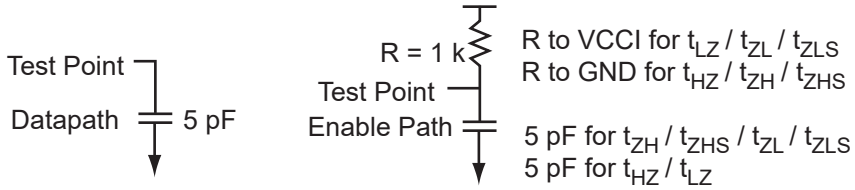
3: Software default selection highlighted in gray.

TABLE 2-84: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.8	0.9	5

Note: *Measuring point = V_{trip}. See Table 2-27 for a complete table of trip points.

FIGURE 2-9: AC LOADING



2.3.4.4.1 Timing Characteristics

1.5 V DC Core Voltage

TABLE 2-85: 1.8 V LVCMOS LOW SLEW – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 1.7 V, APPLICABLE TO PRO I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.59	8.32	0.04	1.80	2.55	0.38	8.48	6.99	2.50	1.42	10.49	9.00	ns
	–1	0.50	7.08	0.03	1.53	2.17	0.33	7.21	5.95	2.13	1.21	8.92	7.66	ns
4 mA	Std.	0.59	6.85	0.04	1.80	2.55	0.38	6.98	5.89	2.93	2.50	8.99	7.90	ns
	–1	0.50	5.83	0.03	1.53	2.17	0.33	5.94	5.01	2.49	2.12	7.65	6.72	ns
6 mA	Std.	0.59	5.81	0.04	1.80	2.55	0.38	5.92	5.13	3.21	3.02	7.93	7.15	ns
	–1	0.50	4.94	0.03	1.53	2.17	0.33	5.03	4.37	2.73	2.57	6.75	6.08	ns
8 mA	Std.	0.59	5.46	0.04	1.80	2.55	0.38	5.56	4.99	3.28	3.17	7.57	7.00	ns
	–1	0.50	4.64	0.03	1.53	2.17	0.33	4.73	4.24	2.79	2.70	6.44	5.95	ns
12 mA	Std.	0.59	5.36	0.04	1.80	2.55	0.38	5.46	4.99	3.37	3.70	7.47	7.01	ns
	–1	0.50	4.56	0.03	1.53	2.17	0.33	4.64	4.25	2.86	3.14	6.35	5.96	ns
16 mA	Std.	0.59	5.36	0.04	1.80	2.55	0.38	5.46	4.99	3.37	3.70	7.47	7.01	ns
	–1	0.50	4.56	0.03	1.53	2.17	0.33	4.64	4.25	2.86	3.14	6.35	5.96	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-86: 1.8 V LVCMOS HIGH SLEW – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 1.7 V, APPLICABLE TO PRO I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.59	3.76	0.04	1.80	2.55	0.38	3.83	3.68	2.50	1.47	5.84	5.70	ns
	–1	0.50	3.20	0.03	1.53	2.17	0.33	3.26	3.13	2.13	1.25	4.97	4.85	ns
4 mA	Std.	0.59	3.05	0.04	1.80	2.55	0.38	3.11	2.73	2.92	2.58	5.12	4.75	ns
	–1	0.50	2.59	0.03	1.53	2.17	0.33	2.64	2.33	2.49	2.19	4.35	4.04	ns
6 mA	Std.	0.59	2.61	0.04	1.80	2.55	0.38	2.66	2.27	3.21	3.12	4.67	4.28	ns
	–1	0.50	2.22	0.03	1.53	2.17	0.33	2.26	1.93	2.73	2.65	3.98	3.64	ns
8 mA	Std.	0.59	2.53	0.04	1.80	2.55	0.38	2.58	2.18	3.27	3.26	4.59	4.19	ns
	–1	0.50	2.15	0.03	1.53	2.17	0.33	2.19	1.85	2.78	2.77	3.90	3.57	ns
12 mA	Std.	0.59	2.52	0.04	1.80	2.55	0.38	2.56	2.07	3.36	3.81	4.58	4.08	ns
	–1	0.50	2.14	0.03	1.53	2.17	0.33	2.18	1.76	2.86	3.24	3.89	3.47	ns
16 mA	Std.	0.59	2.52	0.04	1.80	2.55	0.38	2.56	2.07	3.36	3.81	4.58	4.08	ns
	–1	0.50	2.14	0.03	1.53	2.17	0.33	2.18	1.76	2.86	3.24	3.89	3.47	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-87: 1.8 V LVCMOS LOW SLEW – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 1.7 V, APPLICABLE TO ADVANCED I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.54	7.77	0.04	1.18	0.38	7.92	6.80	2.50	1.44	9.93	8.81	ns
	–1	0.46	6.61	0.03	1.00	0.33	6.73	5.78	2.13	1.22	8.45	7.49	ns

TABLE 2-87: 1.8 V LVCMOS LOW SLEW – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 1.7 V, APPLICABLE TO ADVANCED I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.54	6.38	0.04	1.18	0.38	6.50	5.78	2.91	2.46	8.51	7.79	ns
	–1	0.46	5.43	0.03	1.00	0.33	5.53	4.91	2.47	2.09	7.24	6.63	ns
6 mA	Std.	0.54	5.48	0.04	1.18	0.38	5.58	5.11	3.18	2.94	7.59	7.12	ns
	–1	0.46	4.66	0.03	1.00	0.33	4.75	4.35	2.71	2.51	6.46	6.06	ns
8 mA	Std.	0.54	5.17	0.04	1.18	0.38	5.26	4.97	3.24	3.07	7.27	6.98	ns
	–1	0.46	4.40	0.03	1.00	0.33	4.48	4.23	2.76	2.61	6.19	5.94	ns
12 mA	Std.	0.54	5.06	0.04	1.18	0.38	5.15	5.03	3.34	3.55	7.17	7.04	ns
	–1	0.46	4.30	0.03	1.00	0.33	4.38	4.28	2.84	3.02	6.10	5.99	ns
16 mA	Std.	0.54	5.06	0.04	1.18	0.38	5.15	5.03	3.34	3.55	7.17	7.04	ns
	–1	0.46	4.30	0.03	1.00	0.33	4.38	4.28	2.84	3.02	6.10	5.99	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-88: 1.8 V LVCMOS HIGH SLEW – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 1.7 V, APPLICABLE TO ADVANCED I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.54	3.60	0.04	1.10	0.38	3.66	3.52	2.49	1.49	5.68	5.53	ns
	–1	0.46	3.06	0.03	0.93	0.33	3.12	3.00	2.12	1.27	4.83	4.71	ns
4 mA	Std.	0.54	2.81	0.04	1.10	0.38	2.87	2.64	2.90	2.55	4.88	4.65	ns
	–1	0.46	2.39	0.03	0.93	0.33	2.44	2.25	2.47	2.17	4.15	3.96	ns
6 mA	Std.	0.54	2.47	0.04	1.10	0.38	2.51	2.21	3.18	3.04	4.53	4.22	ns
	–1	0.46	2.10	0.03	0.93	0.33	2.14	1.88	2.70	2.59	3.85	3.59	ns
8 mA	Std.	0.54	2.40	0.04	1.10	0.38	2.45	2.13	3.24	3.17	4.46	4.14	ns
	–1	0.46	2.04	0.03	0.93	0.33	2.08	1.81	2.76	2.70	3.79	3.52	ns
12 mA	Std.	0.54	2.39	0.04	1.10	0.38	2.44	2.04	3.33	3.67	4.45	4.05	ns
	–1	0.46	2.04	0.03	0.93	0.33	2.08	1.73	2.83	3.12	3.79	3.45	ns
16 mA	Std.	0.54	2.39	0.04	1.10	0.38	2.44	2.04	3.33	3.67	4.45	4.05	ns
	–1	0.46	2.04	0.03	0.93	0.33	2.08	1.73	2.83	3.12	3.79	3.45	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-89: 1.8 V LVCMOS LOW SLEW – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 1.7 V, APPLICABLE TO STANDARD PLUS I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.54	7.21	0.04	1.17	0.38	7.35	6.14	2.03	1.32	9.36	8.16	ns
	–1	0.46	6.13	0.03	0.99	0.33	6.25	5.23	1.72	1.12	7.96	6.94	ns
4 mA	Std.	0.54	5.81	0.04	1.17	0.38	5.92	5.26	2.39	2.25	7.93	7.27	ns
	–1	0.46	4.94	0.03	0.99	0.33	5.03	4.47	2.03	1.91	6.74	6.19	ns
6 mA	Std.	0.54	4.96	0.04	1.17	0.38	5.05	4.65	2.64	2.69	7.06	6.66	ns
	–1	0.46	4.22	0.03	0.99	0.33	4.30	3.96	2.25	2.29	6.01	5.67	ns

TABLE 2-89: 1.8 V LVCMOS LOW SLEW – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 1.7 V, APPLICABLE TO STANDARD PLUS I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
8 mA	Std.	0.54	4.96	0.04	1.17	0.38	5.05	4.65	2.64	2.69	7.06	6.66	ns
	–1	0.46	4.22	0.03	0.99	0.33	4.30	3.96	2.25	2.29	6.01	5.67	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-90: 1.8 V LVCMOS HIGH SLEW – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 1.7 V, APPLICABLE TO STANDARD PLUS I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.54	3.22	0.04	1.08	0.38	3.28	3.04	2.02	1.37	5.30	5.06	ns
	–1	0.46	2.74	0.03	0.92	0.33	2.79	2.59	1.72	1.17	4.50	4.30	ns
4 mA	Std.	0.54	2.48	0.04	1.08	0.38	2.53	2.25	2.38	2.34	4.54	4.26	ns
	–1	0.46	2.11	0.03	0.92	0.33	2.15	1.92	2.03	1.99	3.86	3.63	ns
6 mA	Std.	0.54	2.17	0.04	1.08	0.38	2.21	1.86	2.64	2.79	4.22	3.87	ns
	–1	0.46	1.85	0.03	0.92	0.33	1.88	1.58	2.24	2.37	3.59	3.29	ns
8 mA	Std.	0.54	2.17	0.04	1.08	0.38	2.21	1.86	2.64	2.79	4.22	3.87	ns
	–1	0.46	1.85	0.03	0.92	0.33	1.88	1.58	2.24	2.37	3.59	3.29	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

1.2 V DC Core Voltage

TABLE 2-91: 1.8 V LVCMOS LOW SLEW – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 1.7 V, APPLICABLE TO PRO I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.77	8.32	0.05	1.80	2.55	0.50	8.48	6.99	2.50	1.42	10.49	9.00	ns
	–1	0.66	7.08	0.04	1.53	2.17	0.43	7.21	5.95	2.13	1.21	8.92	7.66	ns
4 mA	Std.	0.77	6.85	0.05	1.80	2.55	0.50	6.98	5.89	2.93	2.50	8.99	7.90	ns
	–1	0.66	5.83	0.04	1.53	2.17	0.43	5.94	5.01	2.49	2.12	7.65	6.72	ns
6 mA	Std.	0.77	5.81	0.05	1.80	2.55	0.50	5.92	5.13	3.21	3.02	7.93	7.15	ns
	–1	0.66	4.94	0.04	1.53	2.17	0.43	5.03	4.37	2.73	2.57	6.75	6.08	ns
8 mA	Std.	0.77	5.46	0.05	1.80	2.55	0.50	5.56	4.99	3.28	3.17	7.57	7.00	ns
	–1	0.66	4.64	0.04	1.53	2.17	0.43	4.73	4.24	2.79	2.70	6.44	5.95	ns
12 mA	Std.	0.77	5.36	0.05	1.80	2.55	0.50	5.46	4.99	3.37	3.70	7.47	7.01	ns
	–1	0.66	4.56	0.04	1.53	2.17	0.43	4.64	4.25	2.86	3.14	6.35	5.96	ns
16 mA	Std.	0.77	5.36	0.05	1.80	2.55	0.50	5.46	4.99	3.37	3.70	7.47	7.01	ns
	–1	0.66	4.56	0.04	1.53	2.17	0.43	4.64	4.25	2.86	3.14	6.35	5.96	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-92: 1.8 V LVCMOS HIGH SLEW – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 1.7 V, APPLICABLE TO PRO I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.77	3.76	0.05	1.80	2.55	0.50	3.83	3.68	2.50	1.47	5.84	5.70	ns
	–1	0.66	3.20	0.04	1.53	2.17	0.43	3.26	3.13	2.13	1.25	4.97	4.85	ns
4 mA	Std.	0.77	3.05	0.05	1.80	2.55	0.50	3.11	2.73	2.92	2.58	5.12	4.75	ns
	–1	0.66	2.59	0.04	1.53	2.17	0.43	2.64	2.33	2.49	2.19	4.35	4.04	ns
6 mA	Std.	0.77	2.61	0.05	1.80	2.55	0.50	2.66	2.27	3.21	3.12	4.67	4.28	ns
	–1	0.66	2.22	0.04	1.53	2.17	0.43	2.26	1.93	2.73	2.65	3.98	3.64	ns
8 mA	Std.	0.77	2.53	0.05	1.80	2.55	0.50	2.58	2.18	3.27	3.26	4.59	4.19	ns
	–1	0.66	2.15	0.04	1.53	2.17	0.43	2.19	1.85	2.78	2.77	3.90	3.57	ns
12 mA	Std.	0.77	2.52	0.05	1.80	2.55	0.50	2.56	2.07	3.36	3.81	4.58	4.08	ns
	–1	0.66	2.14	0.04	1.53	2.17	0.43	2.18	1.76	2.86	3.24	3.89	3.47	ns
16 mA	Std.	0.77	2.52	0.05	1.80	2.55	0.50	2.56	2.07	3.36	3.81	4.58	4.08	ns
	–1	0.66	2.14	0.04	1.53	2.17	0.43	2.18	1.76	2.86	3.24	3.89	3.47	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-93: 1.8 V LVCMOS LOW SLEW – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 1.7 V, APPLICABLE TO ADVANCED I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.70	7.77	0.05	1.18	0.50	7.92	6.80	2.50	1.44	9.93	8.81	ns
	–1	0.60	6.61	0.04	1.00	0.43	6.73	5.78	2.13	1.22	8.45	7.49	ns
4 mA	Std.	0.70	6.38	0.05	1.18	0.50	6.50	5.78	2.91	2.46	8.51	7.79	ns
	–1	0.60	5.43	0.04	1.00	0.43	5.53	4.91	2.47	2.09	7.24	6.63	ns

TABLE 2-93: 1.8 V LVCMOS LOW SLEW – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 1.7 V, APPLICABLE TO ADVANCED I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
6 mA	Std.	0.70	5.48	0.05	1.18	0.50	5.58	5.11	3.18	2.94	7.59	7.12	ns
	–1	0.60	4.66	0.04	1.00	0.43	4.75	4.35	2.71	2.51	6.46	6.06	ns
8 mA	Std.	0.70	5.17	0.05	1.18	0.50	5.26	4.97	3.24	3.07	7.27	6.98	ns
	–1	0.60	4.40	0.04	1.00	0.43	4.48	4.23	2.76	2.61	6.19	5.94	ns
12 mA	Std.	0.70	5.06	0.05	1.18	0.50	5.15	5.03	3.34	3.55	7.17	7.04	ns
	–1	0.60	4.30	0.04	1.00	0.43	4.38	4.28	2.84	3.02	6.10	5.99	ns
16 mA	Std.	0.70	5.06	0.05	1.18	0.50	5.15	5.03	3.34	3.55	7.17	7.04	ns
	–1	0.60	4.30	0.04	1.00	0.43	4.38	4.28	2.84	3.02	6.10	5.99	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-94: 1.8 V LVCMOS HIGH SLEW – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 1.7 V, APPLICABLE TO ADVANCED I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.70	3.60	0.05	1.10	0.50	3.66	3.52	2.49	1.49	5.68	5.53	ns
	–1	0.60	3.06	0.04	0.93	0.43	3.12	3.00	2.12	1.27	4.83	4.71	ns
4 mA	Std.	0.70	2.81	0.05	1.10	0.50	2.87	2.64	2.90	2.55	4.88	4.65	ns
	–1	0.60	2.39	0.04	0.93	0.43	2.44	2.25	2.47	2.17	4.15	3.96	ns
6 mA	Std.	0.70	2.47	0.05	1.10	0.50	2.51	2.21	3.18	3.04	4.53	4.22	ns
	–1	0.60	2.10	0.04	0.93	0.43	2.14	1.88	2.70	2.59	3.85	3.59	ns
8 mA	Std.	0.70	2.40	0.05	1.10	0.50	2.45	2.13	3.24	3.17	4.46	4.14	ns
	–1	0.60	2.04	0.04	0.93	0.43	2.08	1.81	2.76	2.70	3.79	3.52	ns
12 mA	Std.	0.70	2.39	0.05	1.10	0.50	2.44	2.04	3.33	3.67	4.45	4.05	ns
	–1	0.60	2.04	0.04	0.93	0.43	2.08	1.73	2.83	3.12	3.79	3.45	ns
16 mA	Std.	0.70	2.39	0.05	1.10	0.50	2.44	2.04	3.33	3.67	4.45	4.05	ns
	–1	0.60	2.04	0.04	0.93	0.43	2.08	1.73	2.83	3.12	3.79	3.45	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-95: 1.8 V LVCMOS LOW SLEW – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 1.7V, APPLICABLE TO STANDARD PLUS I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.70	7.21	0.05	1.17	0.50	7.35	6.14	2.03	1.32	9.36	8.16	ns
	–1	0.60	6.13	0.04	0.99	0.43	6.25	5.23	1.72	1.12	7.96	6.94	ns
4 mA	Std.	0.70	5.81	0.05	1.17	0.50	5.92	5.26	2.39	2.25	7.93	7.27	ns
	–1	0.60	4.94	0.04	0.99	0.43	5.03	4.47	2.03	1.91	6.74	6.19	ns
6 mA	Std.	0.70	4.96	0.05	1.17	0.50	5.05	4.65	2.64	2.69	7.06	6.66	ns
	–1	0.60	4.22	0.04	0.99	0.43	4.30	3.96	2.25	2.29	6.01	5.67	ns

TABLE 2-95: 1.8 V LVCMOS LOW SLEW – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 1.7V, APPLICABLE TO STANDARD PLUS I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
8 mA	Std.	0.70	4.96	0.05	1.17	0.50	5.05	4.65	2.64	2.69	7.06	6.66	ns
	–1	0.60	4.22	0.04	0.99	0.43	4.30	3.96	2.25	2.29	6.01	5.67	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-96: 1.8 V LVCMOS HIGH SLEW – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 1.7 V, APPLICABLE TO STANDARD PLUS I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.70	3.22	0.05	1.08	0.50	3.28	3.04	2.02	1.37	5.30	5.06	ns
	–1	0.60	2.74	0.04	0.92	0.43	2.79	2.59	1.72	1.17	4.50	4.30	ns
4 mA	Std.	0.70	2.48	0.05	1.08	0.50	2.53	2.25	2.38	2.34	4.54	4.26	ns
	–1	0.60	2.11	0.04	0.92	0.43	2.15	1.92	2.03	1.99	3.86	3.63	ns
6 mA	Std.	0.70	2.17	0.05	1.08	0.50	2.21	1.86	2.64	2.79	4.22	3.87	ns
	–1	0.60	1.85	0.04	0.92	0.43	1.88	1.58	2.24	2.37	3.59	3.29	ns
8 mA	Std.	0.70	2.17	0.05	1.08	0.50	2.21	1.86	2.64	2.79	4.22	3.87	ns
	–1	0.60	1.85	0.04	0.92	0.43	1.88	1.58	2.24	2.37	3.59	3.29	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.3.4.5 1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

TABLE 2-97: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS (APPLICABLE TO PRO I/OS)

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4	25	33	10	10
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	6	6	32	39	10	10
8 mA	–0.3	0.35 * VCCI	0.65 * V_{CCI}	1.575	0.25 * VCCI	0.75 * V_{CCI}	8	8	66	55	10	10
12 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	12	12	66	55	10	10

Note 1: Currents are measured at 100°C junction temperature and maximum voltage.

2: Currents are measured at 85°C junction temperature.

3: Software default selection highlighted in gray.

TABLE 2-98: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS (APPLICABLE TO ADVANCED I/O BANKS)

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4	25	33	10	10
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	6	6	32	39	10	10
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	8	8	66	55	10	10
12 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	12	12	66	55	10	10

Note 1: Currents are measured at 100°C junction temperature and maximum voltage.

2: Currents are measured at 85°C junction temperature.

3: Software default selection highlighted in gray.

TABLE 2-99: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS (APPLICABLE TO STANDARD PLUS I/O BANKS)

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4	25	33	10	10

Note 1: Currents are measured at 100°C junction temperature and maximum voltage.

2: Currents are measured at 85°C junction temperature.

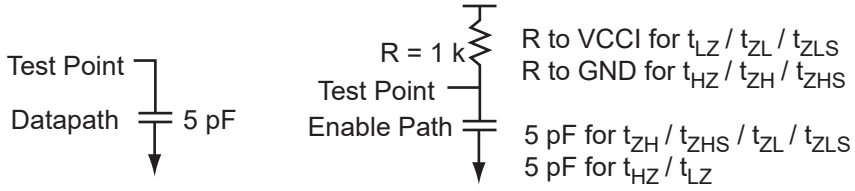
3: Software default selection highlighted in gray.

TABLE 2-100: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.5	0.75	5

Note: *Measuring point = Vtrip. See Table 2-27 for a complete table of trip points.

FIGURE 2-10: AC LOADING



1.5 V DC Core Voltage

TABLE 2-101: 1.5 V LVCMOS LOW SLEW – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 1.4 V, APPLICABLE TO PRO I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.59	8.65	0.04	1.99	2.77	0.38	8.81	7.17	3.06	2.41	10.83	9.18	ns
	–1	0.50	7.36	0.03	1.69	2.36	0.33	7.50	6.10	2.61	2.05	9.21	7.81	ns
4 mA	Std.	0.59	7.40	0.04	1.99	2.77	0.38	7.53	6.26	3.39	3.02	9.55	8.27	ns
	–1	0.50	6.29	0.03	1.69	2.36	0.33	6.41	5.33	2.89	2.57	8.12	7.04	ns
6 mA	Std.	0.59	6.94	0.04	1.99	2.77	0.38	7.07	6.09	3.46	3.19	9.08	8.11	ns
	–1	0.50	5.91	0.03	1.69	2.36	0.33	6.01	5.18	2.94	2.72	7.73	6.90	ns
8 mA	Std.	0.59	6.85	0.04	1.99	2.77	0.38	6.98	6.10	3.57	3.80	8.99	8.11	ns
	–1	0.50	5.83	0.03	1.69	2.36	0.33	5.94	5.19	3.04	3.23	7.65	6.90	ns
12 mA	Std.	0.59	6.85	0.04	1.99	2.77	0.38	6.98	6.10	3.57	3.80	8.99	8.11	ns
	–1	0.50	5.83	0.03	1.69	2.36	0.33	5.94	5.19	3.04	3.23	7.65	6.90	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-102: 1.5 V LVCMOS HIGH SLEW – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 1.4 V, APPLICABLE TO PRO I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.59	3.55	0.04	1.99	2.77	0.38	3.62	3.22	3.05	2.51	5.63	5.23	ns
	–1	0.50	3.02	0.03	1.69	2.36	0.33	3.08	2.74	2.60	2.14	4.79	4.45	ns
4 mA	Std.	0.59	3.03	0.04	1.99	2.77	0.38	3.08	2.64	3.38	3.13	5.10	4.65	ns
	–1	0.50	2.58	0.03	1.69	2.36	0.33	2.62	2.25	2.87	2.66	4.34	3.96	ns
6 mA	Std.	0.59	2.93	0.04	1.99	2.77	0.38	2.98	2.53	3.45	3.30	4.99	4.54	ns
	–1	0.50	2.49	0.03	1.69	2.36	0.33	2.54	2.15	2.93	2.81	4.25	3.86	ns
8 mA	Std.	0.59	2.90	0.04	1.99	2.77	0.38	2.95	2.39	3.57	3.94	4.96	4.41	ns
	–1	0.50	2.46	0.03	1.69	2.36	0.33	2.51	2.04	3.03	3.35	4.22	3.75	ns
12 mA	Std.	0.59	2.90	0.04	1.99	2.77	0.38	2.95	2.39	3.57	3.94	4.96	4.41	ns
	–1	0.50	2.46	0.03	1.69	2.36	0.33	2.51	2.04	3.03	3.35	4.22	3.75	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-103: 1.5 V LVCMOS LOW SLEW – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 1.4 V, APPLICABLE TO ADVANCED I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.54	8.00	0.04	1.18	0.38	8.15	7.01	3.06	2.38	10.16	9.02	ns
	–1	0.46	6.80	0.03	1.00	0.33	6.93	5.96	2.60	2.02	8.64	7.68	ns
4 mA	Std.	0.54	6.91	0.04	1.18	0.38	7.04	6.21	3.37	2.94	9.05	8.22	ns
	–1	0.46	5.88	0.03	1.00	0.33	5.99	5.28	2.87	2.50	7.70	7.00	ns

TABLE 2-103: 1.5 V LVCMOS LOW SLEW – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 1.4 V, APPLICABLE TO ADVANCED I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
6 mA	Std.	0.54	6.51	0.04	1.18	0.38	6.63	6.05	3.45	3.09	8.64	8.06	ns
	–1	0.46	5.54	0.03	1.00	0.33	5.64	5.15	2.93	2.63	7.35	6.86	ns
8 mA	Std.	0.54	6.41	0.04	1.18	0.38	6.53	6.11	3.56	3.64	8.54	8.12	ns
	–1	0.46	5.45	0.03	1.00	0.33	5.56	5.20	3.03	3.10	7.27	6.91	ns
12 mA	Std.	0.54	6.41	0.04	1.18	0.38	6.53	6.11	3.56	3.64	8.54	8.12	ns
	–1	0.46	5.45	0.03	1.00	0.33	5.56	5.20	3.03	3.10	7.27	6.91	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-104: 1.5 V LVCMOS HIGH SLEW – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 1.4 V, APPLICABLE TO ADVANCED I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.54	3.60	0.04	1.10	0.38	3.66	3.52	2.49	1.49	5.68	5.53	ns
	–1	0.46	3.06	0.03	0.93	0.33	3.12	3.00	2.12	1.27	4.83	4.71	ns
4 mA	Std.	0.54	2.81	0.04	1.10	0.38	2.87	2.64	2.90	2.55	4.88	4.65	ns
	–1	0.46	2.39	0.03	0.93	0.33	2.44	2.25	2.47	2.17	4.15	3.96	ns
6 mA	Std.	0.54	2.47	0.04	1.10	0.38	2.51	2.21	3.18	3.04	4.53	4.22	ns
	–1	0.46	2.10	0.03	0.93	0.33	2.14	1.88	2.70	2.59	3.85	3.59	ns
8 mA	Std.	0.54	2.40	0.04	1.10	0.38	2.45	2.13	3.24	3.17	4.46	4.14	ns
	–1	0.46	2.04	0.03	0.93	0.33	2.08	1.81	2.76	2.70	3.79	3.52	ns
12 mA	Std.	0.54	2.39	0.04	1.10	0.38	2.44	2.04	3.33	3.67	4.45	4.05	ns
	–1	0.46	2.04	0.03	0.93	0.33	2.08	1.73	2.83	3.12	3.79	3.45	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-105: 1.5 V LVCMOS LOW SLEW – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 1.4 V, APPLICABLE TO STANDARD PLUS I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.54	7.32	0.04	1.17	0.38	7.45	6.38	2.44	2.18	9.46	8.40	ns
	–1	0.46	6.22	0.03	0.99	0.33	6.34	5.43	2.08	1.86	8.05	7.14	ns
4 mA	Std.	0.54	6.29	0.04	1.17	0.38	6.40	5.65	2.73	2.70	8.42	7.67	ns
	–1	0.46	5.35	0.03	0.99	0.33	5.45	4.81	2.33	2.29	7.16	6.52	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-106: 1.5 V LVCMOS HIGH SLEW – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 1.4 V, APPLICABLE TO STANDARD PLUS I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.54	2.90	0.04	1.28	0.38	2.95	2.63	2.44	2.29	4.97	4.64	ns
	–1	0.46	2.47	0.03	1.09	0.33	2.51	2.24	2.07	1.95	4.23	3.95	ns
4 mA	Std.	0.54	2.52	0.04	1.28	0.38	2.57	2.14	2.73	2.82	4.58	4.15	ns
	–1	0.46	2.15	0.03	1.09	0.33	2.19	1.82	2.32	2.40	3.90	3.53	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

1.2 V DC Core Voltage

TABLE 2-107: 1.5 V LVCMOS LOW SLEW – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 1.4 V, APPLICABLE TO PRO I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.77	8.65	0.05	1.99	2.77	0.50	8.81	7.17	3.06	2.41	10.83	9.18	ns
	–1	0.66	7.36	0.04	1.69	2.36	0.43	7.50	6.10	2.61	2.05	9.21	7.81	ns
4 mA	Std.	0.77	7.40	0.05	1.99	2.77	0.50	7.53	6.26	3.39	3.02	9.55	8.27	ns
	–1	0.66	6.29	0.04	1.69	2.36	0.43	6.41	5.33	2.89	2.57	8.12	7.04	ns
6 mA	Std.	0.77	6.94	0.05	1.99	2.77	0.50	7.07	6.09	3.46	3.19	9.08	8.11	ns
	–1	0.66	5.91	0.04	1.69	2.36	0.43	6.01	5.18	2.94	2.72	7.73	6.90	ns
8 mA	Std.	0.77	6.85	0.05	1.99	2.77	0.50	6.98	6.10	3.57	3.80	8.99	8.11	ns
	–1	0.66	5.83	0.04	1.69	2.36	0.43	5.94	5.19	3.04	3.23	7.65	6.90	ns
12 mA	Std.	0.77	6.85	0.05	1.99	2.77	0.50	6.98	6.10	3.57	3.80	8.99	8.11	ns
	–1	0.66	5.83	0.04	1.69	2.36	0.43	5.94	5.19	3.04	3.23	7.65	6.90	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-108: 1.5 V LVCMOS HIGH SLEW – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 1.4 V, APPLICABLE TO PRO I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.77	3.55	0.05	1.99	2.77	0.50	3.62	3.22	3.05	2.51	5.63	5.23	ns
	–1	0.66	3.02	0.04	1.69	2.36	0.43	3.08	2.74	2.60	2.14	4.79	4.45	ns
4 mA	Std.	0.77	3.03	0.05	1.99	2.77	0.50	3.08	2.64	3.38	3.13	5.10	4.65	ns
	–1	0.66	2.58	0.04	1.69	2.36	0.43	2.62	2.25	2.87	2.66	4.34	3.96	ns
6 mA	Std.	0.77	2.93	0.05	1.99	2.77	0.50	2.98	2.53	3.45	3.30	4.99	4.54	ns
	–1	0.66	2.49	0.04	1.69	2.36	0.43	2.54	2.15	2.93	2.81	4.25	3.86	ns
8 mA	Std.	0.77	2.90	0.05	1.99	2.77	0.50	2.95	2.39	3.57	3.94	4.96	4.41	ns
	–1	0.66	2.46	0.04	1.69	2.36	0.43	2.51	2.04	3.03	3.35	4.22	3.75	ns
12 mA	Std.	0.77	2.90	0.05	1.99	2.77	0.50	2.95	2.39	3.57	3.94	4.96	4.41	ns
	–1	0.66	2.46	0.04	1.69	2.36	0.43	2.51	2.04	3.03	3.35	4.22	3.75	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-109: 1.5 V LVCMOS LOW SLEW – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 1.4 V, APPLICABLE TO ADVANCED I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.70	8.00	0.05	1.18	0.50	8.15	7.01	3.06	2.38	10.16	9.02	ns
	–1	0.60	6.80	0.04	1.00	0.43	6.93	5.96	2.60	2.02	8.64	7.68	ns
4 mA	Std.	0.70	6.91	0.05	1.18	0.50	7.04	6.21	3.37	2.94	9.05	8.22	ns
	–1	0.60	5.88	0.04	1.00	0.43	5.99	5.28	2.87	2.50	7.70	7.00	ns
6 mA	Std.	0.70	6.51	0.05	1.18	0.50	6.63	6.05	3.45	3.09	8.64	8.06	ns
	–1	0.60	5.54	0.04	1.00	0.43	5.64	5.15	2.93	2.63	7.35	6.86	ns

TABLE 2-109: 1.5 V LVCMOS LOW SLEW – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 1.4 V, APPLICABLE TO ADVANCED I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
8 mA	Std.	0.70	6.41	0.05	1.18	0.50	6.53	6.11	3.56	3.64	8.54	8.12	ns
	–1	0.60	5.45	0.04	1.00	0.43	5.56	5.20	3.03	3.10	7.27	6.91	ns
12 mA	Std.	0.70	6.41	0.05	1.18	0.50	6.53	6.11	3.56	3.64	8.54	8.12	ns
	–1	0.60	5.45	0.04	1.00	0.43	5.56	5.20	3.03	3.10	7.27	6.91	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-110: 1.5 V LVCMOS HIGH SLEW – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 1.4 V, APPLICABLE TO ADVANCED I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.70	3.26	0.05	1.30	0.50	3.32	3.11	3.05	2.49	5.33	5.12	ns
	–1	0.60	2.77	0.04	1.10	0.43	2.82	2.64	2.59	2.12	4.53	4.36	ns
4 mA	Std.	0.70	2.84	0.05	1.30	0.50	2.89	2.57	3.37	3.06	4.90	4.59	ns
	–1	0.60	2.41	0.04	1.10	0.43	2.46	2.19	2.86	2.60	4.17	3.90	ns
6 mA	Std.	0.70	2.76	0.05	1.30	0.50	2.81	2.47	3.44	3.21	4.82	4.48	ns
	–1	0.60	2.35	0.04	1.10	0.43	2.39	2.10	2.92	2.73	4.10	3.81	ns
8 mA	Std.	0.70	2.74	0.05	1.30	0.50	2.79	2.36	3.55	3.78	4.80	4.37	ns
	–1	0.60	2.33	0.04	1.10	0.43	2.37	2.01	3.02	3.22	4.08	3.72	ns
12 mA	Std.	0.70	2.74	0.05	1.30	0.50	2.79	2.36	3.55	3.78	4.80	4.37	ns
	–1	0.60	2.33	0.04	1.10	0.43	2.37	2.01	3.02	3.22	4.08	3.72	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-111: 1.5 V LVCMOS LOW SLEW – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 1.4 V, APPLICABLE TO STANDARD PLUS I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.70	7.32	0.05	1.17	0.50	7.45	6.38	2.44	2.18	9.46	8.40	ns
	–1	0.60	6.22	0.04	0.99	0.43	6.34	5.43	2.08	1.86	8.05	7.14	ns
4 mA	Std.	0.70	6.29	0.05	1.17	0.50	6.40	5.65	2.73	2.70	8.42	7.67	ns
	–1	0.60	5.35	0.04	0.99	0.43	5.45	4.81	2.33	2.29	7.16	6.52	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-112: 1.5 V LVCMOS HIGH SLEW – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 1.4 V, APPLICABLE TO STANDARD PLUS I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.70	2.90	0.05	1.28	0.50	2.95	2.63	2.44	2.29	4.97	4.64	ns
	–1	0.60	2.47	0.04	1.09	0.43	2.51	2.24	2.07	1.95	4.23	3.95	ns

TABLE 2-112: 1.5 V LVCMOS HIGH SLEW – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 1.4 V, APPLICABLE TO STANDARD PLUS I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.70	2.52	0.05	1.28	0.50	2.57	2.14	2.73	2.82	4.58	4.15	ns
	–1	0.60	2.15	0.04	1.09	0.43	2.19	1.82	2.32	2.40	3.90	3.53	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.3.4.6 1.2 V LVCMOS (JESD8-12A)

Low-Voltage CMOS for 1.2 V complies with the LVCMOS standard JESD8-12A for general purpose 1.2 V applications. It uses a 1.2 V input buffer and a push-pull output buffer.

TABLE 2-113: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS (APPLICABLE TO ADVANCED I/O BANKS)

1.2 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH[1]	IOSL[1]	IIL[2]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA	Max. mA	µA	µA
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	2	2	TBD	TBD	10	10

Note 1: Currents are measured at 100°C junction temperature and maximum voltage.

2: Currents are measured at 85°C junction temperature.

3: Software default selection highlighted in gray.

TABLE 2-114: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS (APPLICABLE TO STANDARD PLUS I/O BANKS)

1.2 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH[1]	IOSL[1]	IIL[2]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA	Max. mA	µA	µA
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	2	2	TBD	TBD	10	10

Note 1: Currents are measured at 100°C junction temperature and maximum voltage.

2: Currents are measured at 85°C junction temperature.

3: Software default selection highlighted in gray.

TABLE 2-115: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS (APPLICABLE TO STANDARD I/O BANKS)

1.2 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH[1]	IOSL[1]	IIL[2]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA	Max. mA	µA	µA
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	2	2	TBD	TBD	10	10

Note 1: Currents are measured at 100°C junction temperature and maximum voltage.

2: Currents are measured at 85°C junction temperature.

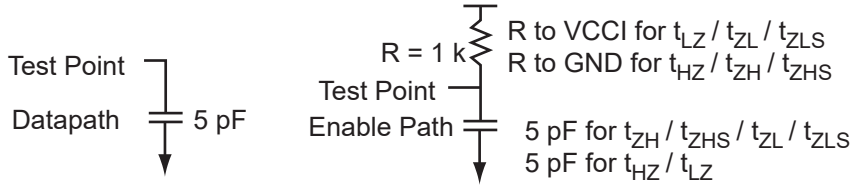
3: Software default selection highlighted in gray.

TABLE 2-116: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.2	0.6	5

Note: *Measuring point = Vtrip. See Table 2-27 for a complete table of trip points.

FIGURE 2-11: AC LOADING



1.2 V DC Core Voltage

TABLE 2-117: 1.2 V LVCMOS LOW SLEW (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 1.4 V, APPLICABLE TO PRO I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.77	11.80	0.05	2.38	3.52	0.50	10.97	8.61	4.79	4.38	12.91	10.55	ns
	–1	0.66	10.04	0.04	2.02	2.99	0.43	9.33	7.32	4.08	3.72	10.98	8.97	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-118: 1.2 V LVCMOS HIGH SLEW (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 1.4 V, APPLICABLE TO PRO I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.77	4.84	0.05	2.38	3.52	0.50	4.50	3.96	4.78	4.51	6.44	5.90	ns
	–1	0.66	4.12	0.04	2.02	2.99	0.43	3.83	3.37	4.06	3.84	5.48	5.02	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-119: 1.2 V LVCMOS HIGH SLEW (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 1.14 V

Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.70	8.77	0.05	1.82	0.50	6.17	5.45	2.80	2.77	8.11	7.39	ns
	–1	0.60	7.46	0.04	1.55	0.43	5.25	4.63	2.39	2.35	6.90	6.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-120: 1.2 V LVCMOS HIGH SLEW (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 1.14 V, APPLICABLE TO ADVANCED I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.70	3.73	0.05	1.82	0.50	2.48	2.06	2.80	2.89	4.42	4.00	ns
	–1	0.60	3.17	0.04	1.55	0.43	2.11	1.76	2.38	2.46	3.76	3.41	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-121: 1.2 V LVCMOS HIGH SLEW (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 1.14 V, APPLICABLE TO STANDARD PLUS I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.70	9.67	0.05	1.83	0.50	6.78	5.99	4.08	4.57	8.72	7.93	ns
	–1	0.60	8.23	0.04	1.56	0.43	5.77	5.09	3.47	3.88	7.42	6.74	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-122: 1.2 V LVCMOS HIGH SLEW (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 1.14 V, APPLICABLE TO STANDARD PLUS I/O BANKS)

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.70	4.17	0.05	1.83	0.50	2.79	2.48	4.23	4.55	4.73	4.42	ns
	–1	0.60	3.54	0.04	1.56	0.43	2.37	2.11	3.60	3.87	4.02	3.76	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.3.4.7 1.2 V LVCMOS Wide Range

TABLE 2-123: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS FOR LVCMOS 1.2 V WIDE RANGE (APPLICABLE TO PRO I/O BANKS)

1.2 V LVCMOS Wide Range	Equivalent Software Default Drive Strength Option[1]	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL	IIH
Drive Strength		Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	µA	µA	Max. mA[2]	Max. mA[2]	µA	µA
100 µA	2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	100	100	20	26	10	10

Note 1: The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: Currents are measured at 85°C junction temperature.

3: All LVMCOS 1.2 V software macros support LVCMOS 3.3 V wide range as specified in the JDEC8-12 specification.

4: Software default selection highlighted in gray.

TABLE 2-124: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS FOR LVCMOS 1.2 WIDE RANGE (APPLICABLE TO ADVANCED I/O BANKS)

1.2 V LVCMOS Wide Range	Equivalent Software Default Drive Strength Option[1]	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL	IIH
Drive Strength		Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	µA	µA	Max. mA[2]	Max. mA[2]	µA	µA
100 µA	2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	100	100	20	26	10	10

Note 1: The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: Currents are measured at 85°C junction temperature.

3: All LVMCOS 1.2 V software macros support LVCMOS 3.3 V wide range as specified in the JDEC8-12 specification.

4: Software default selection highlighted in gray.

TABLE 2-125: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS FOR LVCMOS 1.2 V WIDE RANGE (APPLICABLE TO STANDARD PLUS I/O BANKS)

1.2 V LVCMOS Wide Range	Equivalent Software Default Drive Strength Option[1]	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL	IIH
Drive Strength		Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	µA	µA	Max. mA[2]	Max. mA[2]	µA	µA
100 µA	2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	100	100	20	26	10	10

Note 1: The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: Currents are measured at 85°C junction temperature.

3: All LVMCOS 1.2 V software macros support LVCMOS 3.3 V wide range as specified in the JDEC8-12 specification

4: Software default selection highlighted in gray.

2.3.4.8 3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

TABLE 2-126: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

3.3 V PCI/PCI-X	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
Per PCI specification	Per PCI curves										10	10

Note 1: Currents are measured at 100°C junction temperature and maximum voltage.

2: Currents are measured at 85°C junction temperature.

AC loadings are defined per the PCI/PCI-X specifications for the database; Microchip loadings for enable path characterization are described in Figure 2-12.

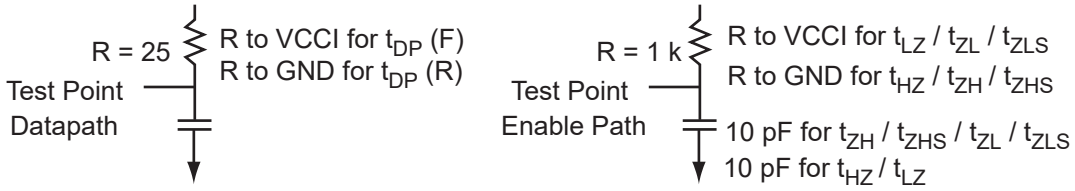
AC loadings are defined per PCI/PCI-X specifications for the datapath; Microchip loading for tristate is described in Table 2-127.

TABLE 2-127: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	3.3	0.285 * VCCI for $t_{DP(R)}$ 0.615 * VCCI for $t_{DP(F)}$	10

Note: *Measuring point = Vtrip. See Table 2-27 for a complete table of trip points.

FIGURE 2-12: AC LOADING



1.5 V DC Core Voltage

TABLE 2-128: 3.3 V PCI/PCI-X – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 3.0 V, APPLICABLE TO PRO I/O BANKS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.59	2.52	0.04	2.47	3.33	0.38	2.57	1.80	2.95	3.25	4.58	3.81	ns
–1	0.50	2.15	0.03	2.10	2.84	0.33	2.19	1.53	2.51	2.77	3.90	3.24	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-129: 3.3 V PCI/PCI-X – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE V_{CC} = 1.425 V, WORST-CASE V_{CCI} = 3.0 V, APPLICABLE TO ADVANCED I/O BANKS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.54	2.41	0.04	0.78	0.38	2.46	1.76	2.89	3.22	4.47	3.77	ns	0.54
–1	0.46	2.05	0.03	0.66	0.33	2.09	1.49	2.46	2.74	3.80	3.21	ns	0.46

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-130: 3.3 V PCI/PCI-X – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE V_{CC} = 1.425 V, WORST-CASE V_{CCI} = 3.0 V, APPLICABLE TO STANDARD PLUS I/O BANKS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.54	2.08	0.04	0.77	0.38	2.12	1.53	2.51	2.90	4.13	3.55	ns	0.54
–1	0.46	1.77	0.03	0.65	0.33	1.80	1.31	2.14	2.47	3.51	3.02	ns	0.46

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

1.2 V DC Core Voltage

TABLE 2-131: 3.3 V PCI/PCI-X – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 3.0 V, APPLICABLE TO PRO I/O BANKS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.77	2.52	0.05	2.47	3.33	0.50	2.57	1.80	2.95	3.25	4.58	3.81	ns
–1	0.66	2.15	0.04	2.10	2.84	0.43	2.19	1.53	2.51	2.77	3.90	3.24	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-132: 3.3 V PCI/PCI-X – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 3.0 V, APPLICABLE TO ADVANCED I/O BANKS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.70	2.41	0.05	0.78	0.50	2.46	1.76	2.89	3.22	4.47	3.77	0.73	ns
–1	0.60	2.05	0.04	0.66	0.43	2.09	1.49	2.46	2.74	3.80	3.21	0.62	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-133: 3.3 V PCI/PCI-X – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 3.0 V, APPLICABLE TO STANDARD PLUS I/O BANKS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.70	2.08	0.05	0.77	0.50	2.12	1.53	2.51	2.90	4.13	3.55	0.73	ns
–1	0.60	1.77	0.04	0.65	0.43	1.80	1.31	2.14	2.47	3.51	3.02	0.62	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.3.5 VOLTAGE-REFERENCED I/O CHARACTERISTICS

2.3.5.1 3.3 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The V_{CCI} pin should be connected to 3.3 V.

TABLE 2-134: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

3.3 V GTL	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
20 mA[3]	–0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	–	20	20	268	181	10	10

Note 1: Currents are measured at 100°C junction temperature and maximum voltage.

2: Currents are measured at 85°C junction temperature.

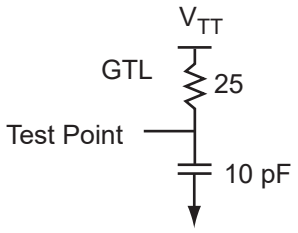
3: Output drive strength is below JEDEC specification.

TABLE 2-135: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.05	VREF + 0.05	0.8	0.8	1.2	10

Note: *Measuring point = Vtrip. See Table 2-16 for a complete table of trip points.

FIGURE 2-13: AC LOADING



2.3.5.1.1 Timing Characteristics

TABLE 2-136: 3.3 V GTL – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 3.0 V VREF = 0.8 V, APPLICABLE TO PRO I/O BANKS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.59	1.87	0.04	2.12	0.38	1.83	1.87			3.85	3.88	ns
–1	0.50	1.59	0.03	1.80	0.33	1.56	1.59			3.27	3.30	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-137: 3.3 V GTL – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 3.0 V VREF = 0.8 V, APPLICABLE TO PRO I/OS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.77	1.87	0.05	2.12	0.50	1.83	1.87			3.85	3.88	ns
–1	0.66	1.59	0.04	1.80	0.43	1.56	1.59			3.27	3.30	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.3.5.2 2.5 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The V_{CCI} pin should be connected to 2.5 V.

TABLE 2-138: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

2.5 GTL	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
20 mA[3]	–0.3	VREF – 0.05	VREF + 0.05	2.7	0.4	–	20	20	169	124	10	10

Note 1: Currents are measured at 100°C junction temperature and maximum voltage.

2: Currents are measured at 85°C junction temperature.

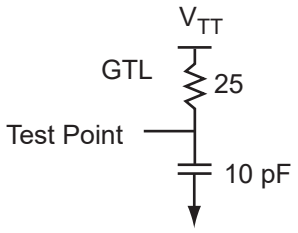
3: Output drive strength is below JEDEC specification.

TABLE 2-139: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.05	VREF + 0.05	0.8	0.8	1.2	10

Note: *Measuring point = Vtrip. See Table 2-16 for a complete table of trip points.

FIGURE 2-14: AC LOADING



2.3.5.2.1 Timing Characteristics

TABLE 2-140: 2.5 V GTL – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 3.0 V VREF = 0.8 V, APPLICABLE TO PRO I/O BANKS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.59	1.92	0.04	2.05	0.38	1.95	1.92			3.96	3.93	ns
–1	0.50	1.63	0.03	1.75	0.33	1.66	1.63			3.37	3.34	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-141: 2.5 V GTL – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 3.0 V VREF = 0.8 V, APPLICABLE TO PRO I/O BANKS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.77	1.92	0.05	2.05	0.50	1.95	1.92			3.96	3.93	ns
–1	0.66	1.63	0.04	1.75	0.43	1.66	1.63			3.37	3.34	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.3.5.3 3.3 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The V_{CCI} pin should be connected to 3.3 V.

TABLE 2-142: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

3.3 V GTL+	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
35 mA	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	35	35	268	181	10	10

Note 1: Currents are measured at 100°C junction temperature and maximum voltage.

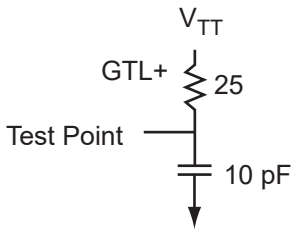
2: Currents are measured at 85°C junction temperature.

TABLE 2-143: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.1	VREF + 0.1	1.0	1.0	1.5	10

Note: *Measuring point = Vtrip. See Table 2-16 for a complete table of trip points.

FIGURE 2-15: AC LOADING



2.3.5.3.1 Timing Characteristics

TABLE 2-144: 3.3 V GTL+ – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 3.0 V VREF = 1.0 V, APPLICABLE TO PRO I/O BANKS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.59	1.85	0.04	2.12	0.38	1.88	1.85			3.90	3.86	ns
–1	0.50	1.57	0.03	1.80	0.33	1.60	1.57			3.31	3.29	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-145: 3.3 V GTL+ – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 3.0 V VREF = 1.0 V, APPLICABLE TO PRO I/O BANKS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.77	1.85	0.05	2.12	0.50	1.88	1.85			3.90	3.86	ns
–1	0.66	1.57	0.04	1.80	0.43	1.60	1.57			3.31	3.29	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.3.5.4 2.5 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The V_{CCI} pin should be connected to 2.5 V.

TABLE 2-146: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

2.5 V GTL+	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
33 mA	–0.3	VREF – 0.1	VREF + 0.1	2.7	0.6	–	33	33	169	124	10	10

Note 1: Currents are measured at 100°C junction temperature and maximum voltage.

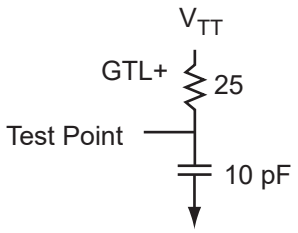
2: Currents are measured at 85°C junction temperature.

TABLE 2-147: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.1	VREF + 0.1	1.0	1.0	1.5	10

Note: *Measuring point = Vtrip. See Table 2-16 for a complete table of trip points.

FIGURE 2-16: AC LOADING



2.3.5.4.1 Timing Characteristics

TABLE 2-148: 2.5 V GTL+ – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 2.3 V VREF = 1.0 V, APPLICABLE TO PRO I/O BANKS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.59	1.99	0.04	2.05	0.38	2.02	1.89			4.03	3.90	ns
–1	0.50	1.69	0.03	1.75	0.33	1.72	1.61			3.43	3.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-16 for derating values.

TABLE 2-149: 2.5 V GTL+ – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 2.3 V VREF = 1.0 V, APPLICABLE TO PRO I/O BANKS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.77	1.99	0.05	2.05	0.50	2.02	1.89			4.03	3.90	ns
–1	0.66	1.69	0.04	1.75	0.43	1.72	1.61			3.43	3.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-16 for derating values.

2.3.5.5 HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

TABLE 2-150: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

HSTL Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
8 mA	–0.3	VREF – 0.1	VREF + 0.1	1.575	0.4	VCCI – 0.4	8	8	32	39	10	10

Note 1: Currents are measured at 100°C junction temperature and maximum voltage.

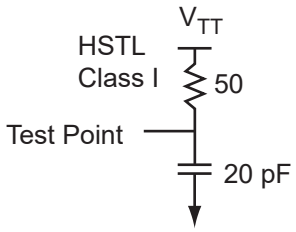
2: Currents are measured at 85°C junction temperature.

TABLE 2-151: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.1	VREF + 0.1	0.75	0.75	0.75	20

Note: *Measuring point = Vtrip. See Table 2-16 for a complete table of trip points.

FIGURE 2-17: AC LOADING



2.3.5.5.1 Timing Characteristics

TABLE 2-152: HSTL CLASS I – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 1.4 V VREF = 0.75 V, APPLICABLE TO PRO I/O BANKS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.59	2.86	0.04	2.50	0.38	2.91	2.83			4.93	4.84	ns
–1	0.50	2.43	0.03	2.12	0.33	2.48	2.41			4.19	4.12	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-153: HSTL CLASS I – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 1.4 V VREF = 0.75 V, APPLICABLE TO PRO I/O BANKS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.77	2.86	0.05	2.50	0.50	2.91	2.83			4.93	4.84	ns
–1	0.66	2.43	0.04	2.12	0.43	2.48	2.41			4.19	4.12	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.3.5.6 HSTL Class II

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

TABLE 2-154: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

HSTL Class II	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
15 mA[3]	–0.3	VREF – 0.1	VREF + 0.1	1.575	0.4	VCCI – 0.4	15	15	66	55	10	10

Note 1: Currents are measured at 100°C junction temperature and maximum voltage.

2: Currents are measured at 85°C junction temperature.

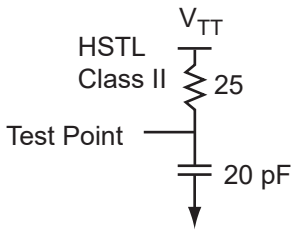
3: Output drive strength is below JEDEC specification.

TABLE 2-155: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.1	VREF + 0.1	0.75	0.75	0.75	20

Note: *Measuring point = Vtrip. See Table 2-16 for a complete table of trip points.

FIGURE 2-18: AC LOADING



2.3.5.6.1 Timing Characteristics

TABLE 2-156: HSTL CLASS II – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 1.4 V VREF = 0.75 V, APPLICABLE TO PRO I/O BANKS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.59	2.72	0.04	2.50	0.38	2.77	2.44			4.78	4.45	ns
–1	0.50	2.32	0.03	2.12	0.33	2.36	2.08			4.07	3.79	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-157: HSTL CLASS II – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 1.4 V VREF = 0.75 V, APPLICABLE TO PRO I/O BANKS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.77	2.72	0.05	2.50	0.50	2.77	2.44			4.78	4.45	ns
–1	0.66	2.32	0.04	2.12	0.43	2.36	2.08			4.07	3.79	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.3.5.7 SSTL2 Class I

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

TABLE 2-158: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

SSTL2 Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
15 mA	–0.3	VREF – 0.2	VREF + 0.2	2.7	0.54	VCCI – 0.62	15	15	83	87	10	10

Note 1: Currents are measured at 100°C junction temperature and maximum voltage.

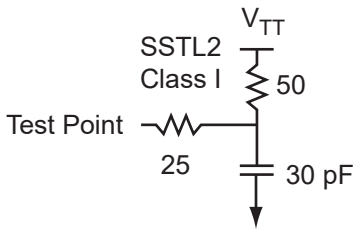
2: Currents are measured at 85°C junction temperature.

TABLE 2-159: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.25	1.25	1.25	30

Note: *Measuring point = Vtrip. See Table 2-16 for a complete table of trip points.

FIGURE 2-19: AC LOADING



2.3.5.7.1 Timing Characteristics

TABLE 2-160: SSTL2 CLASS I – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 2.3 V VREF = 1.25 V, APPLICABLE TO PRO I/OS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.59	1.91	0.04	1.89	0.38	1.95	1.66			1.95	1.66	ns
–1	0.50	1.63	0.03	1.61	0.33	1.66	1.41			1.66	1.41	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-161: SSTL2 CLASS I – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 2.3 V VREF = 1.25 V, APPLICABLE TO PRO I/O BANKS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.77	1.91	0.05	1.89	0.50	1.95	1.66			1.95	1.66	ns
–1	0.66	1.63	0.04	1.61	0.43	1.66	1.41			1.66	1.41	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.3.5.8 SSTL2 Class II

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

TABLE 2-162: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

SSTL2 Class II	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
18 mA	–0.3	VREF – 0.2	VREF + 0.2	2.7	0.35	VCCI – 0.43	18	18	169	124	10	10

Note 1: Currents are measured at 100°C junction temperature and maximum voltage.

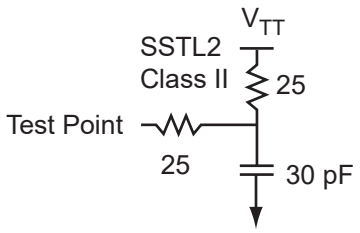
2: Currents are measured at 85°C junction temperature.

TABLE 2-163: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.25	1.25	1.25	30

Note: *Measuring point = Vtrip. See Table 2-16 for a complete table of trip points.

FIGURE 2-20: AC LOADING



2.3.5.8.1 Timing Characteristics

TABLE 2-164: SSTL2 CLASS II – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 2.3 V VREF = 1.25 V, APPLICABLE TO PRO I/O BANKS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.59	1.95	0.04	1.89	0.38	1.99	1.59			1.99	1.59	ns
–1	0.50	1.66	0.03	1.61	0.33	1.69	1.36			1.69	1.36	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-165: SSTL2 CLASS II – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE V_{CCI} = 2.3 V VREF = 1.25 V, APPLICABLE TO PRO I/O BANKS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.77	1.95	0.05	1.89	0.50	1.99	1.59			1.99	1.59	ns
–1	0.66	1.66	0.04	1.61	0.43	1.69	1.36			1.69	1.36	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.3.5.9 SSTL3 Class I

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

TABLE 2-166: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

SSTL3 Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
14 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.7	VCCI – 1.1	14	14	51	54	10	10

Note 1: Currents are measured at 100°C junction temperature and maximum voltage.

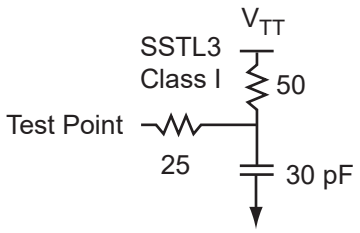
2: Currents are measured at 85°C junction temperature.

TABLE 2-167: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.5	1.5	1.485	30

Note: *Measuring point = Vtrip. See Table 2-16 for a complete table of trip points.

FIGURE 2-21: AC LOADING



2.3.5.9.1 Timing Characteristics

TABLE 2-168: SSTL3 CLASS I – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 3.0 V VREF = 1.5 V, APPLICABLE TO PRO I/O BANKS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.59	2.08	0.04	1.81	0.38	2.11	1.65			2.11	1.65	ns
–1	0.50	1.77	0.03	1.54	0.33	1.80	1.41			1.80	1.41	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-169: SSTL3 CLASS I – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 3.0 V VREF = 1.5 V, APPLICABLE TO PRO I/O BANKS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.77	2.08	0.05	1.81	0.50	2.11	1.65			2.11	1.65	ns
–1	0.66	1.77	0.04	1.54	0.43	1.80	1.41			1.80	1.41	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.3.5.10 SSTL3 Class II

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

TABLE 2-170: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

SSTL3 Class II	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
21 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.5	VCCI – 0.9	21	21	103	109	10	10

Note 1: Currents are measured at 100°C junction temperature and maximum voltage.

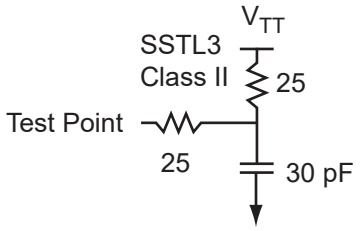
2: Currents are measured at 85°C junction temperature.

TABLE 2-171: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.5	1.5	1.485	30

Note: *Measuring point = Vtrip. See Table 2-16 for a complete table of trip points.

FIGURE 2-22: AC LOADING



2.3.5.10.1 Timing Characteristics

TABLE 2-172: SSTL3 CLASS II – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 3.0 V VREF = 1.5 V, APPLICABLE TO PRO I/O BANKS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.59	1.86	0.04	1.81	0.38	1.89	1.50			1.89	1.50	ns
–1	0.50	1.58	0.03	1.54	0.33	1.61	1.28			1.61	1.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-173: SSTL3 CLASS II – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 3.0 V VREF = 1.5 V, APPLICABLE TO PRO I/O BANKS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.77	1.86	0.05	1.81	0.50	1.89	1.50			1.89	1.50	ns
–1	0.66	1.58	0.04	1.54	0.43	1.61	1.28			1.61	1.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.3.6 DIFFERENTIAL I/O CHARACTERISTICS

2.3.6.1 Physical Implementation

Configuration of the I/O modules as a differential pair is handled by Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

2.3.6.2 LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-23. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, ProASIC3 also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

FIGURE 2-23: LVDS CIRCUIT DIAGRAM AND BOARD-LEVEL IMPLEMENTATION

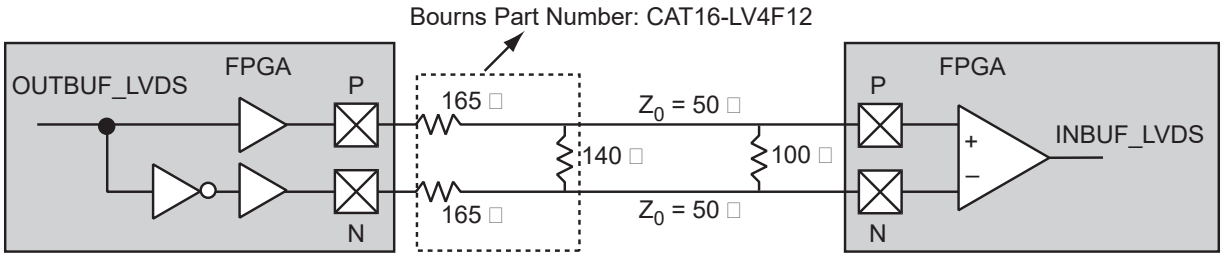


TABLE 2-174: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCI	Supply Voltage	2.375	2.5	2.625	V
VOL	Output Low Voltage	0.9	1.075	1.25	V
VOH	Output High Voltage	1.25	1.425	1.6	V
IOL [1]	Output Lower Current	0.65	0.91	1.16	mA
IOH [1]	Output High Current	0.65	0.91	1.16	mA
V_I	Input Voltage	0		2.925	V
IIH [2]	Input High Leakage Current			10	µA
IIL [2]	Input Low Leakage Current			10	µA
VODIFF	Differential Output Voltage	250	350	450	mV
VOCM	Output Common Mode Voltage	1.125	1.25	1.375	V
VICM	Input Common Mode Voltage	0.05	1.25	2.35	V
VIDIFF	Input Differential Voltage	100	350		mV

Note 1: Currents are measured at 85°C junction temperature.

2: IOL/IOH is defined by VODIFF/(Resistor Network).

TABLE 2-175: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input Low (V)	Input High (V)	Measuring Point* (V)
1.075	1.325	Cross point

Note: *Measuring point = V_{trip}. See Table 2-27 for a complete table of trip points.

2.3.6.2.1 Timing Characteristics

1.5 V DC Core Voltage

TABLE 2-176: LVDS – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 2.3 V, APPLICABLE TO PRO I/O BANKS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.59	1.65	0.04	2.18	ns
–1	0.50	1.40	0.03	1.85	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-177: LVDS – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 2.3 V, APPLICABLE TO ADVANCED I/O BANKS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.54	1.65	0.04	1.44	ns
–1	0.46	1.40	0.03	1.23	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

1.2 V DC Core Voltage

TABLE 2-178: LVDS – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 2.3 V, APPLICABLE TO PRO I/O BANKS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.77	1.68	0.05	2.18	ns
–1	0.66	1.43	0.04	1.85	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-179: LVDS – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 2.3 V, APPLICABLE TO ADVANCED I/O BANKS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.70	1.65	0.05	1.44	ns
–1	0.60	1.40	0.04	1.23	ns

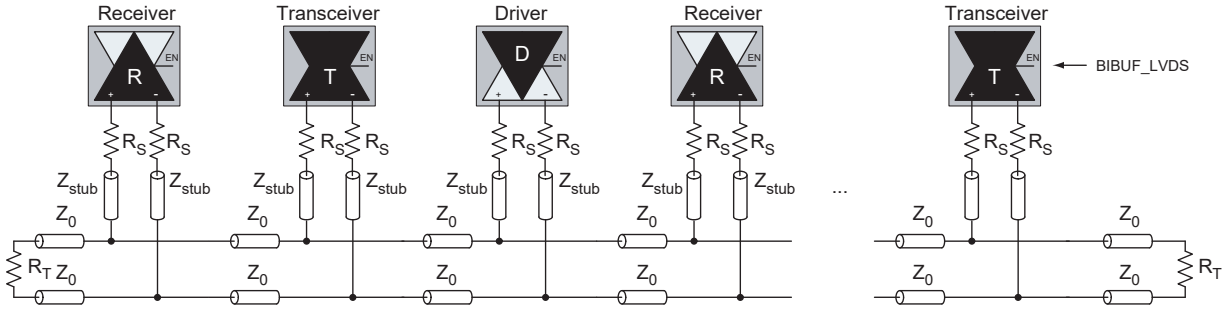
Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.3.6.3 B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Microchip LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Microchip LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-24. The input and output buffer delays are available in the LVDS section in Table 2-174.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case Industrial operating conditions, at the farthest receiver: R_S = 60 Ω and R_T = 70 Ω, given Z_0 = 50 Ω (2") and Z_{stub} = 50 Ω (~1.5").

FIGURE 2-24: B-LVDS/M-LVDS MULTIPOINT APPLICATION USING LVDS I/O BUFFERS



2.3.6.4 LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-25. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

FIGURE 2-25: LVPECL CIRCUIT DIAGRAM AND BOARD-LEVEL IMPLEMENTATION

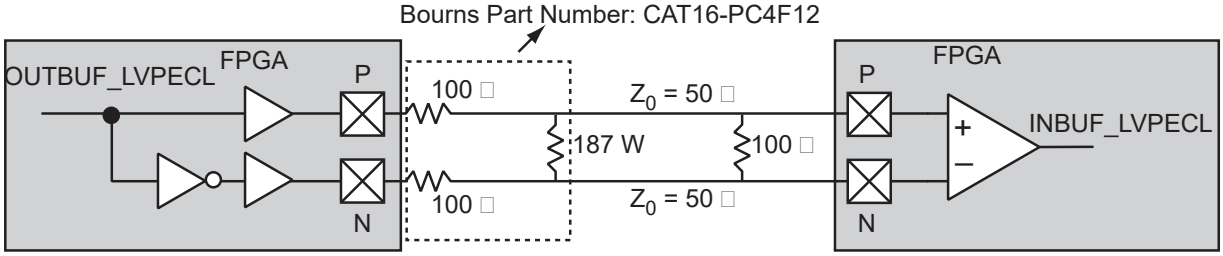


TABLE 2-180: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
VCCI	Supply Voltage	3.0		3.3		3.6		V
VOL	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
VOH	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
VIL, VIH	Input Low, Input High Voltages	0	3.6	0	3.6	0	3.6	V
VODIFF	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
VOCM	Output Common-Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
VICM	Input Common-Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
VIDIFF	Input Differential Voltage	300		300		300		mV

TABLE 2-181: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input Low (V)	Input High (V)	Measuring Point* (V)
1.64	1.94	Cross point

Note: *Measuring point = Vtrip. See Table 2-27 for a complete table of trip points.

2.3.6.4.1 Timing Characteristics

1.5 V DC Core Voltage

TABLE 2-182: LVPECL – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 3.0 V, APPLICABLE TO PRO I/O BANKS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.59	1.64	0.04	1.97	ns
–1	0.50	1.40	0.03	1.67	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-183: LVPECL – APPLIES TO 1.5 V DC CORE VOLTAGE, COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 3.0 V, APPLICABLE TO ADVANCED I/O BANKS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.54	1.62	0.04	1.26	ns
–1	0.46	1.38	0.03	1.08	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

1.2 V DC Core Voltage

TABLE 2-184: LVPECL – APPLIES TO 1.2 V DC CORE VOLTAGE, COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 3.0 V, APPLICABLE TO PRO I/O BANKS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.77	1.62	0.05	1.97	ns
–1	0.66	1.37	0.04	1.67	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-185: LVPECL – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V, WORST-CASE VCCI = 3.0 V, APPLICABLE TO ADVANCED I/O BANKS)

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.70	1.62	0.05	1.26	ns
–1	0.60	1.38	0.04	1.08	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.3.7 I/O REGISTER SPECIFICATIONS

2.3.7.1 Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

FIGURE 2-26: TIMING MODEL OF REGISTERED I/O BUFFERS WITH SYNCHRONOUS ENABLE

AND ASYNCHRONOUS PRESET

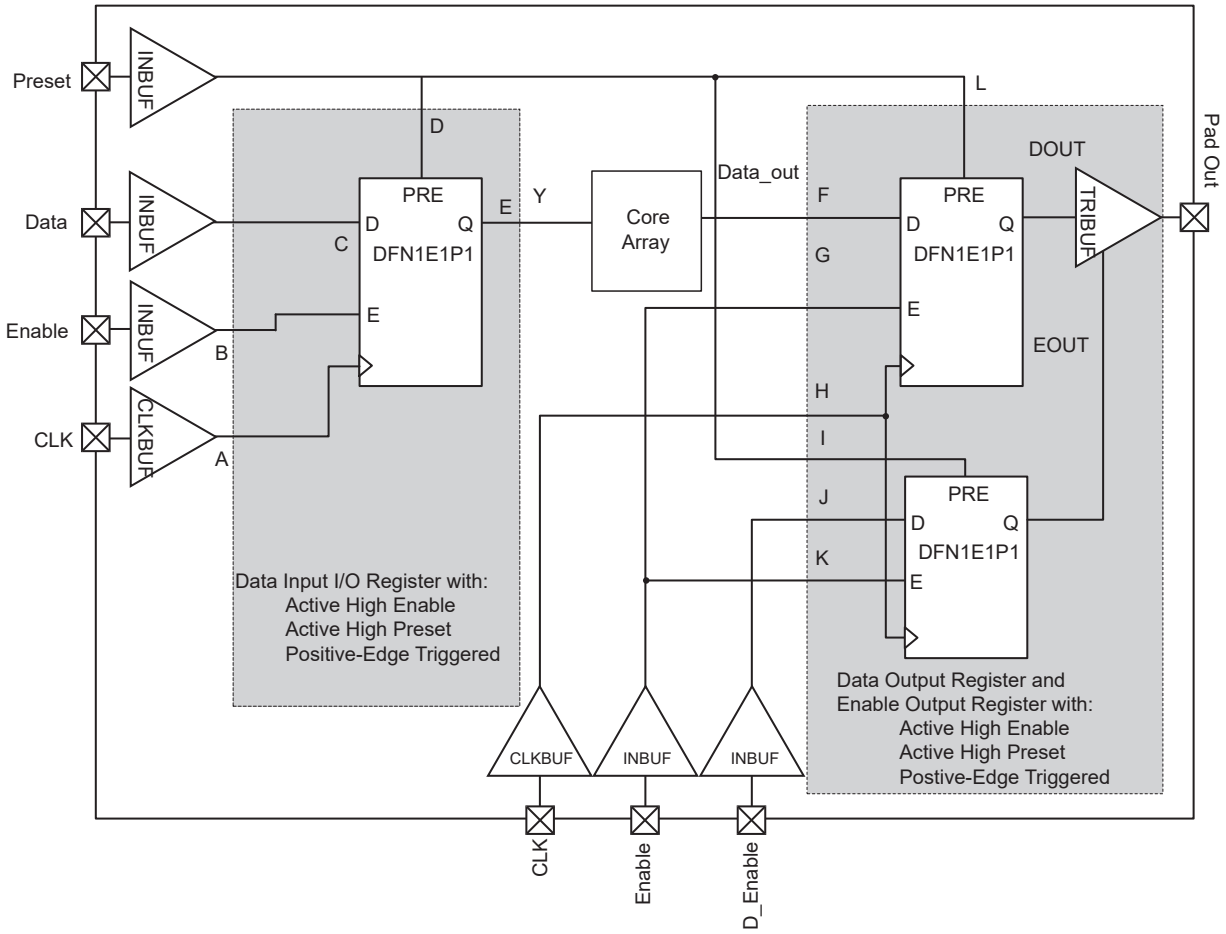


TABLE 2-186: PARAMETER DEFINITION AND MEASURING NODES

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

Note: *See Figure 2-26 for more information.

2.3.7.2 Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

FIGURE 2-27: TIMING MODEL OF THE REGISTERED I/O BUFFERS WITH SYNCHRONOUS ENABLE AND ASYNCHRONOUS CLEAR

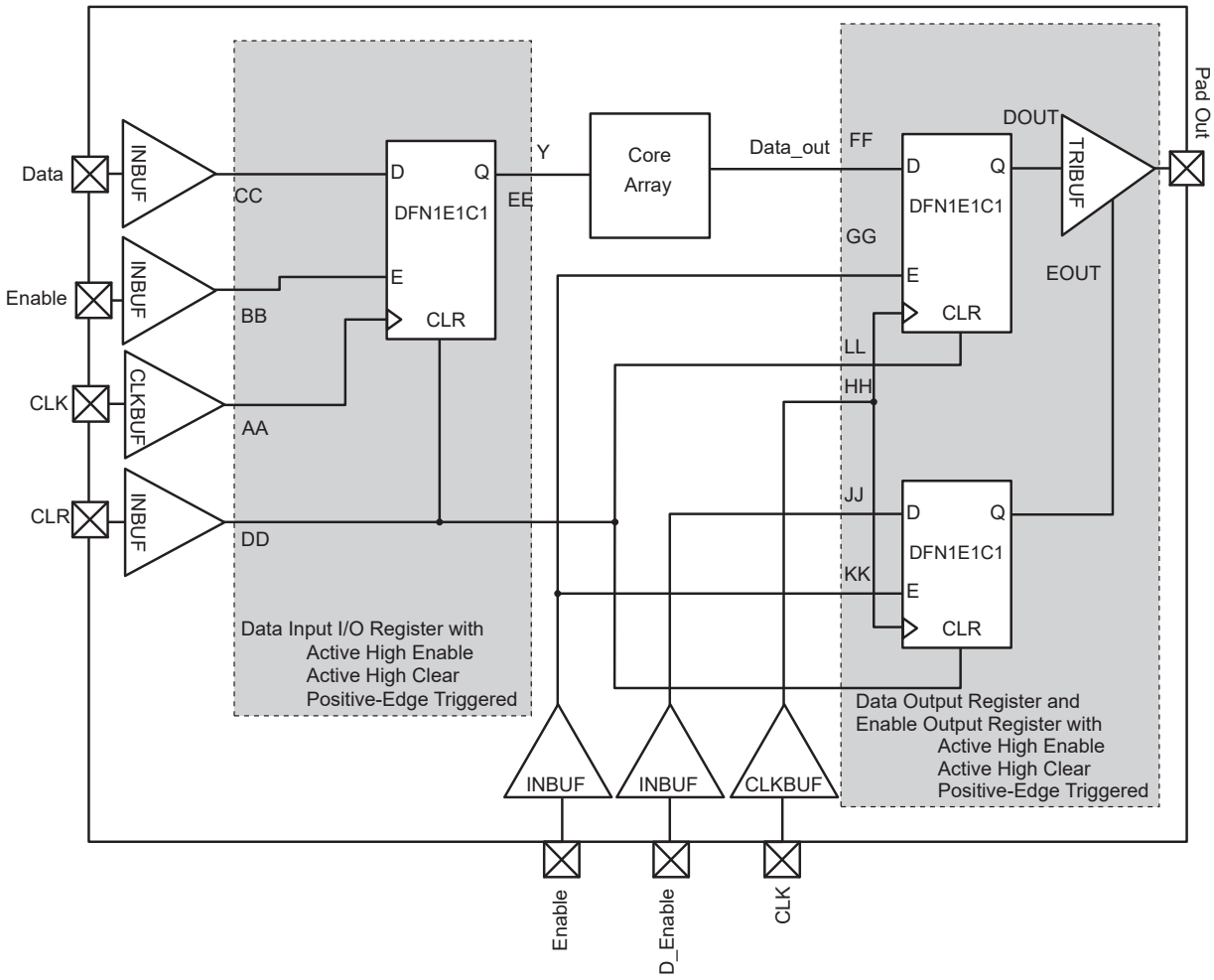


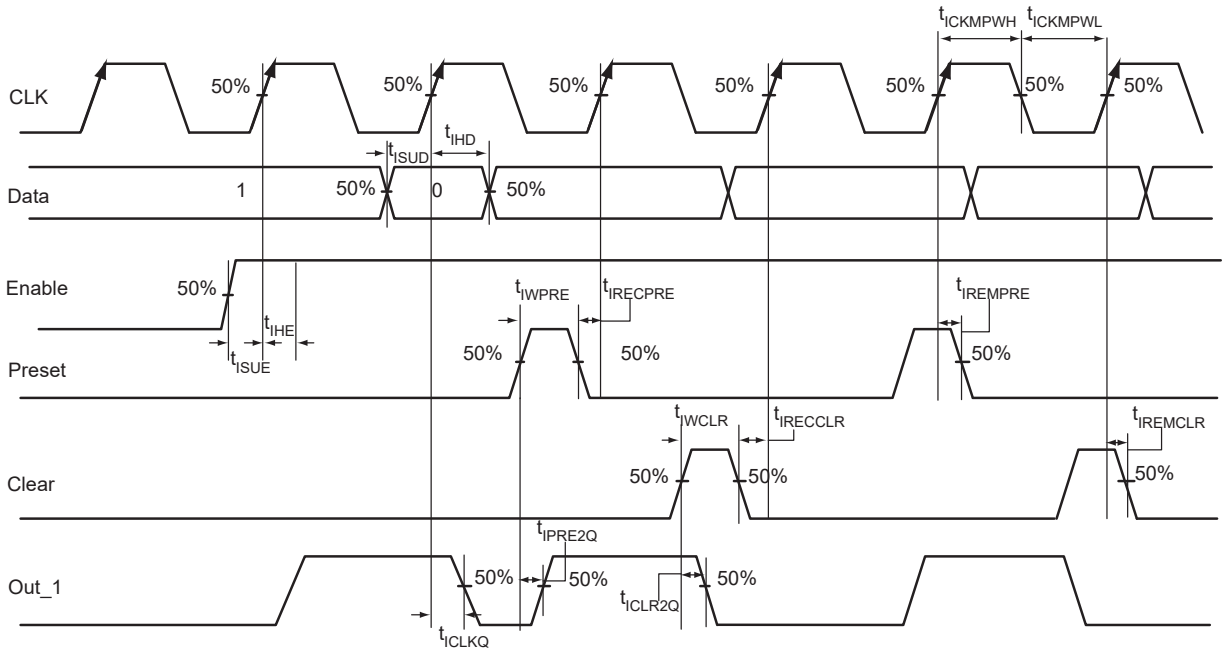
TABLE 2-187: PARAMETER DEFINITION AND MEASURING NODES

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	FF, HH
t_{OHD}	Data Hold Time for the Output Data Register	FF, HH
t_{OSUE}	Enable Setup Time for the Output Data Register	GG, HH
t_{OHE}	Enable Hold Time for the Output Data Register	GG, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold Time for the Output Enable Register	JJ, HH
t_{OESUE}	Enable Setup Time for the Output Enable Register	KK, HH
t_{OEHE}	Enable Hold Time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t_{IHD}	Data Hold Time for the Input Data Register	CC, AA
t_{ISUE}	Enable Setup Time for the Input Data Register	BB, AA
t_{IHE}	Enable Hold Time for the Input Data Register	BB, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

Note: *See Figure 2-27 for more information.

2.3.7.3 Input Register

FIGURE 2-28: INPUT REGISTER TIMING DIAGRAM



1.5 V DC Core Voltage

TABLE 2-188: INPUT DATA REGISTER PROPAGATION DELAYS (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V)

Parameter	Description	–1	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.24	0.29	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.27	0.31	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.38	0.45	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.46	0.54	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.46	0.54	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.23	0.27	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.23	0.27	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	0.22	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	0.22	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.31	0.36	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.28	0.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

1.2 V DC Core Voltage

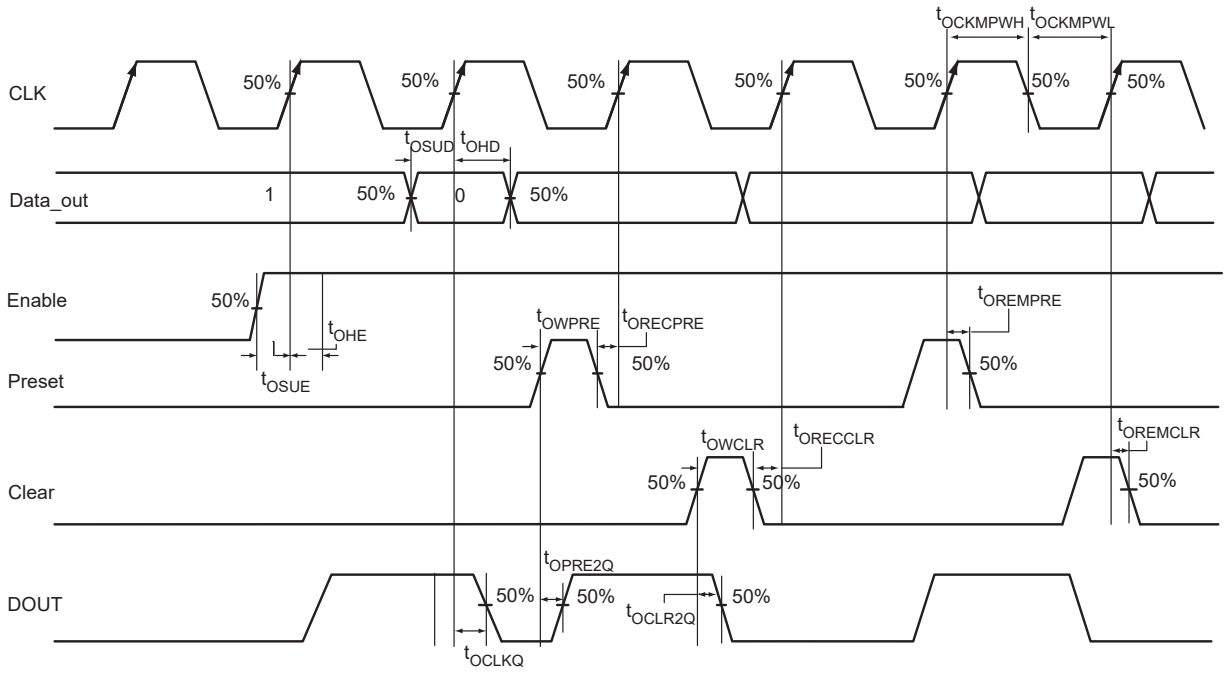
TABLE 2-189: INPUT DATA REGISTER PROPAGATION DELAYS (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V)

Parameter	Description	–1	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.32	0.37	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.35	0.41	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.50	0.58	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.60	0.71	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.60	0.71	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.30	0.35	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.30	0.35	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	0.22	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	0.22	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.31	0.36	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.28	0.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.3.7.4 Output Register

FIGURE 2-29: OUTPUT REGISTER TIMING DIAGRAM



2.3.7.4.1 Timing Characteristics

1.5 V DC Core Voltage

TABLE 2-190: OUTPUT DATA REGISTER PROPAGATION DELAYS (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V)

Parameter	Description	–1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.60	0.71	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.32	0.37	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.45	0.53	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.82	0.96	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.82	0.96	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.23	0.27	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.23	0.27	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	0.22	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	0.22	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.31	0.36	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.28	0.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

1.2 V DC Core Voltage

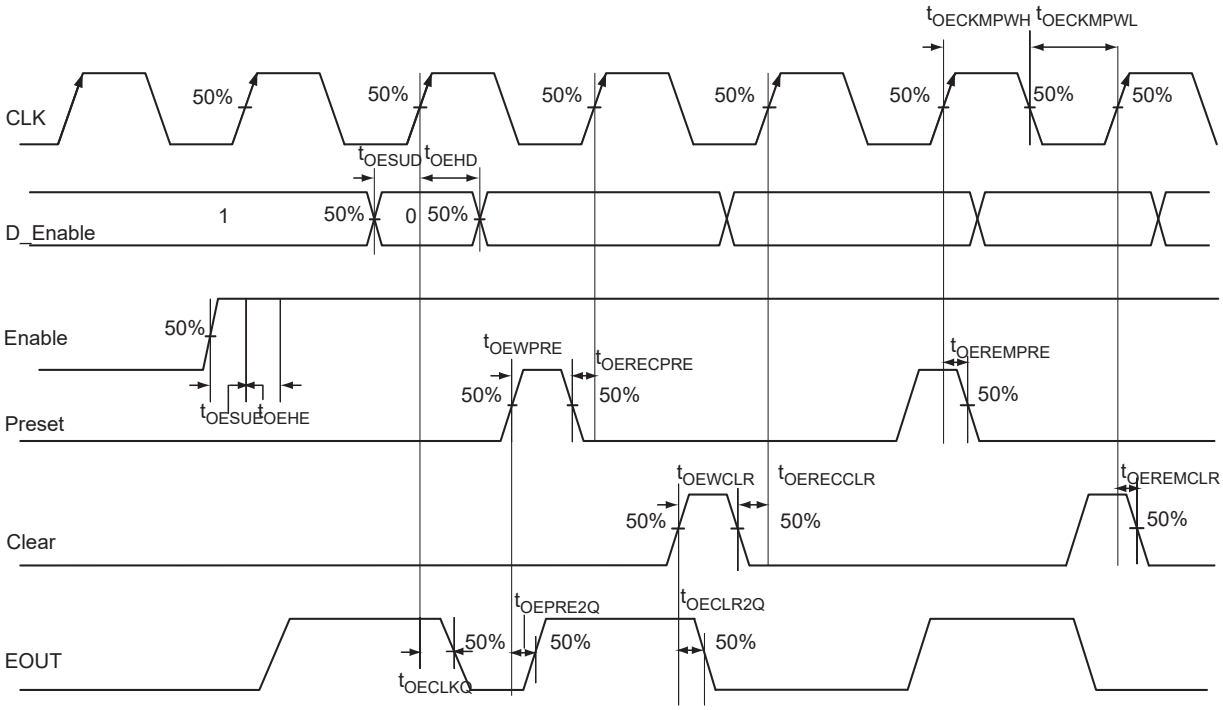
TABLE 2-191: OUTPUT DATA REGISTER PROPAGATION DELAYS (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V)

Parameter	Description	–1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.78	0.92	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.42	0.49	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.58	0.69	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	1.07	1.26	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	1.07	1.26	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.30	0.35	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.30	0.35	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	0.22	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	0.22	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.31	0.36	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.28	0.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.3.7.5 Output Enable Register

FIGURE 2-30: OUTPUT ENABLE REGISTER TIMING DIAGRAM



2.3.7.5.1 Timing Characteristics

1.5 V DC Core Voltage

TABLE 2-192: OUTPUT ENABLE REGISTER PROPAGATION DELAYS (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V)

Parameter	Description	–1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.45	0.53	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.32	0.37	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.44	0.52	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.68	0.80	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.68	0.80	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.23	0.27	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.23	0.27	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	0.22	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	0.22	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.31	0.36	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.28	0.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

1.2 V DC Core Voltage

TABLE 2-193: OUTPUT ENABLE REGISTER PROPAGATION DELAYS (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V)

Parameter	Description	–1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.59	0.70	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.42	0.49	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.58	0.68	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.89	1.04	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.89	1.04	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.30	0.35	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.30	0.35	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	0.22	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	0.22	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.31	0.36	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.28	0.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.3.8 DDR MODULE SPECIFICATIONS

2.3.8.1 Input DDR Module

FIGURE 2-31: INPUT DDR TIMING MODEL

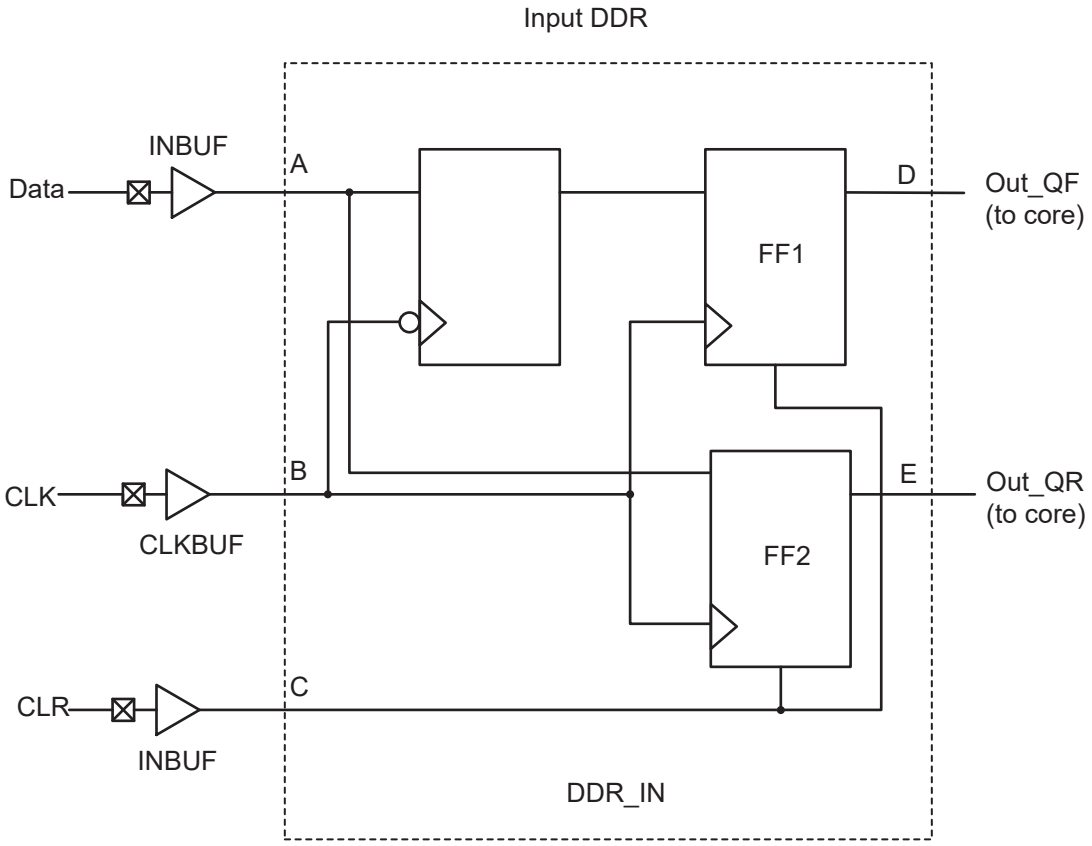
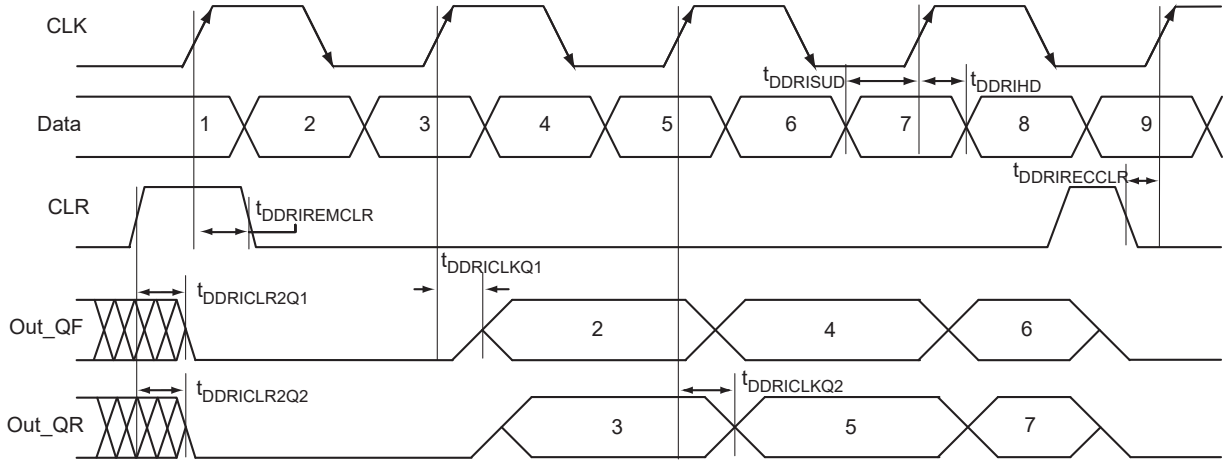


TABLE 2-194: PARAMETER DEFINITIONS

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

FIGURE 2-32: INPUT DDR TIMING DIAGRAM



2.3.8.1.1 Timing Characteristics

1.5 V DC Core Voltage

TABLE 2-195: INPUT DDR PROPAGATION DELAYS (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V)

Parameter	Description	–1	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.28	0.33	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.40	0.47	ns
$t_{DDRISUD1}$	Data Setup for Input DDR (fall)	0.29	0.34	ns
$t_{DDRISUD2}$	Data Setup for Input DDR (rise)	0.25	0.29	ns
$t_{DDRIHD1}$	Data Hold for Input DDR (fall)	0.00	0.00	ns
$t_{DDRIHD2}$	Data Hold for Input DDR (rise)	0.00	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.47	0.55	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.58	0.68	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal Time for Input DDR	0.00	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery Time for Input DDR	0.23	0.27	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.18	0.22	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width High for Input DDR	0.31	0.36	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width Low for Input DDR	0.28	0.32	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	250.00	250.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

1.2 V DC Core Voltage

TABLE 2-196: INPUT DDR PROPAGATION DELAYS (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V)

Parameter	Description	–1	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.43	0.37	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.61	0.52	ns
$t_{DDRISUD1}$	Data Setup for Input DDR (fall)	0.44	0.38	ns
$t_{DDRISUD2}$	Data Setup for Input DDR (rise)	0.39	0.33	ns
$t_{DDRIHD1}$	Data Hold for Input DDR (fall)	0.00	0.00	ns
$t_{DDRIHD2}$	Data Hold for Input DDR (rise)	0.00	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.73	0.62	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.89	0.76	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal Time for Input DDR	0.00	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery Time for Input DDR	0.35	0.30	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.22	0.19	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width High for Input DDR	0.36	0.31	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width Low for Input DDR	0.32	0.28	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	160.00	160.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.3.8.2 Output DDR Module

FIGURE 2-33: OUTPUT DDR TIMING MODEL

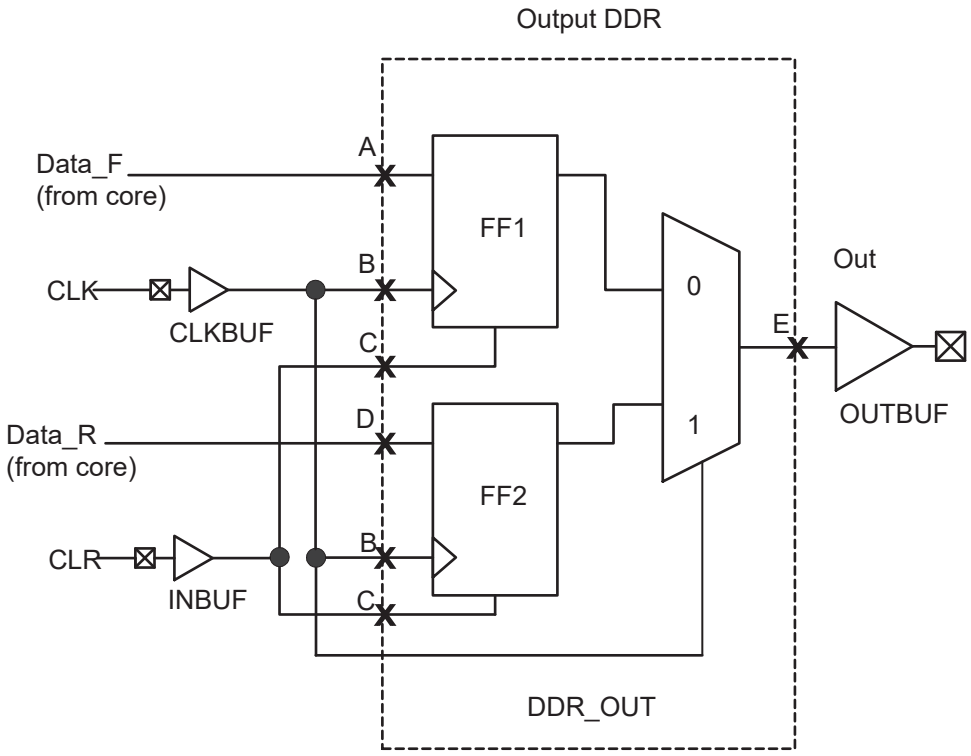
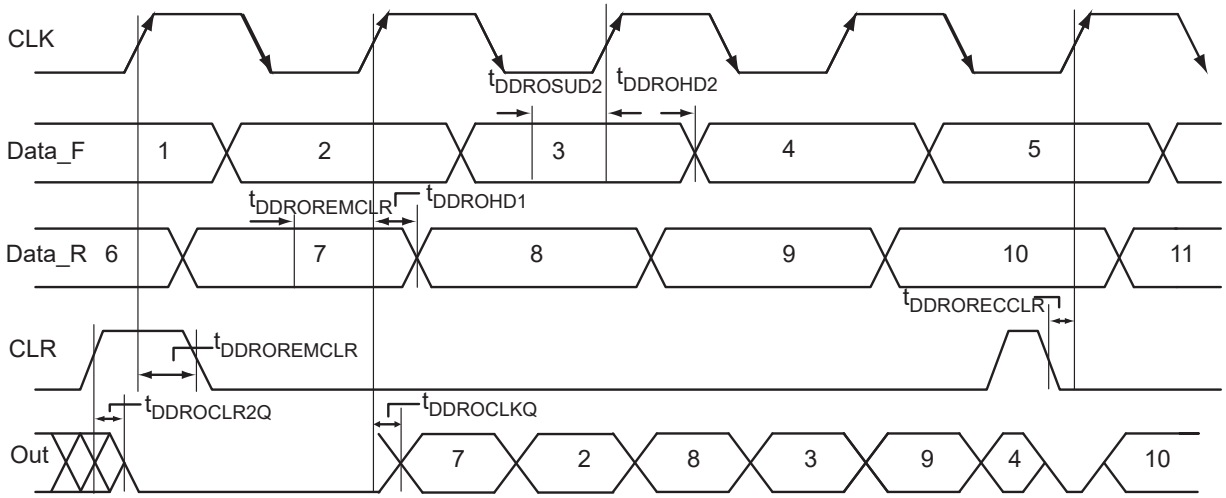


TABLE 2-197: PARAMETER DEFINITIONS

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

FIGURE 2-34: OUTPUT DDR TIMING DIAGRAM



2.3.8.2.1 Timing Characteristics

1.5 V DC Core Voltage

TABLE 2-198: OUTPUT DDR PROPAGATION DELAYS (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V)

Parameter	Description	–1	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	0.72	0.84	ns
$t_{DDRISUD1}$	Data_F Data Setup for Output DDR	0.39	0.45	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.39	0.45	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	0.82	0.96	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.23	0.27	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	0.22	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR	0.31	0.36	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR	0.28	0.32	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	250.00	250.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

1.2 V DC Core Voltage

TABLE 2-199: OUTPUT DDR PROPAGATION DELAYS (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V)

Parameter	Description	–1	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	1.10	0.94	ns
$t_{DDRISUD1}$	Data_F Data Setup for Output DDR	0.59	0.50	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.59	0.50	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	1.26	1.07	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.35	0.30	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.22	0.19	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR	0.36	0.31	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR	0.32	0.28	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	160.00	160.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.4 VersaTile Characteristics

2.4.1 VERSATILE SPECIFICATIONS AS A COMBINATORIAL MODULE

The ProASIC3 library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *IGLOO®, Fusion, and ProASIC3 Macro Library Guide*.

FIGURE 2-35: SAMPLE OF COMBINATORIAL CELLS

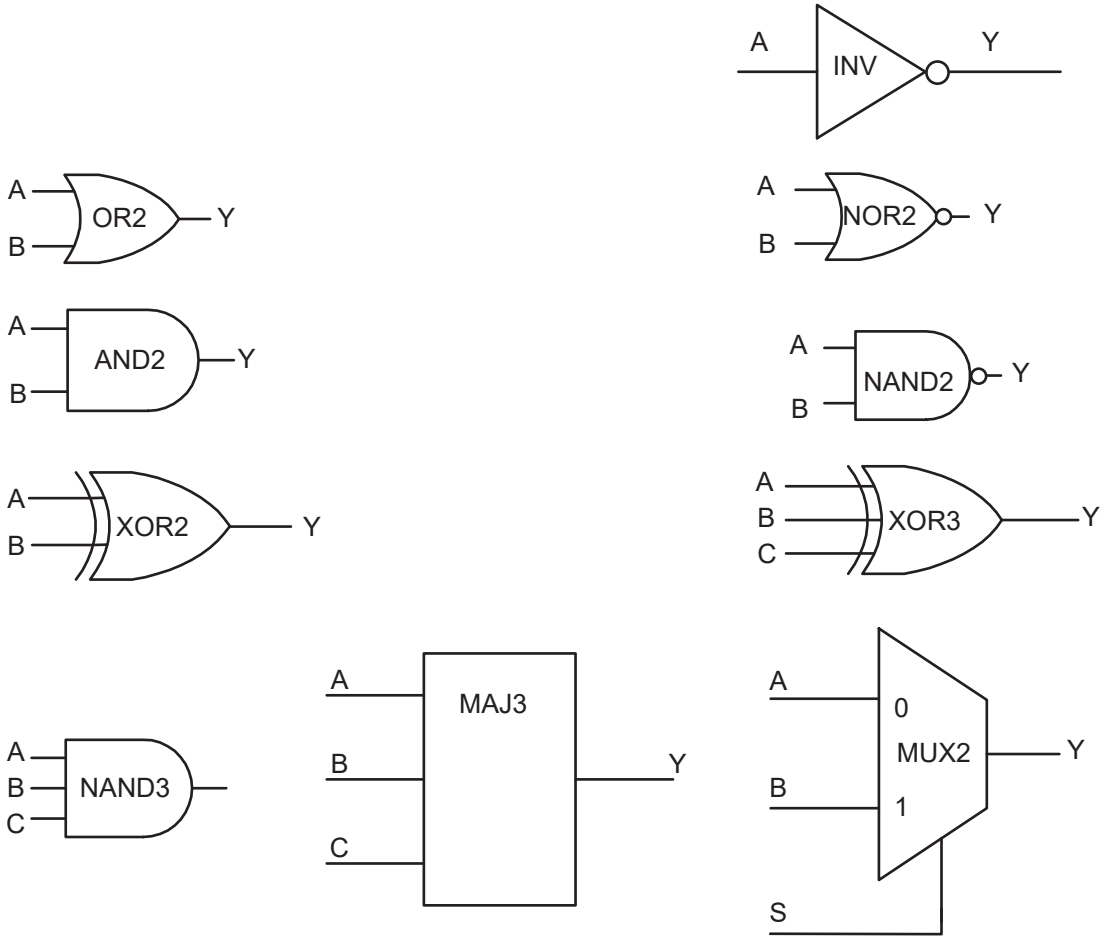
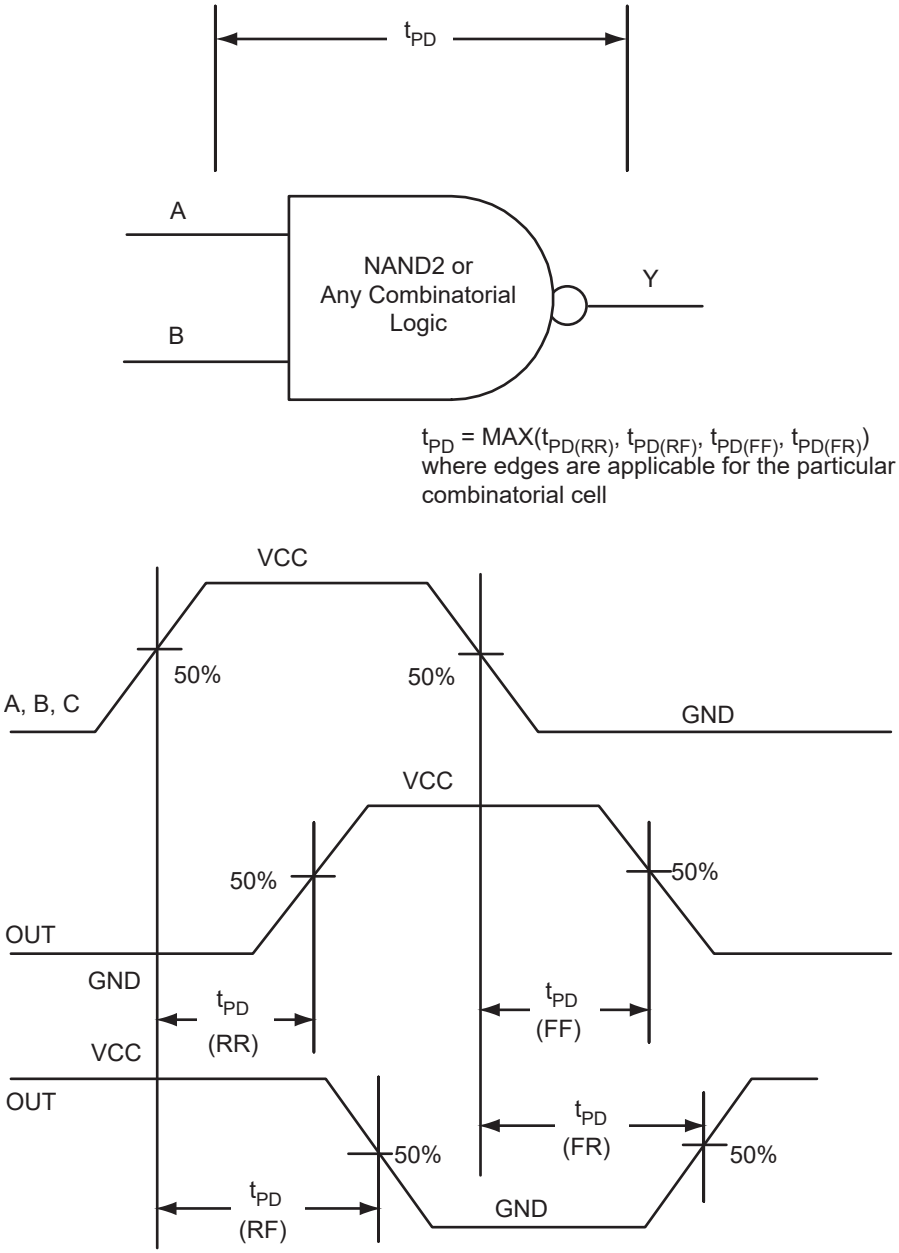


FIGURE 2-36: TIMING MODEL AND WAVEFORMS



2.4.1.1 Timing Characteristics

1.5 V DC Core Voltage

TABLE 2-200: COMBINATORIAL CELL PROPAGATION DELAYS (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V)

Combinatorial Cell	Equation	Parameter	–1	Std.	Units
INV	Y =!A	t_{PD}	0.41	0.48	ns
AND2	Y = A · B	t_{PD}	0.48	0.57	ns
NAND2	Y =!(A · B)	t_{PD}	0.48	0.57	ns
OR2	Y = A + B	t_{PD}	0.50	0.58	ns
NOR2	Y =!(A + B)	t_{PD}	0.50	0.58	ns
XOR2	Y = A ⊕ B	t_{PD}	0.75	0.88	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	0.71	0.84	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	0.89	1.05	ns
MUX2	Y = A !S + B S	t_{PD}	0.52	0.61	ns
AND3	Y = A · B · C	t_{PD}	0.57	0.67	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

1.2 V DC Core Voltage

TABLE 2-201: COMBINATORIAL CELL PROPAGATION DELAYS (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V)

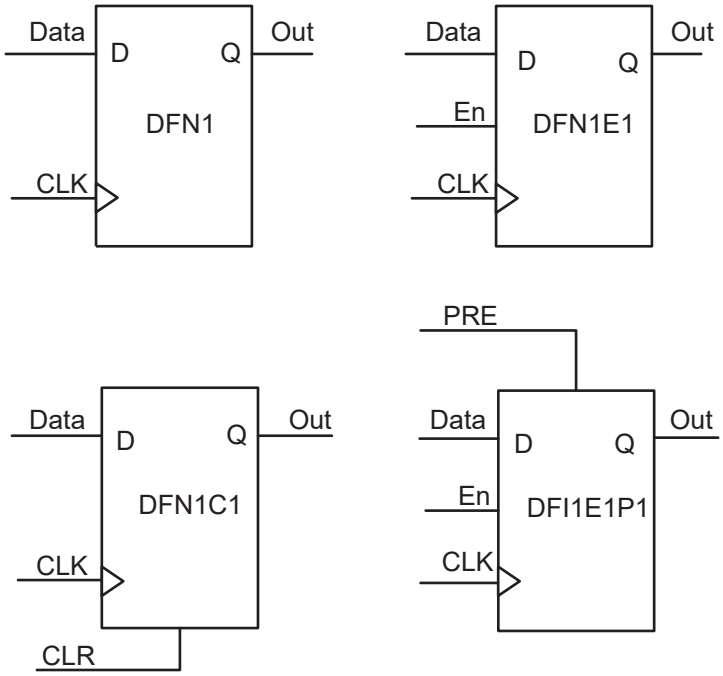
Combinatorial Cell	Equation	Parameter	–1	Std.	Units
INV	Y = !A	t_{PD}	0.54	0.63	ns
AND2	Y = A · B	t_{PD}	0.63	0.74	ns
NAND2	Y = !(A · B)	t_{PD}	0.63	0.74	ns
OR2	Y = A + B	t_{PD}	0.65	0.76	ns
NOR2	Y = !(A + B)	t_{PD}	0.65	0.76	ns
XOR2	Y = A ⊕ B	t_{PD}	0.98	1.16	ns
MAJ3	Y = MAJ(A , B, C)	t_{PD}	0.93	1.09	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	1.17	1.37	ns
MUX2	Y = A !S + B S	t_{PD}	0.68	0.79	ns
AND3	Y = A · B · C	t_{PD}	0.75	0.88	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.4.2 VERSATILE SPECIFICATIONS AS A SEQUENTIAL MODULE

The ProASIC3 library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.

FIGURE 2-37: SAMPLE OF SEQUENTIAL CELLS



2.4.2.1 Timing Characteristics

1.5 V DC Core Voltage

TABLE 2-202: REGISTER DELAYS (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V)

Parameter	Description	–1	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.56	0.66	ns
t_{SUD}	Data Setup Time for the Core Register	0.44	0.51	ns
t_{HD}	Data Hold Time for the Core Register	0.00	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.46	0.55	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.41	0.48	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.41	0.48	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.23	0.27	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.23	0.27	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.30	0.34	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.30	0.34	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.56	0.64	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.56	0.64	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

1.2 V DC Core Voltage

TABLE 2-203: REGISTER DELAYS (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V)

Parameter	Description	–1	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.73	0.86	ns
t_{SUD}	Data Setup Time for the Core Register	0.57	0.67	ns
t_{HD}	Data Hold Time for the Core Register	0.00	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.61	0.71	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.53	0.63	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.53	0.63	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.30	0.35	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.30	0.35	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.30	0.34	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.30	0.34	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.56	0.64	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.56	0.64	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

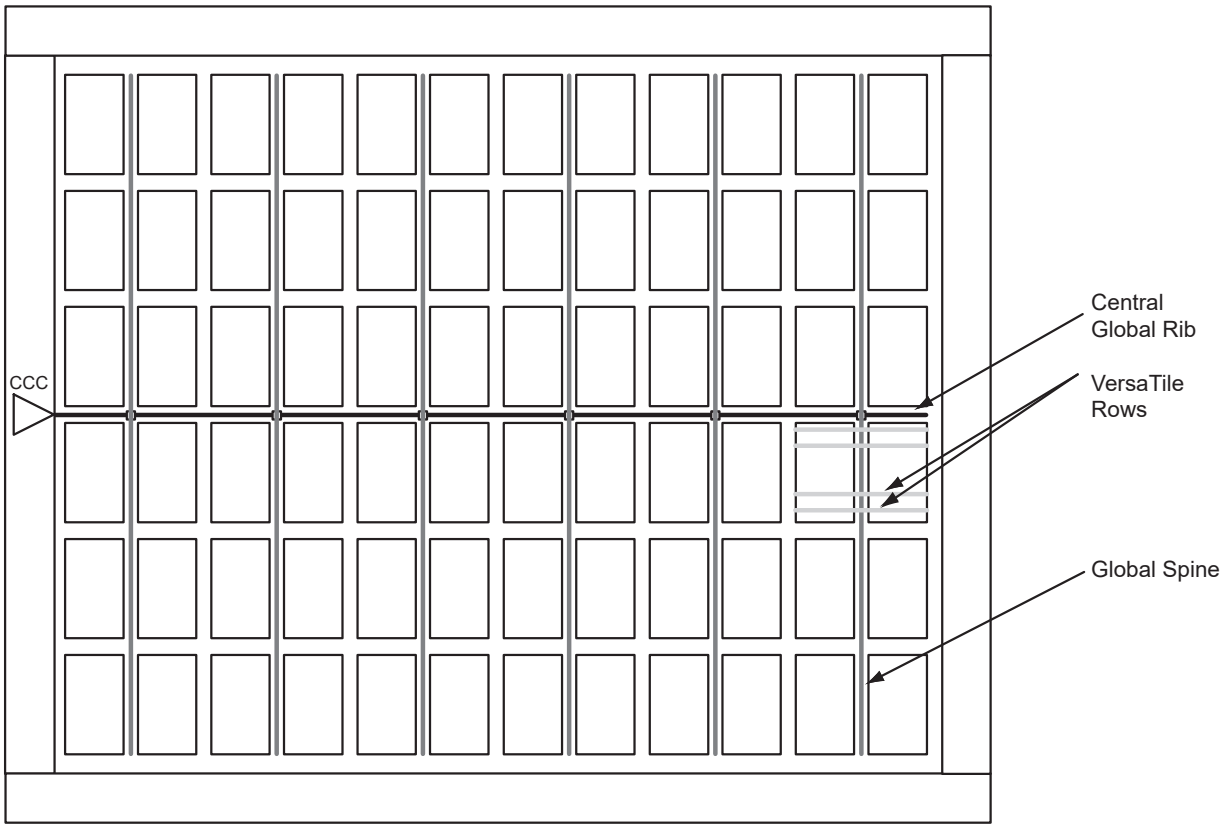
2.5 Global Resource Characteristics

2.5.1 A3P250L CLOCK TREE TOPOLOGY

Clock delays are device-specific. Figure 2-38 is an example of a global tree used for clock routing. The global tree pre-

sented in Figure 2-38 is driven by a CCC located on the west side of the A3P250L device. It is used to drive all D-flip-flops in the device.

FIGURE 2-38: EXAMPLE OF GLOBAL TREE USE IN AN A3P250L DEVICE FOR CLOCK ROUTING



2.5.2 GLOBAL TREE TIMING CHARACTERISTICS

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the section Clock Conditioning Circuits. Table 2-204 to Table 2-204 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

2.5.2.1 Timing Characteristics

TABLE 2-204: A3PE3000L GLOBAL RESOURCE – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, VCC = 1.425 V)

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.53	1.75	1.79	2.06	ns
t_{RCKH}	Input High Delay for Global Clock	1.51	1.77	1.78	2.08	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.75		0.88		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		1.00		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.26		0.30	ns

Note 1: Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2: Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-205: A3PE3000L GLOBAL RESOURCE – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, VCC = 1.14 V)

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.52	1.94	1.78	2.28	ns
t_{RCKH}	Input High Delay for Global Clock	1.49	1.96	1.76	2.30	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.05		1.24		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.23		1.44		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.47		0.55	ns

Note 1: Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2: Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.6 Clock Conditioning Circuits

2.6.1 CCC ELECTRICAL SPECIFICATIONS

2.6.1.1 Timing Characteristics

TABLE 2-206: PROASIC3L CCC/PLL SPECIFICATION (CCC/PLL OPERATING AT 1.2 V)

Parameter	Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		250	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		250	MHz
Delay Increments in Programmable Delay Blocks [1, 2]		270[3]		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Serial Clock (SCLK) for Dynamic PLL[4]			100	MHz
Input Cycle-to-Cycle Jitter (peak magnitude)			1	ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}	Max Peak-to-Peak Period Jitter			
	1 Global Network Used	External FB Used	3 Global Networks Used	
0.75 MHz to 24 MHz	0.50%	0.75%	0.70%	
24 MHz to 100 MHz	1.00%	1.50%	1.20%	
100 MHz to 250 MHz	2.50%	3.75%	2.75%	
Acquisition Time				
LockControl = 0			300	µs
LockControl = 1			6.0	ms
Tracking Jitter[5]				
LockControl = 0			2	ns
LockControl = 1			1	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1, 2]	1.2		15.65	ns
Delay Range in Block: Programmable Delay 2 [1, 2]	0.025		15.65	ns
Delay Range in Block: Fixed Delay [1, 2]		3.1		ns

Note 1: This delay is a function of voltage and temperature. See Table 2-6 for deratings.

2: T_J = 25°C, V_{CC} = 1.2 V

3: When the CCC/PLL core is generated by Microchip core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help for more information.

4: Maximum value obtained for a –1 speed grade device in worst-case commercial conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

5: Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.

TABLE 2-207: PROASIC3L CCC/PLL SPECIFICATION (CCC/PLL OPERATING AT 1.5 V)

Parameter	Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		350	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		350	MHz
Delay Increments in Programmable Delay Blocks [1, 2]		160[3]		ps
Serial Clock (SCLK) for Dynamic PLL [4]			110	
Number of Programmable Values in Each Programmable Delay Block			32	
Input Period Jitter			1.5	ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}	Max Peak-to-Peak Period Jitter			
	1 Global Network Used		3 Global Networks Used	
0.75 MHz to 24 MHz	0.50%		0.70%	
24 MHz to 100 MHz	1.00%		1.20%	
100 MHz to 250 MHz	1.75%		2.00	
250 MHz to 350 MHz	2.50%		5.60%	
Acquisition Time				
LockControl = 0			300	µs
LockControl = 1			6.0	ms
Tracking Jitter[5]				
LockControl = 0			1.6	ns
LockControl = 1			0.8	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1, 2]	0.6		5.56	ns
Delay Range in Block: Programmable Delay 2 [1, 2]	0.025		5.56	ns
Delay Range in Block: Fixed Delay [1, 2]		2.2		ns

Note 1: This delay is a function of voltage and temperature. See Table 2-6 for deratings.

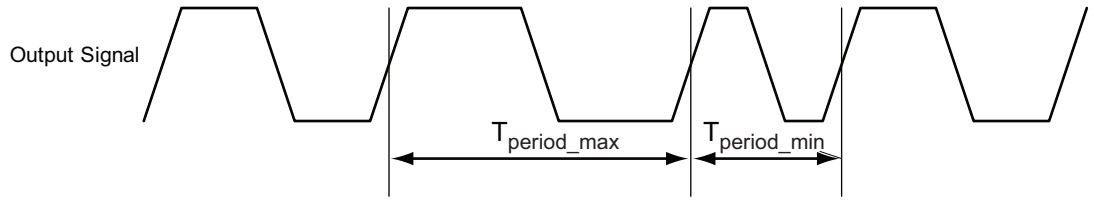
2: T_J = 25°C, VCC = 1.5 V

3: When the CCC/PLL core is generated by Microchip core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help for more information.

4: Maximum value obtained for a –1 speed grade device in worst-case commercial conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

5: Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.

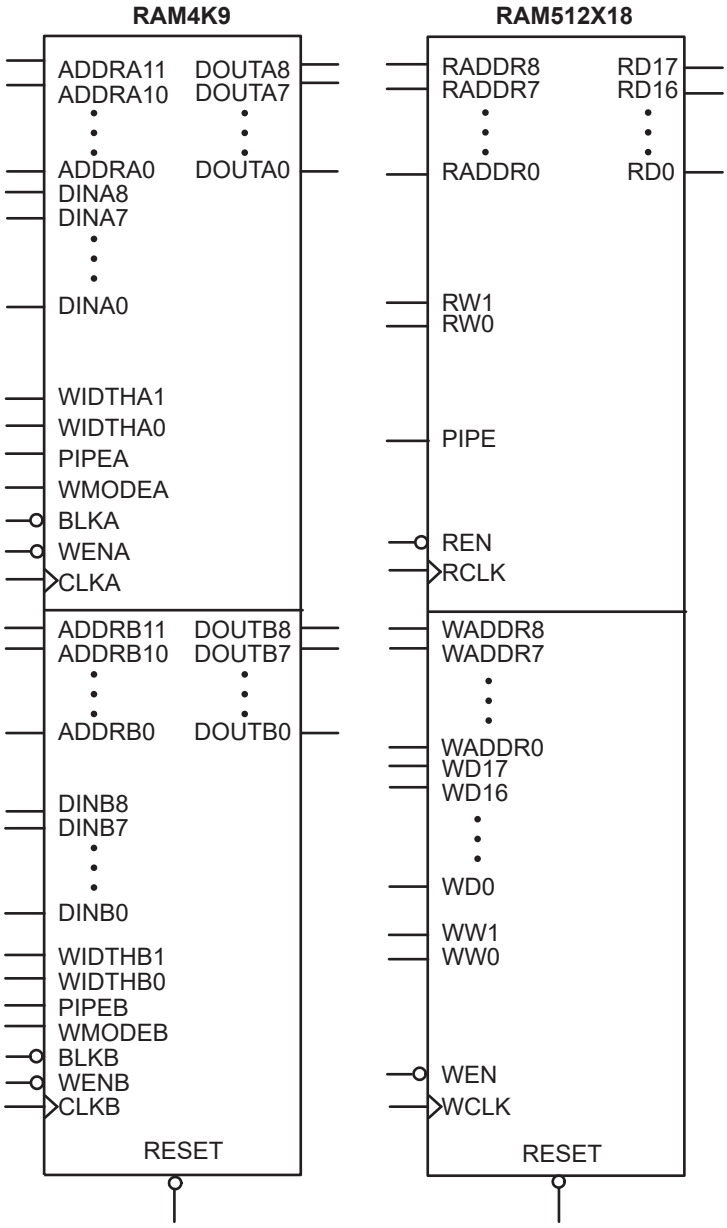
FIGURE 2-39: PEAK-TO-PEAK JITTER DEFINITION



2.7 Embedded SRAM and FIFO Characteristics

2.7.1 SRAM

FIGURE 2-40: RAM MODELS



2.7.1.1 Timing Waveforms

FIGURE 2-41: RAM READ FOR PASS-THROUGH OUTPUT. APPLICABLE TO BOTH RAM4K9 AND RAM512X18

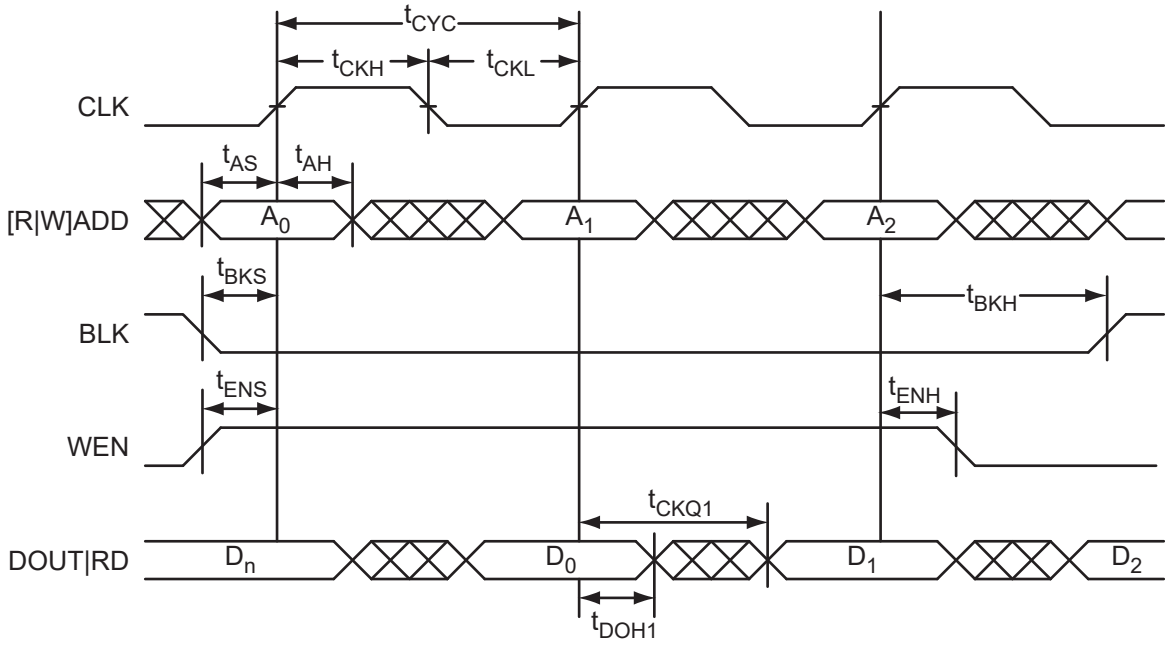


FIGURE 2-42: RAM READ FOR PIPELINED OUTPUT. APPLICABLE TO BOTH RAM4K9 AND RAM512X18

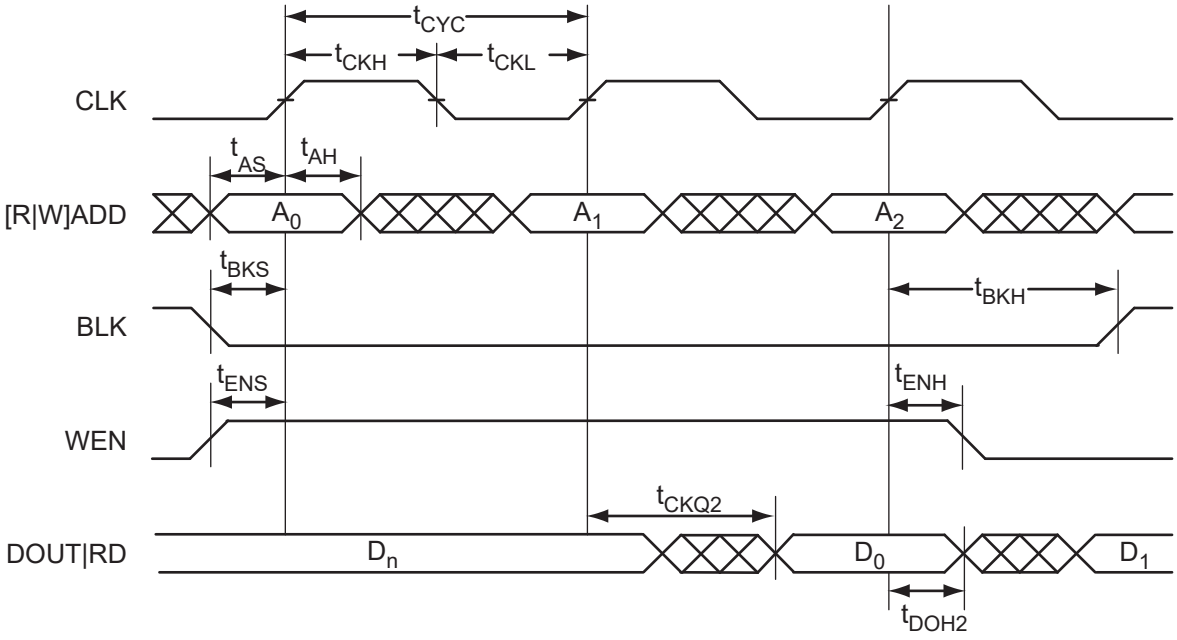


FIGURE 2-43: RAM WRITE, OUTPUT RETAINED. APPLICABLE TO BOTH RAM4K9 AND RAM512X18

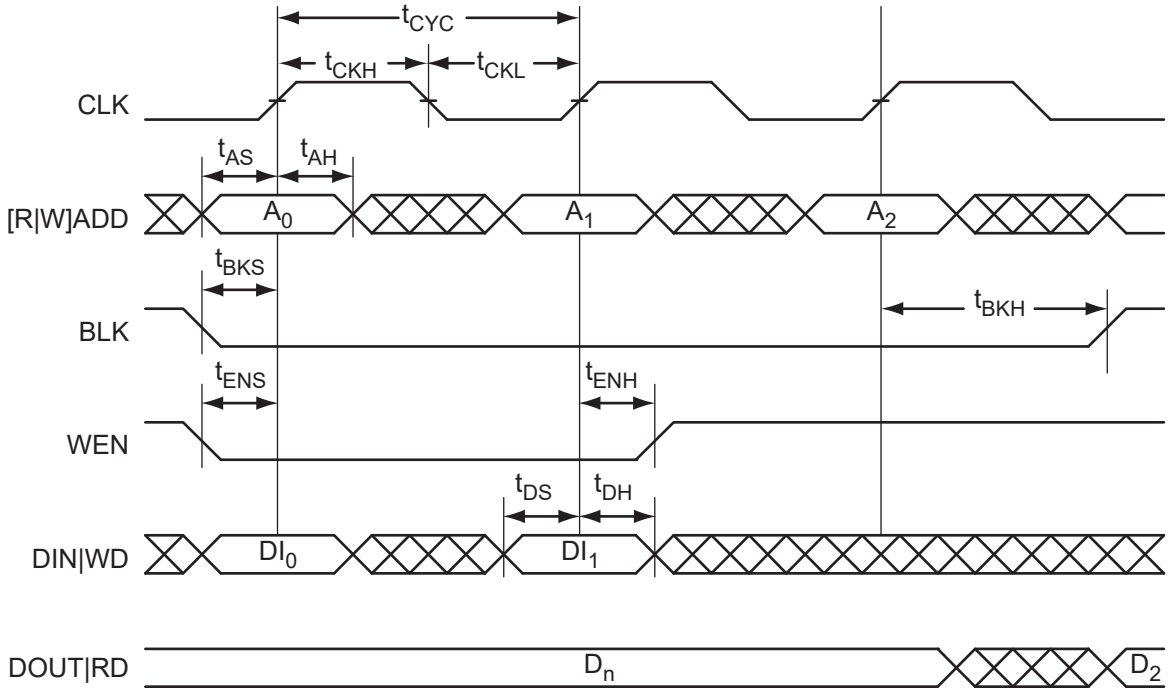


FIGURE 2-44: RAM WRITE, OUTPUT AS WRITE DATA (WMODE = 1). APPLICABLE TO RAM4K9 ONLY

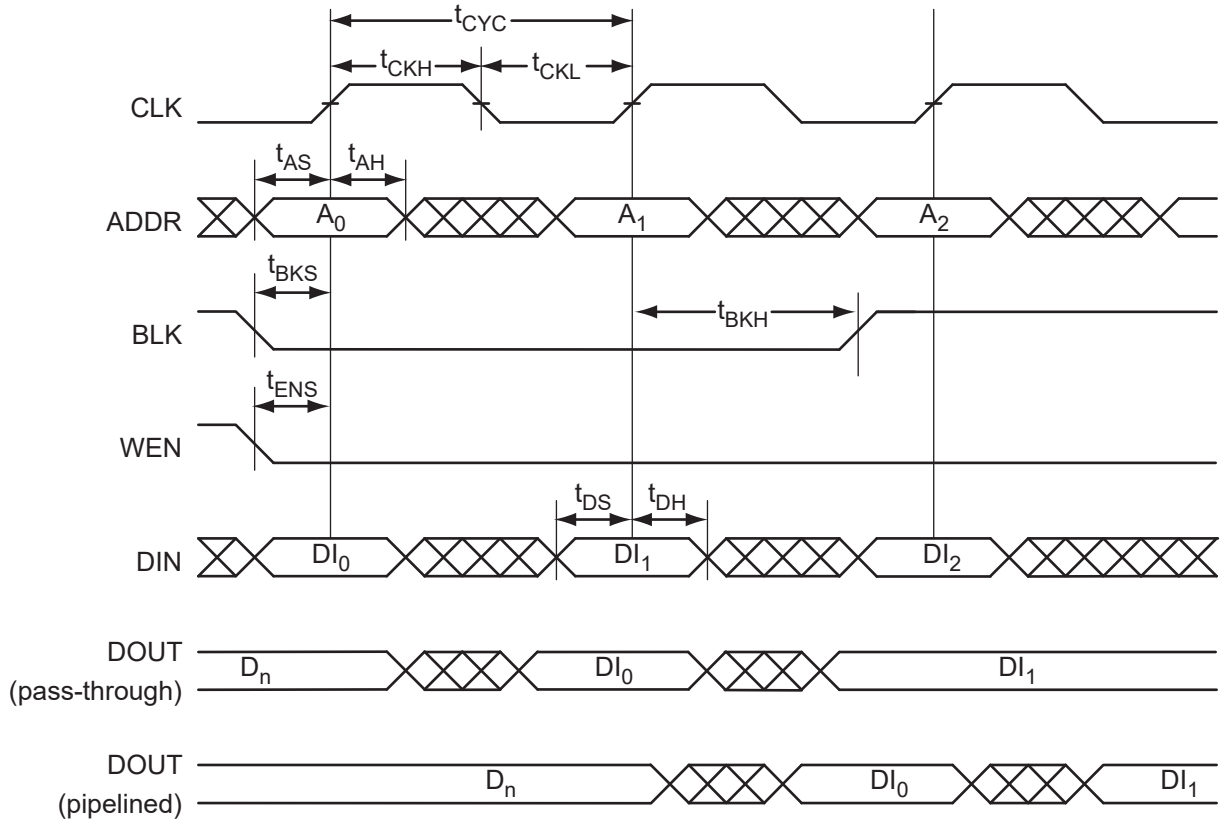
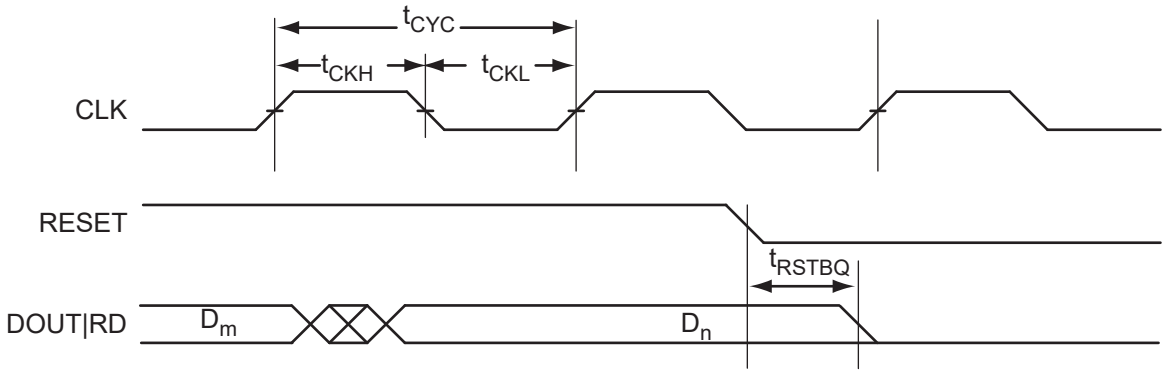


FIGURE 2-45: RAM RESET. APPLICABLE TO BOTH RAM4K9 AND RAM512X18



2.7.1.1.1 Timing Characteristics

TABLE 2-208: RAM4K9 – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V)

Parameter	Description	–1	Std.	Units
t_{AS}	Address setup time	0.25	0.30	ns
t_{AH}	Address hold time	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.15	0.17	ns
t_{ENH}	REN, WEN hold time	0.10	0.12	ns
t_{BKS}	BLK setup time	0.24	0.28	ns
t_{BKH}	BLK hold time	0.02	0.02	ns
t_{DS}	Input data (DIN) setup time	0.19	0.22	ns
t_{DH}	Input data (DIN) hold time	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on DOUT (output retained, WMODE = 0)	1.82	2.14	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	2.40	2.83	ns
t_{CKQ2}	Clock High to new data valid on DOUT (pipelined)	0.91	1.07	ns
t_{C2CWWL} [1]	Address collision clk-to-clk delay for reliable write after write on same address – applicable to closing edge	0.24	0.29	ns
t_{C2CRWH} [1]	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.20	0.24	ns
t_{C2CWRH} [1]	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.25	0.30	ns
t_{RSTBQ}	RESET Low to data out Low on DOUT (flow-through)	0.94	1.11	ns
	RESET Low to data out Low on DOUT (pipelined)	0.94	1.11	ns
$t_{REMRSTB}$	RESET removal	0.29	0.34	ns
$t_{RECRSTB}$	RESET recovery	1.53	1.80	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.55	0.64	ns
t_{CYC}	Clock cycle time	5.10	5.87	ns
F_{MAX}	Maximum frequency	196	170	MHz

Note 1: For more information, refer to the application note *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-209: RAM4K9 – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V)

Parameter	Description	–1	Std.	Units
t_{AS}	Address setup time	0.33	0.39	ns
t_{AH}	Address hold time	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.19	0.22	ns
t_{ENH}	REN, WEN hold time	0.13	0.15	ns
t_{BKS}	BLK setup time	0.31	0.36	ns
t_{BKH}	BLK hold time	0.02	0.03	ns
t_{DS}	Input data (DIN) setup time	0.24	0.29	ns
t_{DH}	Input data (DIN) hold time	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on DOUT (output retained, WMODE = 0)	2.38	2.80	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	3.14	3.69	ns
t_{CKQ2}	Clock High to new data valid on DOUT (pipelined)	1.19	1.40	ns
t_{C2CWWL}[1]	Address collision clk-to-clk delay for reliable write after write on same address – applicable to closing edge	0.25	0.30	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.27	0.32	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.37	0.44	ns
t_{RSTBQ}	RESET Low to data out Low on DOUT (flow-through)	1.23	1.45	ns
	RESET Low to data out Low on DOUT (pipelined)	1.23	1.45	ns
$t_{REMRSTB}$	RESET removal	0.38	0.45	ns
$t_{RECRSTB}$	RESET recovery	2.00	2.35	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.63	0.72	ns
t_{CYC}	Clock cycle time	5.75	6.61	ns
F_{MAX}	Maximum frequency	174	151	MHz

Note 1: For more information, refer to the application note *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-210: RAM512X18 – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V)

Parameter	Description	–1	Std.	Units
t_{AS}	Address setup time	0.25	0.30	ns
t_{AH}	Address hold time	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.09	0.11	ns
t_{ENH}	REN, WEN hold time	0.06	0.07	ns
t_{DS}	Input data (WD) setup time	0.19	0.22	ns
t_{DH}	Input data (WD) hold time	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on DO (output retained, WMODE = 0)	2.20	2.59	ns
t_{CKQ2}	Clock High to new data valid on DO (pipelined)	0.91	1.07	ns
t_{C2CRWH} [1]	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.18	0.21	ns
t_{C2CWRH} [1]	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.21	0.25	ns
t_{RSTBQ}	RESET Low to data out Low on RD (flow through)	0.94	1.11	ns
	RESET Low to data out Low on RD (pipelined)	0.94	1.11	ns
$t_{REMRSTB}$	RESET removal	0.29	0.34	ns
$t_{RECRSTB}$	RESET recovery	1.53	1.80	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.55	0.64	ns
t_{CYC}	Clock cycle time	5.10	5.87	ns
F_{MAX}	Maximum frequency	196	170	MHz

Note 1: For more information, refer to the application note *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-211: RAM512X18 – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V)

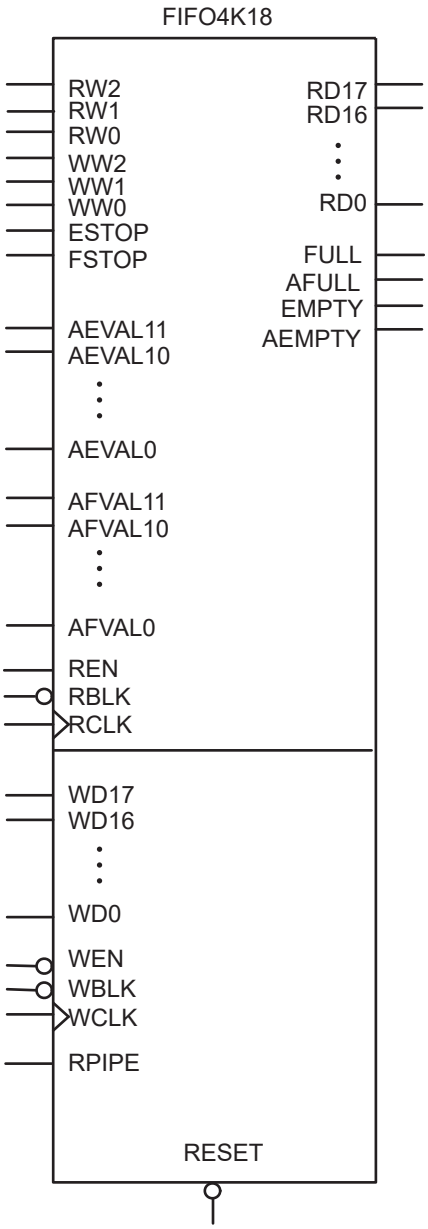
Parameter	Description	–1	Std.	Units
t_{AS}	Address setup time	0.33	0.39	ns
t_{AH}	Address hold time	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.12	0.14	ns
t_{ENH}	REN, WEN hold time	0.08	0.09	ns
t_{DS}	Input data (WD) setup time	0.24	0.29	ns
t_{DH}	Input data (WD) hold time	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained, WMODE = 0)	2.88	3.39	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	1.19	1.40	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.25	0.29	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.31	0.36	ns
t_{RSTBQ}	RESET Low to data out Low on RD (flow-through)	1.23	1.45	ns
	RESET Low to data out Low on RD (pipelined)	1.23	1.45	ns
$t_{REMRSTB}$	RESET removal	0.38	0.45	ns
$t_{RECRSTB}$	RESET recovery	2.00	2.35	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.63	0.72	ns
t_{CYC}	Clock cycle time	5.75	6.61	ns
F_{MAX}	Maximum frequency	174	151	MHz

Note 1: For more information, refer to the application note *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values

2.7.2 FIFO

FIGURE 2-46: FIFO MODEL



Timing Waveforms

FIGURE 2-47: FIFO READ

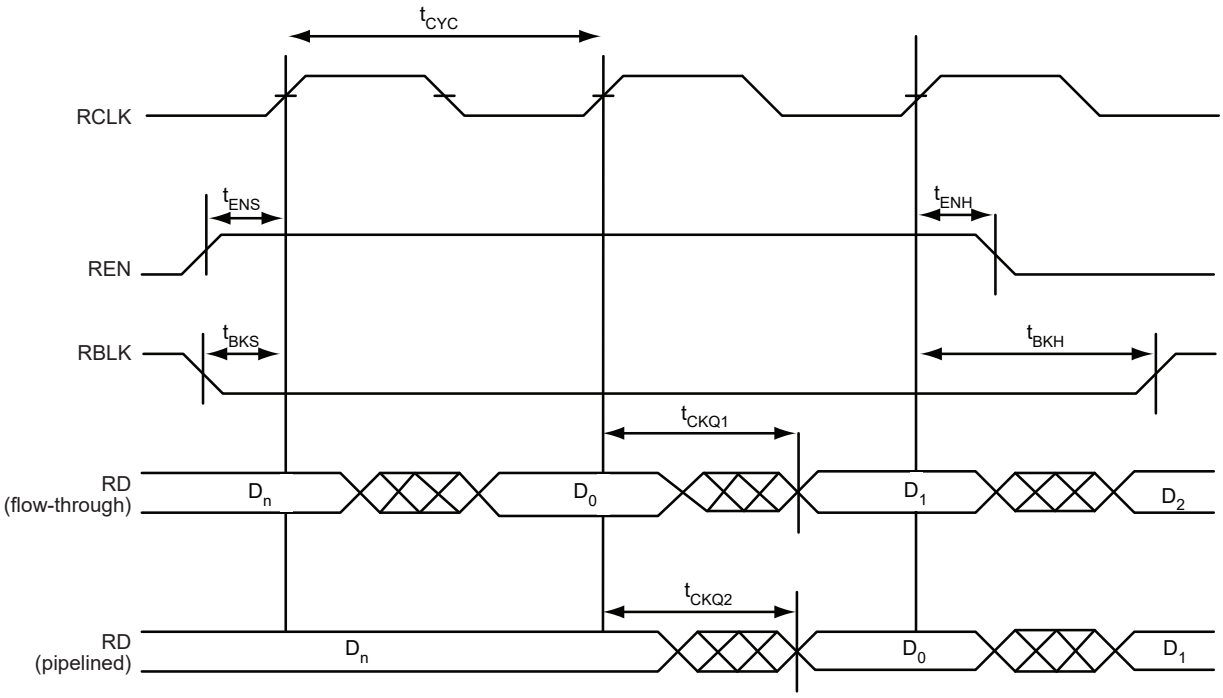


FIGURE 2-48: FIFO WRITE

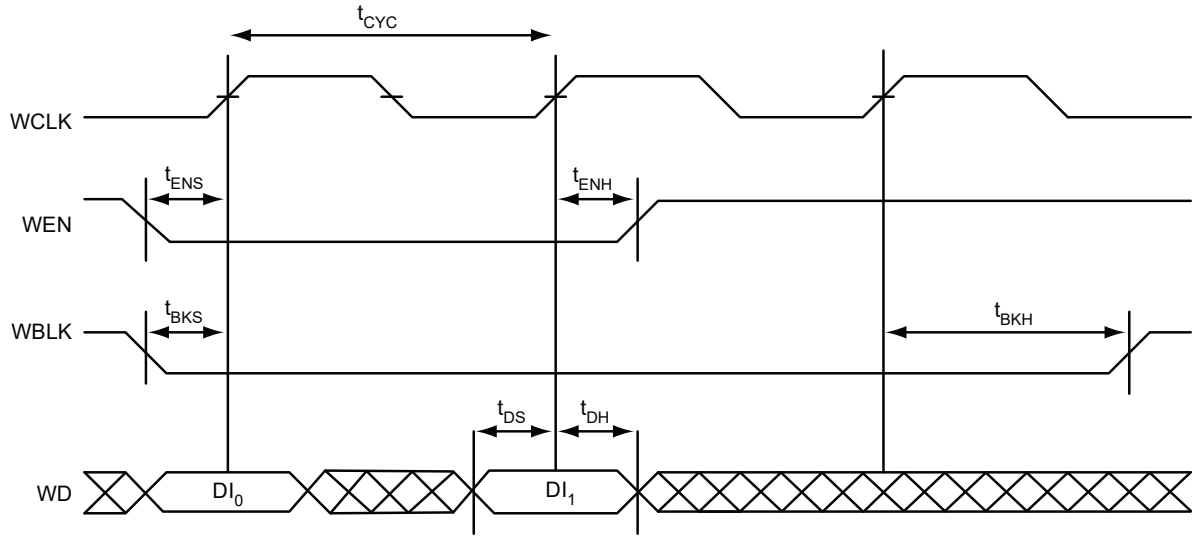


FIGURE 2-49: FIFO RESET

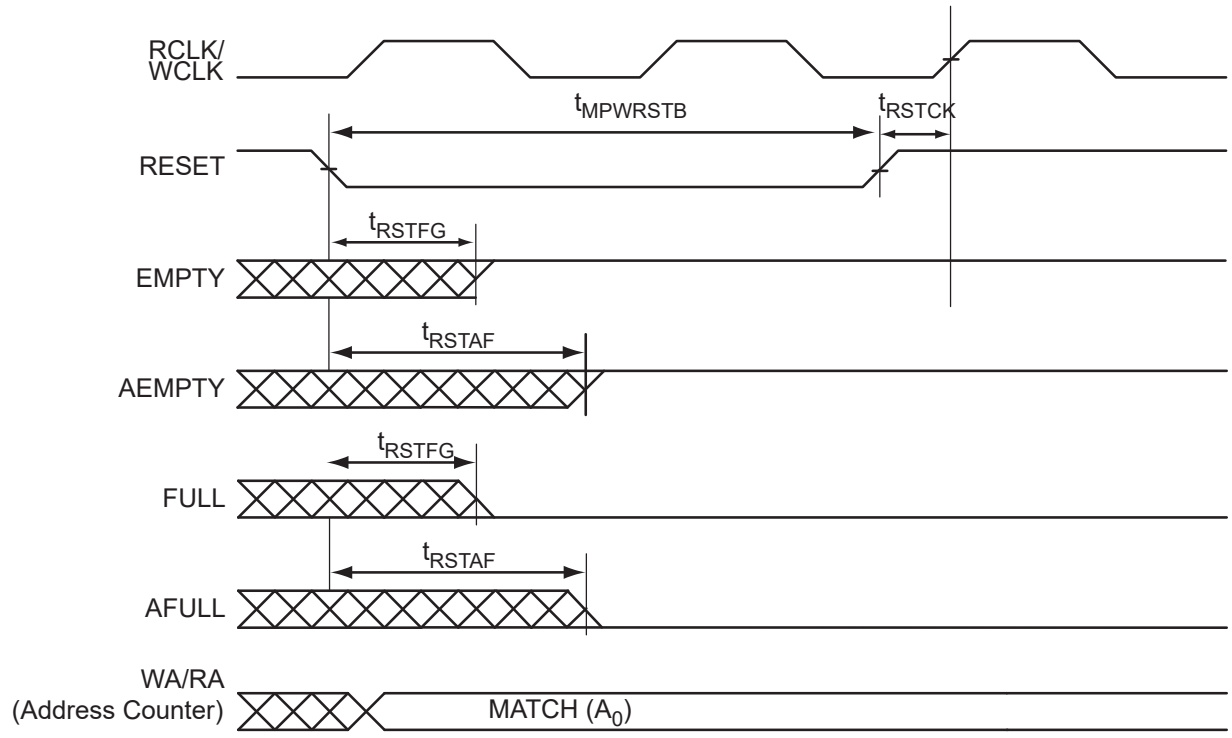


FIGURE 2-50: FIFO EMPTY FLAG AND AEMPTY FLAG ASSERTION

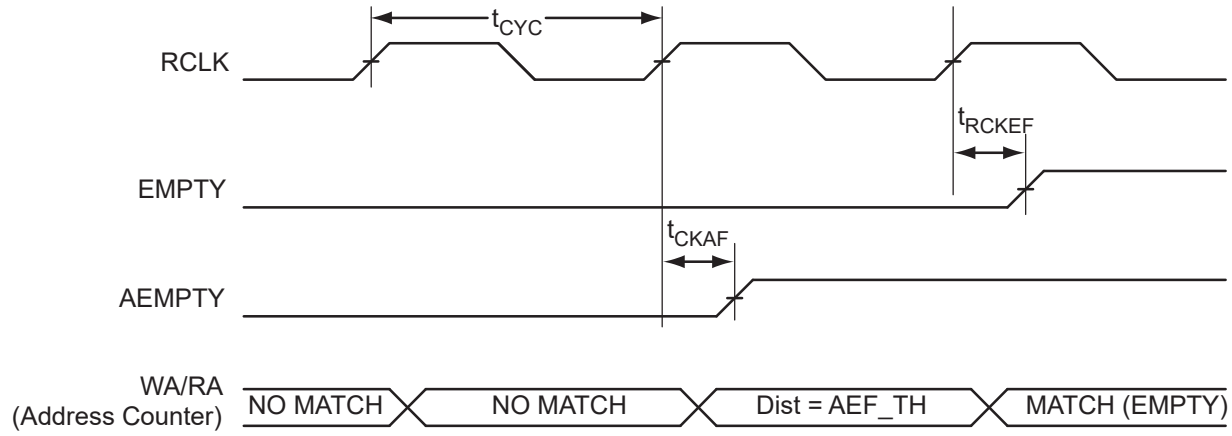


FIGURE 2-51: FIFO FULL FLAG AND AFULL FLAG ASSERTION

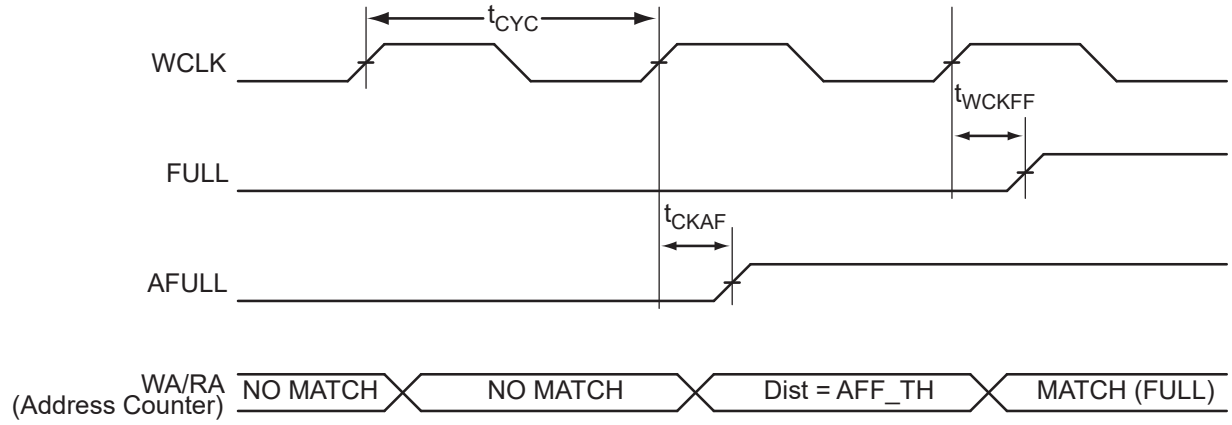


FIGURE 2-52: FIFO EMPTY FLAG AND AEMPTY FLAG DEASSERTION

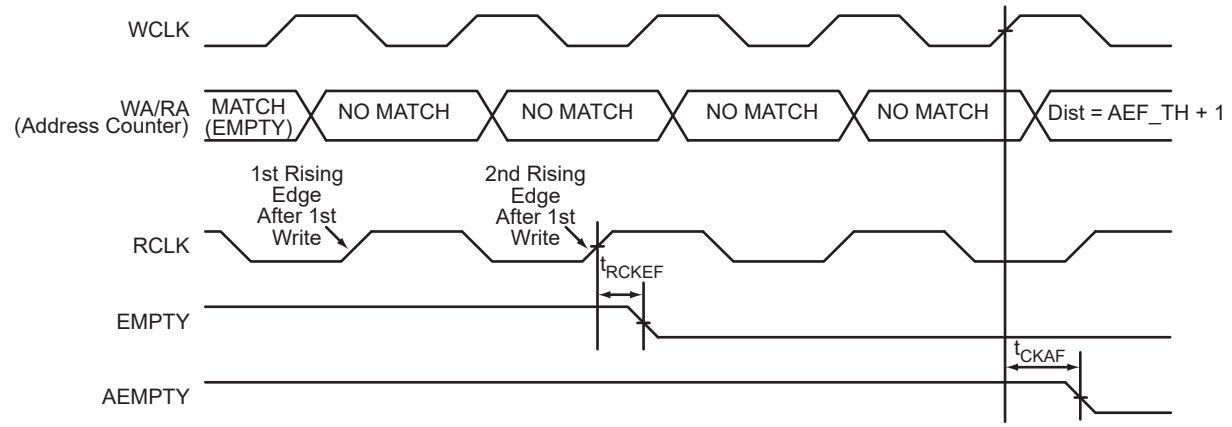
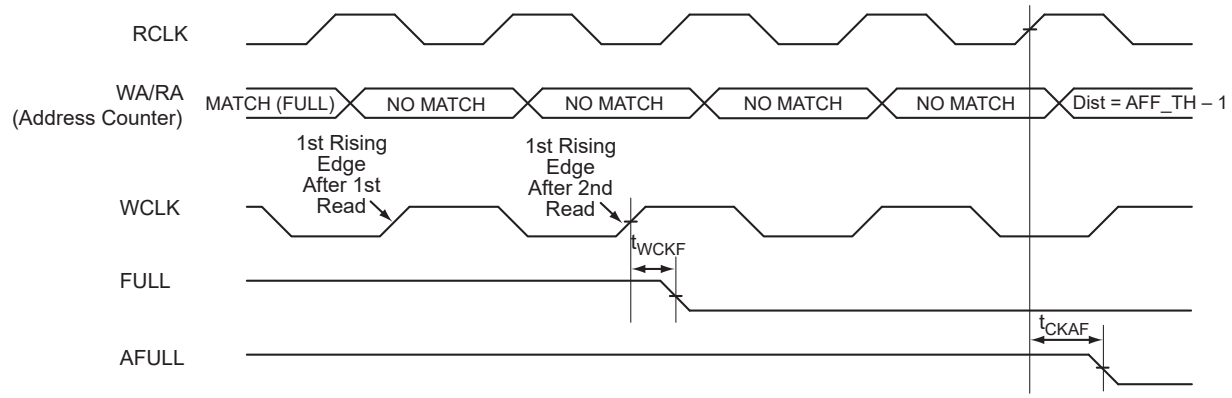


FIGURE 2-53: FIFO FULL FLAG AND AFULL FLAG DEASSERTION



2.7.2.1 Timing Characteristics

TABLE 2-212: FIFO – APPLIES TO 1.5 V DC CORE VOLTAGE (WORST COMMERCIAL-CASE CONDITIONS: T_J = 70°C, VCC = 1.425 V)

Parameter	Description	–1	Std.	Units
t_{ENS}	REN, WEN Setup Time	1.40	1.65	ns
t_{ENH}	REN, WEN Hold Time	0.02	0.02	ns
t_{BKS}	BLK Setup Time	0.40	0.47	ns
t_{BKH}	BLK Hold Time	0.00	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.19	0.22	ns
t_{DH}	Input Data (WD) Hold Time	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.40	2.83	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	0.91	1.07	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	1.75	2.06	ns
t_{WCKFF}	WCLK High to Full Flag Valid	1.66	1.96	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	6.31	7.42	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	1.73	2.03	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	6.25	7.35	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	0.94	1.11	ns
	RESET Low to Data Out Low on RD (pipelined)	0.94	1.11	ns
$t_{REMRSTB}$	RESET Removal	0.29	0.34	ns
$t_{RECRSTB}$	RESET Recovery	1.53	1.80	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.55	0.64	ns
t_{CYC}	Clock Cycle Time	5.10	5.87	ns
F_{MAX}	Maximum Frequency for FIFO	196	170	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

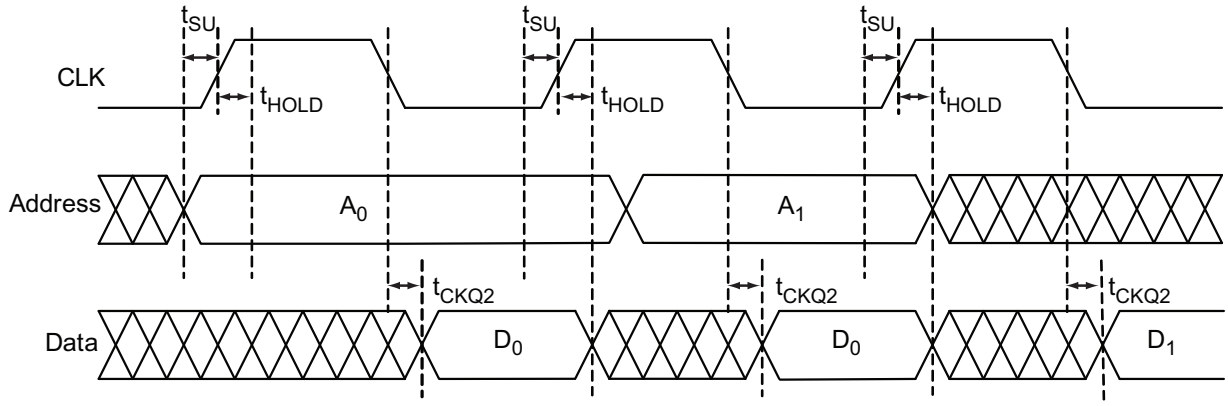
TABLE 2-213: FIFO – APPLIES TO 1.2 V DC CORE VOLTAGE (WORST COMMERCIAL-CASE CONDITIONS: T_J = 70°C, VCC = 1.14 V)

Parameter	Description	–1	Std.	Units
t_{ENS}	REN, WEN Setup Time	1.84	2.16	ns
t_{ENH}	REN, WEN Hold Time	0.02	0.03	ns
t_{BKS}	BLK Setup Time	0.40	0.47	ns
t_{BKH}	BLK Hold Time	0.00	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.24	0.29	ns
t_{DH}	Input Data (WD) Hold Time	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	3.14	3.69	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	1.19	1.40	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	2.29	2.69	ns
t_{WCKFF}	WCLK High to Full Flag Valid	2.18	2.56	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	8.25	9.70	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	2.26	2.65	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	8.17	9.60	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	1.23	1.45	ns
	RESET Low to Data Out Low on RD (pipelined)	1.23	1.45	ns
$t_{REMRSTB}$	RESET Removal	0.38	0.45	ns
$t_{RECRSTB}$	RESET Recovery	2.00	2.35	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.63	0.72	ns
t_{CYC}	Clock Cycle Time	5.75	6.61	ns
F_{MAX}	Maximum Frequency for FIFO	174	151	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.8 Embedded FlashROM Characteristics

FIGURE 2-54: TIMING DIAGRAM



2.8.1 TIMING CHARACTERISTICS

TABLE 2-214: EMBEDDED FLASHROM ACCESS TIME – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V)

Parameter	Description	–1	Std.	Units
t_{SU}	Address Setup Time	0.54	0.64	ns
t_{HOLD}	Address Hold Time	0.00	0.00	ns
t_{CK2Q}	Clock to Out	16.55	19.46	ns
F_{MAX}	Maximum Clock Frequency	15	15	MHz

TABLE 2-215: EMBEDDED FLASHROM ACCESS TIME– APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V)

Parameter	Description	–1	Std.	Units
t_{SU}	Address Setup Time	0.71	0.83	ns
t_{HOLD}	Address Hold Time	0.00	0.00	ns
t_{CK2Q}	Clock to Out	21.64	25.44	ns
F_{MAX}	Maximum Clock Frequency	15	15	MHz

2.9 JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the section User I/O Characteristics for more details.

2.9.1 TIMING CHARACTERISTICS

TABLE 2-216: JTAG 1532 – APPLIES TO 1.5 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425 V)

Parameter	Description	–1	Std.	Units
t_{DISU}	Test Data Input Setup Time	0.57	0.67	ns
t_{DIHD}	Test Data Input Hold Time	1.13	1.33	ns
t_{TMSSU}	Test Mode Select Setup Time	0.57	0.67	ns
t_{TMDHD}	Test Mode Select Hold Time	1.13	1.33	ns
t_{TCK2Q}	Clock to Q (data out)	5.67	6.67	ns
t_{RSTB2Q}	Reset to Q (data out)	22.67	26.67	ns
F_{TCKMAX}	TCK Maximum Frequency	24.00	21.00	MHz
$t_{TRSTREM}$	ResetB Removal Time	0.00	0.00	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.23	0.27	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-217: JTAG 1532 – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V)

Parameter	Description	–1	Std.	Units
t_{DISU}	Test Data Input Setup Time	0.75	0.88	ns
t_{DIHD}	Test Data Input Hold Time	1.50	1.76	ns
t_{TMSSU}	Test Mode Select Setup Time	0.75	0.88	ns
t_{TMDHD}	Test Mode Select Hold Time	1.50	1.76	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-217: JTAG 1532 – APPLIES TO 1.2 V DC CORE VOLTAGE (COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14 V)

Parameter	Description	–1	Std.	Units
t_{TCK2Q}	Clock to Q (data out)	6.00	7.06	ns
t_{RSTB2Q}	Reset to Q (data out)	25.00	29.41	ns
F_{TCKMAX}	TCK Maximum Frequency	20.00	17.00	MHz
$t_{TRSTREM}$	ResetB Removal Time	0.45	0.53	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.00	0.00	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

3.0 PIN DESCRIPTIONS AND PACKAGING

3.1 Supply Pins

GND **Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ **Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

VCC **Core Supply Voltage**

Supply voltage to the FPGA core, nominally 1.2 V or 1.5 V. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

VCC can be switched dynamically from 1.2 V to 1.5 V or vice versa. This allows in-system programming (ISP) when VCC is at 1.5 V and the benefit of low power operation when VCC is at 1.2 V.

VCCIBx **I/O Supply Voltage**

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are up to eight I/O banks on ProASIC3L low power flash devices plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. In general, unused I/O banks should have their corresponding VCCIX pins tied to GND. If an output pad is terminated to ground through any resistor and if the corresponding VCCIX is left floating, then the leakage current to ground is ~ 0uA. However, if an output pad is terminated to ground through any resistor and the corresponding VCCIX grounded, then the leakage current to ground is ~ 3 uA. For unused banks the aforementioned behavior is to be taken into account while deciding if it’s better to float VCCIX of unused bank or tie it to GND.

VMVx **I/O Supply Voltage (quiet)**

Quiet supply voltage to the input buffers of each I/O bank. *x* is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (i.e., VMV0 to VCCIB0, VMV1 to VCCIB1, etc.).

VCCPLA/B/C/D/E/F **PLL Supply Voltage**

Supply voltage to analog PLL, nominally 1.5 V or 1.2 V for ProASIC3 devices

When the PLLs are not used, the Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microchip recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. Refer to the PLL Power Supply Decoupling section of the "Clock Conditioning Circuits in IGLOO and ProASIC3 Devices" chapter of the *ProASIC3L FPGA Fabric User’s Guide* for a complete board solution for the PLL analog power supply and ground. There is one VCCPLF pin on ProASIC3L devices.

VCOMPLA/B/C/D/E/F **PLL Ground**

Ground to analog PLL power supplies. When the PLLs are not used, the Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. There is one VCOMPLF pin on ProASIC3L devices.

VJTAG JTAG Supply Voltage

ProASIC3L devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND. It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a device is in a JTAG chain of interconnected boards, the board containing the device can be powered down, provided both VJTAG and VCC to the part remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode.

Microchip recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

VPUMP Programming Supply Voltage

ProASIC3Ldevices support single-voltage ISP of the configuration flash and FlashROM. For programming, VPUMP should be 3.3 V nominal. During normal device operation, VPUMP can be left floating or can be tied (pulled up) to any voltage between 0 V and the VPUMP maximum. Programming power supply voltage (VPUMP) range is listed in the datasheet.

When the VPUMP pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 µF and 0.33 µF capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Microchip recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

3.2 User Pins

I/O User Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to VCCI. With VCCI, VMV, and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

GL Globals

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits in IGLOO and ProASIC3 Devices" chapter of the *ProASIC3L FPGA Fabric User's Guide*. All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

Refer to the "I/O Structures in IGLOO and ProASIC3 Devices" chapter of the *ProASIC3L FPGA Fabric User's Guide* for an explanation of the naming of global pins.

FF Flash*Freeze Mode Activation Pin

Flash*Freeze mode is available on ProASIC3L devices. The FF pin is a dedicated input pin used to enter and exit Flash*Freeze mode. The FF pin is active low, has the same characteristics as a single-ended I/O, and must meet the maximum rise and fall times. When Flash*Freeze mode is not used in the design, the FF pin is available as a regular I/O.

When Flash*Freeze mode is used, the FF pin must not be left floating, to avoid accidentally entering Flash*Freeze mode. While in Flash*Freeze mode, the Flash*Freeze pin should be constantly asserted.

The Flash*Freeze pin can be used with any single-ended I/O standard supported by the I/O bank in which the pin is located, and input signal levels compatible with the I/O standard selected. The FF pin should be treated as a sensitive asynchronous signal. When defining pin placement and board layout, simultaneously switching outputs (SSOs) and their effects on sensitive asynchronous pins must be considered.

Unused FF or I/O pins are tristated with weak pull-up. This default configuration applies to both Flash*Freeze mode and normal operation mode. No user intervention is required.

Table 3-1 shows the Flash*Freeze pin location on the available packages ProASIC3L devices. The Flash*Freeze pin location is independent of device (except for the PQ208 package), allowing migration to larger or smaller devices while maintaining the same pin location on the board. Refer to the "Flash*Freeze Technology and Low Power Modes" chapter of the *ProASIC3L FPGA Fabric User's Guide* for more information on I/O states during Flash*Freeze mode.

TABLE 3-1: FLASH*FREEZE PIN LOCATION

ProASIC3L Package	Flash*Freeze Pin
VQ100	27
FG144	L3
FG256	T3
FG324	R5
FG484	W6
FG896	AH4
PQ208 PQ208-A3P1000L PQ208-A3PE3000L	 55 58

3.3 JTAG Pins

ProASIC3L devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Microchip recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to Table 3-2 for more information.

TABLE 3-2: RECOMMENDED TIE-OFF VALUES FOR THE TCK AND TRST PINS

VJTAG	Tie-Off Resistance
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

Note 1: Equivalent parallel resistance if more than one device is on the JTAG chain

2: The TCK pin can be pulled up/down.

3: The TRST pin is pulled down.

TDI Test Data Input

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

TMS **Test Mode Select**

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

TRST **Boundary Scan Reset Pin**

The TRST pin functions as an active-low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 3-2 and must satisfy the parallel resistance value requirement. The values in Table 3-2 correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microchip recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements.

3.4 Special Function Pins

NC **No Connect**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

DC **Do Not Connect**

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

3.5 Packaging

Semiconductor technology is constantly shrinking in size while growing in capability and functional integration. To enable next-generation silicon technologies, semiconductor packages have also evolved to provide improved performance and flexibility.

Microchip consistently delivers packages that provide the necessary mechanical and environmental protection to ensure consistent reliability and performance. Microchip IC packaging technology efficiently supports high-density FPGAs with large-pin-count Ball Grid Arrays (BGAs), but is also flexible enough to accommodate stringent form factor requirements for Chip Scale Packaging (CSP). In addition, Microchip offers a variety of packages designed to meet your most demanding application and economic requirements for today's embedded and mobile systems.

3.6 Related Documents

3.6.1 USER'S GUIDES

ProASICL FPGA Fabric User's Guide

http://www.microsemi.com/soc/documents/PA3L_UG.pdf

3.6.2 PACKAGING

The following documents provide packaging information and device selection for low power flash devices.

3.6.3 *PRODUCT CATALOG*

http://www.microsemi.com/soc/documents/ProdCat_PIB.pdf

Lists devices currently recommended for new designs and the packages available for each member of the family. Use this document or the datasheet tables to determine the best package for your design, and which package drawing to use.

3.6.4 *PACKAGE MECHANICAL DRAWINGS*

http://www.microsemi.com/soc/documents/PckgMechDrwngs.pdf

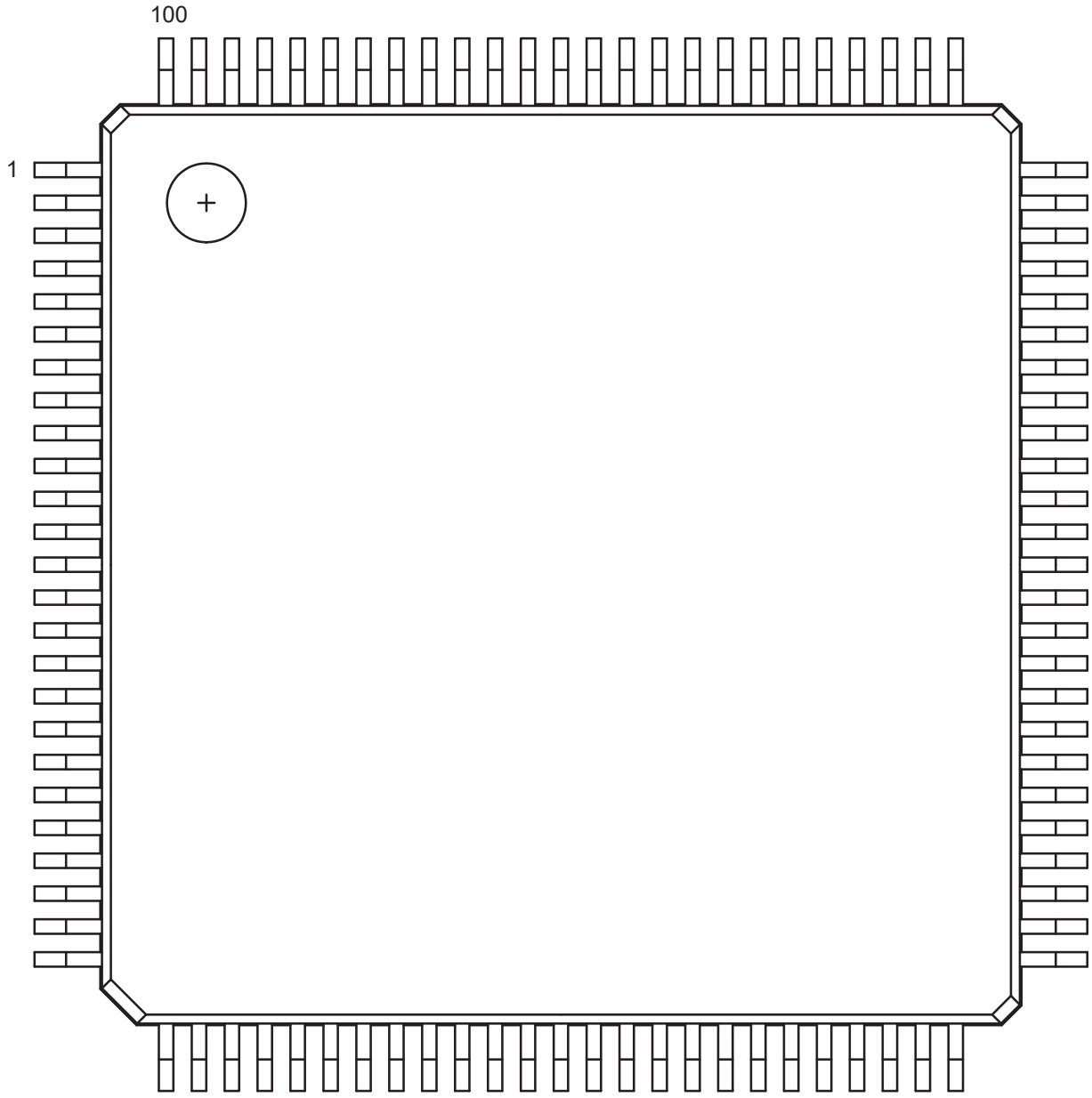
This document contains the package mechanical drawings for all packages currently or previously supplied by Microchip. Use the bookmarks to navigate to the package mechanical drawings.

Additional packaging materials: *http://www.microsemi.com/soc/products/solutions/package/docs.aspx*.

4.0 PACKAGE PIN ASSIGNMENTS

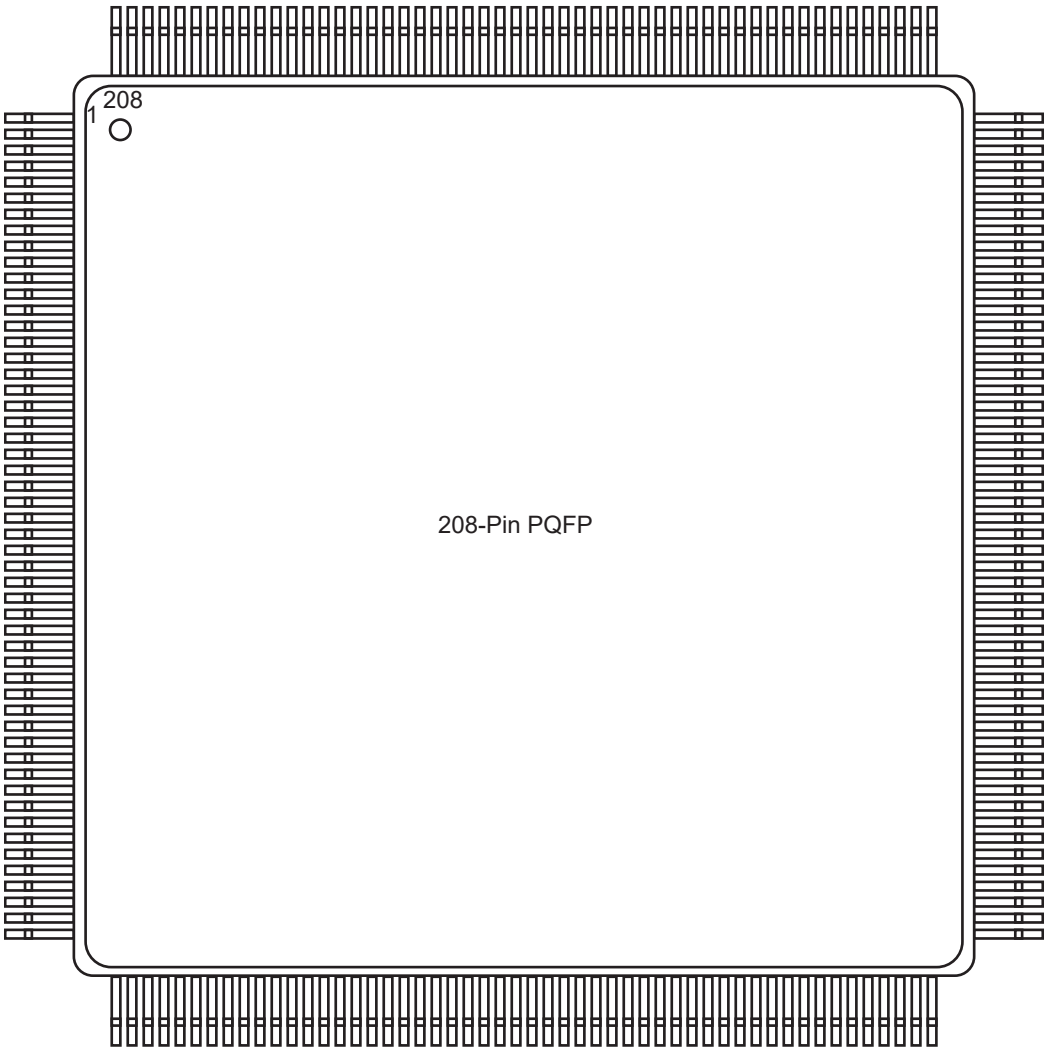
4.1 VQ100 - Top View

Note: For Package Manufacturing and Environmental information, visit the Resource Center at *http://www.microsemi.com./soc/products/solutions/package/docs.aspx*.



4.2 PQ208 - Top View

Note: For Package Manufacturing and Environmental information, visit the Resource Center at *http://www.microsemi.com/soc/products/solutions/package/docs.aspx*.


208
1
208-Pin PQFP

PQ208	
Pin Number	**APL1000 Function**
1	GND
2	GAA2/IO225PDB3
3	IO225NDB3
4	GAB2/IO224PDB3
5	IO224NDB3
6	GAC2/IO223PDB3
7	IO223NDB3
8	IO222PDB3
9	IO222NDB3
10	IO220PDB3
11	IO220NDB3
12	IO218PDB3
13	IO218NDB3
14	IO216PDB3
15	IO216NDB3
16	VCC
17	GND
18	VCCIB3
19	IO212PDB3
20	IO212NDB3
21	GFC1/IO209PDB3
22	GFC0/IO209NDB3
23	GFB1/IO208PDB3
24	GFB0/IO208NDB3
25	VCOMPLF
26	GFA0/IO207NPB3
27	VCCPLF
28	GFA1/IO207PPB3
29	GND
30	GFA2/IO206PDB3
31	IO206NDB3
32	GFB2/IO205PDB3
33	IO205NDB3
34	GFC2/IO204PDB3
35	IO204NDB3
36	VCC
37	IO199PDB3
38	IO199NDB3
39	IO197PSB3
40	VCCIB3
41	GND
42	IO191PDB3
43	IO191NDB3
44	GEC1/IO190PDB3

PQ208	
Pin Number	**APL1000 Function**
45	GEC0/IO190NDB3
46	GEB1/IO189PDB3
47	GEB0/IO189NDB3
48	GEA1/IO188PDB3
49	GEA0/IO188NDB3
50	VMV3
51	GNDQ
52	GND
53	VMV2
54	GEA2/IO187RSB2
55	FF/GEB2/IO186RSB2
56	GEC2/IO185RSB2
57	IO184RSB2
58	IO183RSB2
59	IO182RSB2
60	IO181RSB2
61	IO180RSB2
62	VCCIB2
63	IO178RSB2
64	IO176RSB2
65	GND
66	IO174RSB2
67	IO172RSB2
68	IO170RSB2
69	IO168RSB2
70	IO166RSB2
71	VCC
72	VCCIB2
73	IO162RSB2
74	IO160RSB2
75	IO158RSB2
76	IO156RSB2
77	IO154RSB2
78	IO152RSB2
79	IO150RSB2
80	IO148RSB2
81	GND
82	IO143RSB2
83	IO141RSB2
84	IO139RSB2
85	IO137RSB2
86	IO135RSB2
87	IO133RSB2
88	VCC

PQ208	
Pin Number	**APL1000 Function**
89	VCCIB2
90	IO128RSB2
91	IO126RSB2
92	IO124RSB2
93	IO122RSB2
94	IO120RSB2
95	IO118RSB2
96	GDC2/IO116RSB2
97	GND
98	GDB2/IO115RSB2
99	GDA2/IO114RSB2
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV2
105	GND
106	VPUMP
107	GNDQ
108	TDO
109	TRST
110	VJTAG
111	GDA0/IO113NDB1
112	GDA1/IO113PDB1
113	GDB0/IO112NDB1
114	GDB1/IO112PDB1
115	GDC0/IO111NDB1
116	GDC1/IO111PDB1
117	IO109NDB1
118	IO109PDB1
119	IO106NDB1
120	IO106PDB1
121	IO104PSB1
122	GND
123	VCCIB1
124	IO99NDB1
125	IO99PDB1
126	NC
127	IO96NDB1
128	GCC2/IO96PDB1
129	GCB2/IO95PSB1
130	GND
131	GCA2/IO94PSB1
132	GCA1/IO93PDB1

PQ208	
Pin Number	**APL1000 Function**
133	GCA0/IO93NDB1
134	GCB0/IO92NDB1
135	GCB1/IO92PDB1
136	GCC0/IO91NDB1
137	GCC1/IO91PDB1
138	IO88NDB1
139	IO88PDB1
140	VCCIB1
141	GND
142	VCC
143	IO86PSB1
144	IO84NDB1
145	IO84PDB1
146	IO82NDB1
147	IO82PDB1
148	IO80NDB1
149	GBC2/IO80PDB1
150	IO79NDB1
151	GBB2/IO79PDB1
152	IO78NDB1
153	GBA2/IO78PDB1
154	VMV1
155	GNDQ
156	GND
157	VMV0
158	GBA1/IO77RSB0
159	GBA0/IO76RSB0
160	GBB1/IO75RSB0
161	GBB0/IO74RSB0
162	GND
163	GBC1/IO73RSB0
164	GBC0/IO72RSB0
165	IO70RSB0
166	IO67RSB0
167	IO63RSB0
168	IO60RSB0
169	IO57RSB0
170	VCCIB0
171	VCC
172	IO54RSB0
173	IO51RSB0
174	IO48RSB0
175	IO45RSB0
176	IO42RSB0

PQ208	
Pin Number	**APL1000 Function**
177	IO40RSB0
178	GND
179	IO38RSB0
180	IO35RSB0
181	IO33RSB0
182	IO31RSB0
183	IO29RSB0
184	IO27RSB0
185	IO25RSB0
186	VCCIB0
187	VCC
188	IO22RSB0
189	IO20RSB0
190	IO18RSB0
191	IO16RSB0
192	IO15RSB0
193	IO14RSB0
194	IO13RSB0
195	GND
196	IO12RSB0
197	IO11RSB0
198	IO10RSB0
199	IO09RSB0
200	VCCIB0
201	GAC1/IO05RSB0
202	GAC0/IO04RSB0
203	GAB1/IO03RSB0
204	GAB0/IO02RSB0
205	GAA1/IO01RSB0
206	GAA0/IO00RSB0
207	GNDQ
208	VMV0

PQ208	
Pin Number	**A3PE3000L Function**
1	GND
2	GNDQ
3	VMV7
4	GAB2/IO308PSB7V4
5	GAA2/IO309PDB7V4
6	IO309NDB7V4
7	GAC2/IO307PDB7V4
8	IO307NDB7V4
9	IO303PDB7V3
10	IO303NDB7V3
11	IO299PDB7V3
12	IO299NDB7V3
13	IO295PDB7V2
14	IO295NDB7V2
15	IO291PSB7V2
16	VCC
17	GND
18	VCCIB7
19	IO285PDB7V1
20	IO285NDB7V1
21	IO279PSB7V0
22	GFC1/IO275PSB7V0
23	GFB1/IO274PDB7V0
24	GFB0/IO274NDB7V0
25	VCOMPLF
26	GFA0/IO273NPB6V4
27	VCCPLF
28	GFA1/IO273PPB6V4
29	GND
30	GFA2/IO272PDB6V4
31	IO272NDB6V4
32	GFB2/IO271PPB6V4
33	GFC2/IO270PPB6V4
34	IO271NPB6V4
35	IO270NPB6V4
36	VCC
36	VCC
37	IO252PDB6V2
38	IO252NDB6V2
39	IO248PSB6V1
40	VCCIB6
41	GND
42	IO244PDB6V1
43	IO244NDB6V1

PQ208	
Pin Number	**A3PE3000L Function**
44	GEC1/IO236PDB6V0
45	GEC0/IO236NDB6V0
46	GEB1/IO235PPB6V0
47	GEA1/IO234PPB6V0
48	GEB0/IO235NPB6V0
49	GEA0/IO234NPB6V0
50	VMV6
51	GNDQ
52	GND
53	VMV5
54	GNDQ
55	IO233NDB5V4
56	GEA2/IO233PDB5V4
57	IO232NDB5V4
58	FF/GEB2/IO232PDB5V4
59	IO231NDB5V4
60	GEC2/IO231PDB5V4
61	IO230PSB5V4
62	VCCIB5
62	VCCIB5
63	IO218NDB5V3
64	IO218PDB5V3
65	GND
66	IO214PSB5V2
67	IO212NDB5V2
68	IO212PDB5V2
69	IO208NDB5V1
70	IO208PDB5V1
71	VCC
72	VCCIB5
73	IO202NDB5V1
74	IO202PDB5V1
75	IO198NDB5V0
76	IO198PDB5V0
77	IO197NDB5V0
78	IO197PDB5V0
79	IO194NDB5V0
80	IO194PDB5V0
81	GND
82	IO184NDB4V3
83	IO184PDB4V3
84	IO180NDB4V3
85	IO180PDB4V3
86	IO176NDB4V2

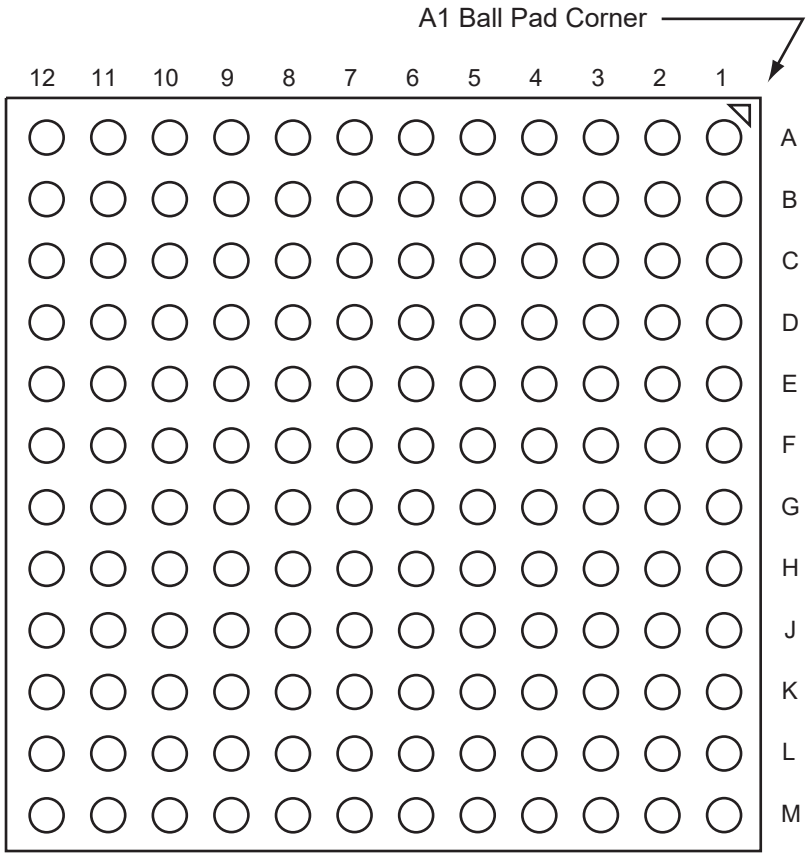
PQ208	
Pin Number	**A3PE3000L Function**
87	IO176PDB4V2
88	VCC
89	VCCIB4
90	IO170NDB4V2
91	IO170PDB4V2
92	IO166NDB4V1
93	IO166PDB4V1
94	IO156NDB4V0
95	GDC2/IO156PDB4V0
96	IO154NPB4V0
97	GND
98	GDB2/IO155PSB4V0
99	GDA2/IO154PPB4V0
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV4
105	GND
106	VPUMP
107	GNDQ
108	TDO
109	TRST
110	VJTAG
111	VMV3
112	GDA0/IO153NPB3V4
113	GDB0/IO152NPB3V4
114	GDA1/IO153PPB3V4
115	GDB1/IO152PPB3V4
116	GDC0/IO151NDB3V4
117	GDC1/IO151PDB3V4
118	IO134NDB3V2
119	IO134PDB3V2
120	IO132NDB3V2
121	IO132PDB3V2
122	GND
123	VCCIB3
124	GCC2/IO117PSB3V0
125	GCB2/IO116PSB3V0
126	NC
127	IO115NDB3V0
128	GCA2/IO115PDB3V0
129	GCA1/IO114PPB3V0
130	GND

PQ208	
Pin Number	**A3PE3000L Function**
131	VCCPLC
132	GCA0/IO114NPB3V0
133	VCOMPLC
134	GCB0/IO113NDB2V3
135	GCB1/IO113PDB2V3
136	GCC1/IO112PSB2V3
137	IO110NDB2V3
138	IO110PDB2V3
139	IO106PSB2V3
140	VCCIB2
141	GND
142	VCC
143	IO99NDB2V2
144	IO99PDB2V2
145	IO96NDB2V1
146	IO96PDB2V1
147	IO91NDB2V1
148	IO91PDB2V1
149	IO88NDB2V0
150	IO88PDB2V0
151	GBC2/IO84PSB2V0
152	GBA2/IO82PSB2V0
153	GBB2/IO83PSB2V0
154	VMV2
155	GNDQ
156	GND
157	VMV1
158	GNDQ
159	GBA1/IO81PDB1V4
160	GBA0/IO81NDB1V4
161	GBB1/IO80PDB1V4
162	GND
163	GBB0/IO80NDB1V4
164	GBC1/IO79PDB1V4
165	GBC0/IO79NDB1V4
166	IO74PDB1V4
167	IO74NDB1V4
168	IO70PDB1V3
169	IO70NDB1V3
170	VCCIB1
171	VCC
171	VCC
172	IO56PSB1V1
173	IO55PDB1V1

PQ208	
Pin Number	**A3PE3000L Function**
174	IO55NDB1V1
175	IO54PDB1V1
176	IO54NDB1V1
177	IO40PDB0V4
178	GND
179	IO40NDB0V4
180	IO37PDB0V4
181	IO37NDB0V4
182	IO35PDB0V4
183	IO35NDB0V4
184	IO32PDB0V3
185	IO32NDB0V3
186	VCCIB0
187	VCC
188	IO28PDB0V3
189	IO28NDB0V3
190	IO24PDB0V2
191	IO24NDB0V2
192	IO21PSB0V2
193	IO16PDB0V1
194	IO16NDB0V1
195	GND
196	IO11PDB0V1
197	IO11NDB0V1
198	IO08PDB0V0
199	IO08NDB0V0
200	VCCIB0
201	GAC1/IO02PDB0V0
202	GAC0/IO02NDB0V0
203	GAB1/IO01PDB0V0
204	GAB0/IO01NDB0V0
205	GAA1/IO00PDB0V0
206	GAA0/IO00NDB0V0
207	GNDQ
208	VMV0

4.3 FG144 - Bottom View

Note: For Package Manufacturing and Environmental information, visit the Resource Center at *http://www.microsemi.com/soc/products/solutions/package/docs.aspx*.


A1 Ball Pad Corner
12 11 10 9 8 7 6 5 4 3 2 1
A
B
C
D
E
F
G
H
J
K
L
M

FG144	
Pin Number	**A3P600L Function**
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO10RSB0
A6	GND
A7	IO34RSB0
A8	VCC
A9	IO50RSB0
A10	GBA0/IO58RSB0
A11	GBA1/IO59RSB0
A12	GNDQ
B1	GAB2/IO173PDB3
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO13RSB0
B6	IO19RSB0
B7	IO31RSB0
B8	IO39RSB0
B9	GBB0/IO56RSB0
B10	GBB1/IO57RSB0
B11	GND
B12	VMV1
C1	IO173NDB3
C2	GFA2/IO161PPB3
C3	GAC2/IO172PDB3
C4	VCC
C5	IO16RSB0
C6	IO25RSB0
C7	IO28RSB0
C8	IO42RSB0
C9	IO45RSB0
C10	GBA2/IO60PDB1
C11	IO60NDB1
C12	GBC2/IO62PPB1
D1	IO169PDB3
D2	IO169NDB3
D3	IO172NDB3
D4	GAA2/IO174PPB3
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO54RSB0
D8	GBC1/IO55RSB0

FG144	
Pin Number	**A3P600L Function**
D9	GBB2/IO61PDB1
D10	IO61NDB1
D11	IO62NPB1
D12	GCB1/IO70PPB1
E1	VCC
E2	GFC0/IO164NDB3
E3	GFC1/IO164PDB3
E4	VCCIB3
E5	IO174NPB3
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO69PDB1
E9	VCCIB1
E10	VCC
E11	GCA0/IO71NDB1
E12	IO72NDB1
F1	GFB0/IO163NPB3
F2	VCOMPLF
F3	GFB1/IO163PPB3
F4	IO161NPB3
F5	GND
F6	GND
F7	GND
F8	GCC0/IO69NDB1
F9	GCB0/IO70NPB1
F10	GND
F11	GCA1/IO71PDB1
F12	GCA2/IO72PDB1
G1	GFA1/IO162PPB3
G2	GND
G3	VCCPLF
G4	GFA0/IO162NPB3
G5	GND
G6	GND
G7	GND
G8	GDC1/IO86PPB1
G9	IO74NDB1
G10	GCC2/IO74PDB1
G11	IO73NDB1
G12	GCB2/IO73PDB1
H1	VCC
H2	GFB2/IO160PDB3
H3	GFC2/IO159PSB3
H4	GEC1/IO146PDB3

FG144	
Pin Number	**A3P600L Function**
H5	VCC
H6	IO80PDB1
H7	IO80NDB1
H8	GDB2/IO90RSB2
H9	GDC0/IO86NPB1
H10	VCCIB1
H11	IO84PSB1
H12	VCC
J1	GEB1/IO145PDB3
J2	IO160NDB3
J3	VCCIB3
J4	GEC0/IO146NDB3
J5	IO129RSB2
J6	IO131RSB2
J7	VCC
J8	TCK
J9	GDA2/IO89RSB2
J10	TDO
J11	GDA1/IO88PDB1
J12	GDB1/IO87PDB1
K1	GEB0/IO145NDB3
K2	GEA1/IO144PDB3
K3	GEA0/IO144NDB3
K4	GEA2/IO143RSB2
K5	IO119RSB2
K6	IO111RSB2
K7	GND
K8	IO94RSB2
K9	GDC2/IO91RSB2
K10	GND
K11	GDA0/IO88NDB1
K12	GDB0/IO87NDB1
L1	GND
L2	VMV3
L3	FF/GEB2/IO142RSB2
L4	IO136RSB2
L5	VCCIB2
L6	IO115RSB2
L7	IO103RSB2
L8	IO97RSB2
L9	TMS
L10	VJTAG
L11	VMV2
L12	TRST

FG144	
Pin Number	**A3P600L Function**
M1	GNDQ
M2	GEC2/IO141RSB2
M3	IO138RSB2
M4	IO123RSB2
M5	IO126RSB2
M6	IO134RSB2
M7	IO108RSB2
M8	IO99RSB2
M9	TDI
M10	VCCIB2
M11	VPUMP
M12	GNDQ

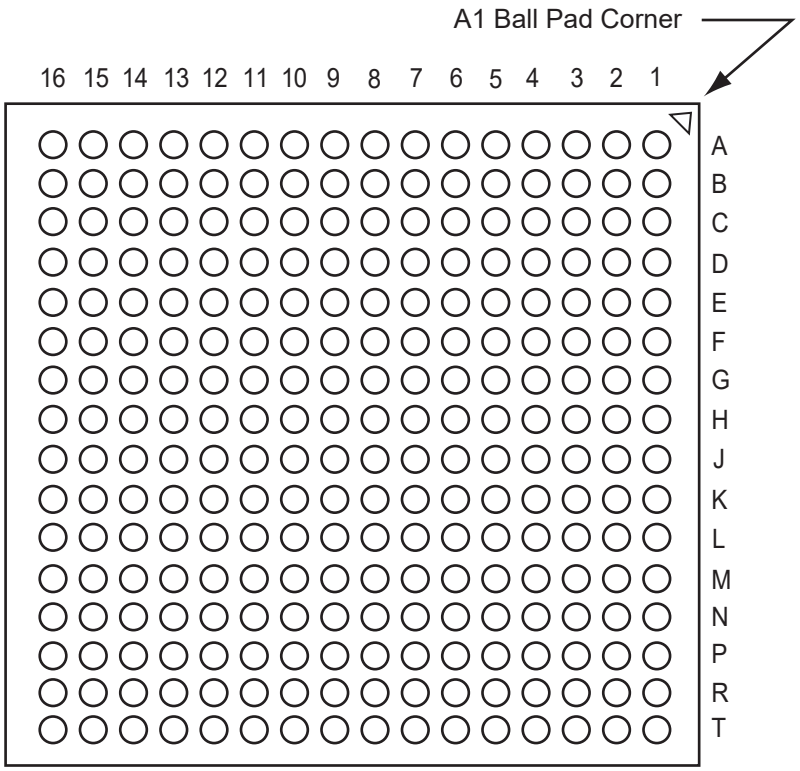
FG144	
Pin Number	**A3P1000L Function**
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO10RSB0
A6	GND
A7	IO44RSB0
A8	VCC
A9	IO69RSB0
A10	GBA0/IO76RSB0
A11	GBA1/IO77RSB0
A12	GNDQ
B1	GAB2/IO224PDB3
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO13RSB0
B6	IO26RSB0
B7	IO35RSB0
B8	IO60RSB0
B9	GBB0/IO74RSB0
B10	GBB1/IO75RSB0
B11	GND
B12	VMV1
C1	IO224NDB3
C2	GFA2/IO206PPB3
C3	GAC2/IO223PDB3
C4	VCC
C5	IO16RSB0
C6	IO29RSB0
C7	IO32RSB0
C8	IO63RSB0
C9	IO66RSB0
C10	GBA2/IO78PDB1
C11	IO78NDB1
C12	GBC2/IO80PPB1
D1	IO213PDB3
D2	IO213NDB3
D3	IO223NDB3
D4	GAA2/IO225PPB3
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO72RSB0
D8	GBC1/IO73RSB0

FG144	
Pin Number	**A3P1000L Function**
D9	GBB2/IO79PDB1
D10	IO79NDB1
D11	IO80NPB1
D12	GCB1/IO92PPB1
E1	VCC
E2	GFC0/IO209NDB3
E3	GFC1/IO209PDB3
E4	VCCIB3
E5	IO225NPB3
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO91PDB1
E9	VCCIB1
E10	VCC
E11	GCA0/IO93NDB1
E12	IO94NDB1
F1	GFB0/IO208NPB3
F2	VCOMPLF
F3	GFB1/IO208PPB3
F4	IO206NPB3
F5	GND
F6	GND
F7	GND
F8	GCC0/IO91NDB1
F9	GCB0/IO92NPB1
F10	GND
F11	GCA1/IO93PDB1
F12	GCA2/IO94PDB1
G1	GFA1/IO207PPB3
G2	GND
G3	VCCPLF
G4	GFA0/IO207NPB3
G5	GND
G6	GND
G7	GND
G8	GDC1/IO111PPB1
G9	IO96NDB1
G10	GCC2/IO96PDB1
G11	IO95NDB1
G12	GCB2/IO95PDB1
H1	VCC
H2	GFB2/IO205PDB3
H3	GFC2/IO204PSB3
H4	GEC1/IO190PDB3

FG144	
Pin Number	**A3P1000L Function**
H5	VCC
H6	IO105PDB1
H7	IO105NDB1
H8	GDB2/IO115RSB2
H9	GDC0/IO111NPB1
H10	VCCIB1
H11	IO101PSB1
H12	VCC
J1	GEB1/IO189PDB3
J2	IO205NDB3
J3	VCCIB3
J4	GEC0/IO190NDB3
J5	IO160RSB2
J6	IO157RSB2
J7	VCC
J8	TCK
J9	GDA2/IO114RSB2
J10	TDO
J11	GDA1/IO113PDB1
J12	GDB1/IO112PDB1
K1	GEB0/IO189NDB3
K2	GEA1/IO188PDB3
K3	GEA0/IO188NDB3
K4	GEA2/IO187RSB2
K5	IO169RSB2
K6	IO152RSB2
K7	GND
K8	IO117RSB2
K9	GDC2/IO116RSB2
K10	GND
K11	GDA0/IO113NDB1
K12	GDB0/IO112NDB1
L1	GND
L2	VMV3
L3	FF/GEB2/IO186RSB2
L4	IO172RSB2
L5	VCCIB2
L6	IO153RSB2
L7	IO144RSB2
L8	IO140RSB2
L9	TMS
L10	VJTAG
L11	VMV2
L12	TRST

FG144	
Pin Number	**A3P1000L Function**
M1	GNDQ
M2	GEC2/IO185RSB2
M3	IO173RSB2
M4	IO168RSB2
M5	IO161RSB2
M6	IO156RSB2
M7	IO145RSB2
M8	IO141RSB2
M9	TDI
M10	VCCIB2
M11	VPUMP
M12	GNDQ

4.4 FG256 - Bottom View



Note: For Package Manufacturing and Environmental information, visit the Resource Center at *http://www.microsemi.com/soc/products/solutions/package/docs.aspx*.

FG256	
Pin Number	**A3P1000L Function**
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO16RSB0
A6	IO22RSB0
A7	IO28RSB0
A8	IO35RSB0
A9	IO45RSB0
A10	IO50RSB0
A11	IO55RSB0
A12	IO61RSB0
A13	GBB1/IO75RSB0
A14	GBA0/IO76RSB0
A15	GBA1/IO77RSB0
A16	GND
B1	GAB2/IO224PDB3
B2	GAA2/IO225PDB3
B3	GNDQ
B4	GAB1/IO03RSB0
B5	IO17RSB0
B6	IO21RSB0
B7	IO27RSB0
B8	IO34RSB0
B9	IO44RSB0
B10	IO51RSB0
B11	IO57RSB0
B12	GBC1/IO73RSB0
B13	GBB0/IO74RSB0
B14	IO71RSB0
B15	GBA2/IO78PDB1
B16	IO81PDB1
C1	IO224NDB3
C2	IO225NDB3
C3	VMV3
C4	IO11RSB0
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0
C7	IO25RSB0
C8	IO36RSB0
C9	IO42RSB0
C10	IO49RSB0
C11	IO56RSB0
C12	GBC0/IO72RSB0

FG256	
Pin Number	**A3P1000L Function**
C13	IO62RSB0
C14	VMV0
C15	IO78NDB1
C16	IO81NDB1
D1	IO222NDB3
D2	IO222PDB3
D3	GAC2/IO223PDB3
D4	IO223NDB3
D5	GNDQ
D6	IO23RSB0
D7	IO29RSB0
D8	IO33RSB0
D9	IO46RSB0
D10	IO52RSB0
D11	IO60RSB0
D12	GNDQ
D13	IO80NDB1
D14	GBB2/IO79PDB1
D15	IO79NDB1
D16	IO82NSB1
E1	IO217PDB3
E2	IO218PDB3
E3	IO221NDB3
E4	IO221PDB3
E5	VMV0
E6	VCCIB0
E7	VCCIB0
E8	IO38RSB0
E9	IO47RSB0
E10	VCCIB0
E11	VCCIB0
E12	VMV1
E13	GBC2/IO80PDB1
E14	IO83PPB1
E15	IO86PPB1
E16	IO87PDB1
F1	IO217NDB3
F2	IO218NDB3
F3	IO216PDB3
F4	IO216NDB3
F5	VCCIB3
F6	GND
F7	VCC
F8	VCC

FG256	
Pin Number	**A3P1000L Function**
F9	VCC
F10	VCC
F11	GND
F12	VCCIB1
F13	IO83NPB1
F14	IO86NPB1
F15	IO90PPB1
F16	IO87NDB1
G1	IO210PSB3
G2	IO213NDB3
G3	IO213PDB3
G4	GFC1/IO209PPB3
G5	VCCIB3
G6	VCC
G7	GND
G8	GND
G9	GND
G10	GND
G11	VCC
G12	VCCIB1
G13	GCC1/IO91PPB1
G14	IO90NPB1
G15	IO88PDB1
G16	IO88NDB1
H1	GFB0/IO208NPB3
H2	GFA0/IO207NDB3
H3	GFB1/IO208PPB3
H4	VCOMPLF
H5	GFC0/IO209NPB3
H6	VCC
H7	GND
H8	GND
H9	GND
H10	GND
H11	VCC
H12	GCC0/IO91NPB1
H13	GCB1/IO92PPB1
H14	GCA0/IO93NPB1
H15	IO96NPB1
H16	GCB0/IO92NPB1
J1	GFA2/IO206PSB3
J2	GFA1/IO207PDB3
J3	VCCPLF
J4	IO205NDB3

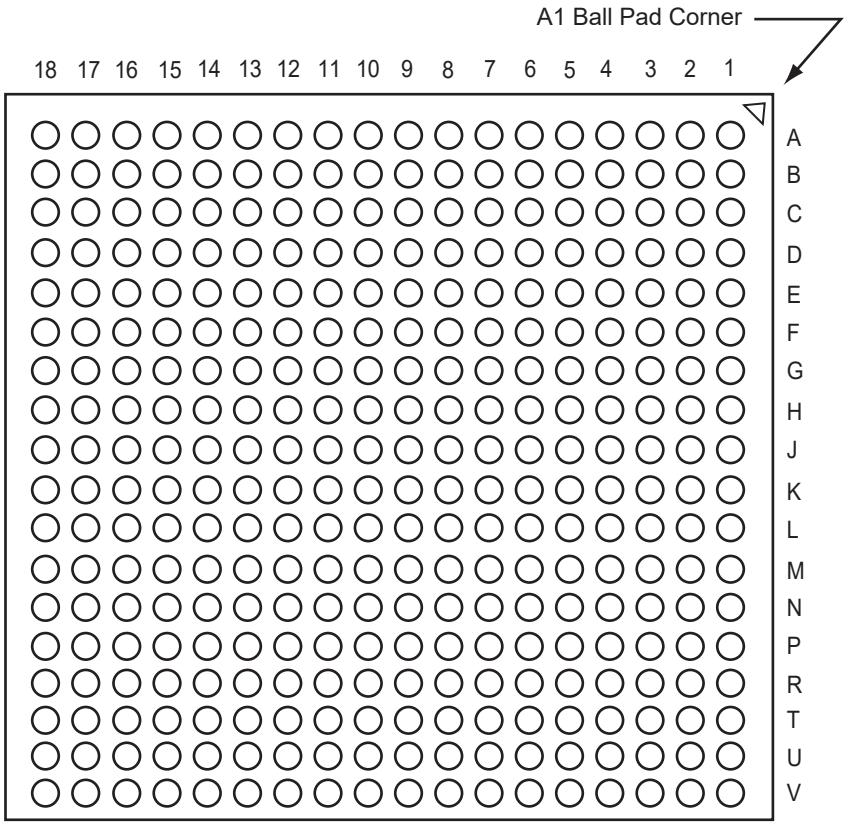
FG256	
Pin Number	**A3P1000L Function**
J5	GFB2/IO205PDB3
J6	VCC
J7	GND
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO95PPB1
J13	GCA1/IO93PPB1
J14	GCC2/IO96PPB1
J15	IO100PPB1
J16	GCA2/IO94PSB1
K1	GFC2/IO204PDB3
K2	IO204NDB3
K3	IO203NDB3
K4	IO203PDB3
K5	VCCIB3
K6	VCC
K7	GND
K8	GND
K9	GND
K10	GND
K11	VCC
K12	VCCIB1
K13	IO95NPB1
K14	IO100NPB1
K15	IO102NDB1
K16	IO102PDB1
L1	IO202NDB3
L2	IO202PDB3
L3	IO196PPB3
L4	IO193PPB3
L5	VCCIB3
L6	GND
L7	VCC
L8	VCC
L9	VCC
L10	VCC
L11	GND
L12	VCCIB1
L13	GDB0/IO112NPB1
L14	IO106NDB1
L15	IO106PDB1
L16	IO107PDB1

FG256	
Pin Number	**A3P1000L Function**
M1	IO197NSB3
M2	IO196NPB3
M3	IO193NPB3
M4	GEC0/IO190NPB3
M5	VMV3
M6	VCCIB2
M7	VCCIB2
M8	IO147RSB2
M9	IO136RSB2
M10	VCCIB2
M11	VCCIB2
M12	VMV2
M13	IO110NDB1
M14	GDB1/IO112PPB1
M15	GDC1/IO111PDB1
M16	IO107NDB1
N1	IO194PSB3
N2	IO192PPB3
N3	GEC1/IO190PPB3
N4	IO192NPB3
N5	GNDQ
N6	GEA2/IO187RSB2
N7	IO161RSB2
N8	IO155RSB2
N9	IO141RSB2
N10	IO129RSB2
N11	IO124RSB2
N12	GNDQ
N13	IO110PDB1
N14	VJTAG
N15	GDC0/IO111NDB1
N16	GDA1/IO113PDB1
P1	GEB1/IO189PDB3
P2	GEB0/IO189NDB3
P3	VMV2
P4	IO179RSB2
P5	IO171RSB2
P6	IO165RSB2
P7	IO159RSB2
P8	IO151RSB2
P9	IO137RSB2
P10	IO134RSB2
P11	IO128RSB2
P12	VMV1

FG256	
Pin Number	**A3P1000L Function**
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO113NDB1
R1	GEA1/IO188PDB3
R2	GEA0/IO188NDB3
R3	IO184RSB2
R4	GEC2/IO185RSB2
R5	IO168RSB2
R6	IO163RSB2
R7	IO157RSB2
R8	IO149RSB2
R9	IO143RSB2
R10	IO138RSB2
R11	IO131RSB2
R12	IO125RSB2
R13	GDB2/IO115RSB2
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO183RSB2
T3	FF/GEB2/ IO186RSB2
T4	IO172RSB2
T5	IO170RSB2
T6	IO164RSB2
T7	IO158RSB2
T8	IO153RSB2
T9	IO142RSB2
T10	IO135RSB2
T11	IO130RSB2
T12	GDC2/IO116RSB2
T13	IO120RSB2
T14	GDA2/IO114RSB2
T15	TMS
T16	GND

4.5 FG324 - Bottom View

Note: For Package Manufacturing and Environmental information, visit the Resource Center at *http://www.microsemi.com/soc/products/solutions/package/docs.aspx*.


A1 Ball Pad Corner
18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
A
B
C
D
E
F
G
H
J
K
L
M
N
P
R
T
U
V

FG324	
Pin Number	**A3PE3000L Function**
A1	GND
A2	IO08NDB0V0
A3	IO08PDB0V0
A4	IO10NDB0V1
A5	IO10PDB0V1
A6	IO12PDB0V1
A7	GND
A8	IO32NDB0V3
A9	IO32PDB0V3
A10	IO42PPB1V0
A11	IO52NPB1V1
A12	GND
A13	IO66NDB1V3
A14	IO72NDB1V3
A15	IO72PDB1V3
A16	IO74NDB1V4
A17	IO74PDB1V4
A18	GND
B1	IO305PDB7V3
B2	GAB2/IO308PDB7V4
B3	GAA0/IO00NPB0V0
B4	VCCIB0
B5	GNDQ
B6	IO12NDB0V1
B7	IO18NDB0V2
B8	VCCIB0
B9	IO42NPB1V0
B10	IO44NDB1V0
B11	VCCIB1
B12	IO52PPB1V1
B13	IO66PDB1V3
B14	GNDQ
B15	VCCIB1
B16	GBA0/IO81NDB1V4
B17	GBA1/IO81PDB1V4
B18	IO88PDB2V0
C1	IO305NDB7V3
C2	IO308NDB7V4
C3	GAA2/IO309PPB7V4
C4	GAA1/IO00PPB0V0
C5	VMV0
C6	IO14NDB0V1
C7	IO18PDB0V2

FG324	
Pin Number	**A3PE3000L Function**
C8	IO40NDB0V4
C9	IO40PDB0V4
C10	IO44PDB1V0
C11	IO56NDB1V1
C12	IO64NDB1V2
C13	IO64PDB1V2
C14	VMV1
C15	GBC0/IO79NDB1V4
C16	GBC1/IO79PDB1V4
C17	GBB2/IO83PPB2V0
C18	IO88NDB2V0
D1	IO303PDB7V3
D2	VCCIB7
D3	GAC2/IO307PPB7V4
D4	IO309NPB7V4
D5	GAB1/IO01PPB0V0
D6	IO14PDB0V1
D7	IO24NDB0V2
D8	IO24PDB0V2
D9	IO28PDB0V3
D10	IO48NDB1V0
D11	IO56PDB1V1
D12	IO60PPB1V2
D13	GBB0/IO80NDB1V4
D14	GBB1/IO80PDB1V4
D15	GBA2/IO82PDB2V0
D16	IO83NPB2V0
D17	VCCIB2
D18	IO90PDB2V1
E1	IO303NDB7V3
E2	GNDQ
E2	GNDQ
E3	VMV7
E3	VMV7
E4	IO307NPB7V4
E5	VCCPLA
E6	GAB0/IO01NPB0V0
E7	VCCIB0
E8	GND
E9	IO28NDB0V3
E10	IO48PDB1V0
E11	GND
E12	VCCIB1

FG324	
Pin Number	**A3PE3000L Function**
E13	IO60NPB1V2
E14	VCCPLB
E15	IO82NDB2V0
E16	VMV2
E16	VMV2
E17	GNDQ
E17	GNDQ
E18	IO90NDB2V1
F1	IO299NDB7V3
F2	IO299PDB7V3
F3	IO295PDB7V2
F4	IO295NDB7V2
F5	VCOMPLA
F6	IO291PPB7V2
F7	GAC0/IO02NDB0V0
F8	GAC1/IO02PDB0V0
F9	IO26PDB0V3
F10	IO34PDB0V4
F11	IO58NDB1V2
F12	IO58PDB1V2
F13	IO94PPB2V1
F14	VCOMPLB
F15	GBC2/IO84PDB2V0
F16	IO84NDB2V0
F17	IO92NDB2V1
F18	IO92PDB2V1
G1	GND
G2	IO287PDB7V1
G3	IO287NDB7V1
G4	IO283PPB7V1
G5	VCCIB7
G6	IO279PDB7V0
G7	IO291NPB7V2
G8	VCC
G9	IO26NDB0V3
G10	IO34NDB0V4
G11	VCC
G12	IO94NPB2V1
G13	IO98PDB2V2
G14	VCCIB2
G15	GCC0/IO112NPB2V3
G16	IO104PDB2V2
G17	IO104NDB2V2

FG324	
Pin Number	**A3PE3000L Function**
G18	GND
H1	IO267PDB6V4
H2	VCCIB7
H3	IO283NPB7V1
H4	GFB1/IO274PPB7V0
H5	GND
H6	IO279NDB7V0
H7	VCC
H8	VCC
H9	GND
H10	GND
H11	VCC
H12	VCC
H13	IO98NDB2V2
H14	GND
H15	GCB1/IO113PDB2V3
H16	GCC1/IO112PPB2V3
H17	VCCIB2
H18	IO108PDB2V3
J1	IO267NDB6V4
J2	GFA0/IO273NDB6V4
J3	VCOMPLF
J4	GFA2/IO272PDB6V4
J5	GFB0/IO274NPB7V0
J6	GFC0/IO275NDB7V0
J7	GFC1/IO275PDB7V0
J8	GND
J9	GND
J10	GND
J11	GND
J12	GCA2/IO115PDB3V0
J13	GCA1/IO114PDB3V0
J14	GCA0/IO114NDB3V0
J15	GCB0/IO113NDB2V3
J16	VCOMPLC
J17	IO120NPB3V0
J18	IO108NDB2V3
K1	IO263PDB6V3
K2	GFA1/IO273PDB6V4
K3	VCCPLF
K4	IO272NDB6V4
K5	GFC2/IO270PPB6V4
K6	GFB2/IO271PDB6V4

FG324	
Pin Number	**A3PE3000L Function**
K7	IO271NDB6V4
K8	GND
K9	GND
K10	GND
K11	GND
K12	IO115NDB3V0
K13	GCB2/IO116PDB3V0
K14	IO116NDB3V0
K15	GCC2/IO117PDB3V0
K16	VCCPLC
K17	IO124NPB3V1
K18	IO120PPB3V0
L1	IO263NDB6V3
L2	VCCIB6
L3	IO259PDB6V3
L4	IO259NDB6V3
L5	GND
L6	IO270NPB6V4
L7	VCC
L8	VCC
L9	GND
L10	GND
L11	VCC
L12	VCC
L13	IO132PDB3V2
L14	GND
L15	IO117NDB3V0
L16	IO128NPB3V1
L17	VCCIB3
L18	IO124PPB3V1
M1	GND
M2	IO255PDB6V2
M3	IO255NDB6V2
M4	IO251PPB6V2
M5	VCCIB6
M6	GEB0/IO235NDB6V0
M7	GEB1/IO235PDB6V0
M8	VCC
M9	IO192PPB4V4
M10	IO154NPB4V0
M11	VCC
M12	GDA0/IO153NPB3V4
M13	IO132NDB3V2

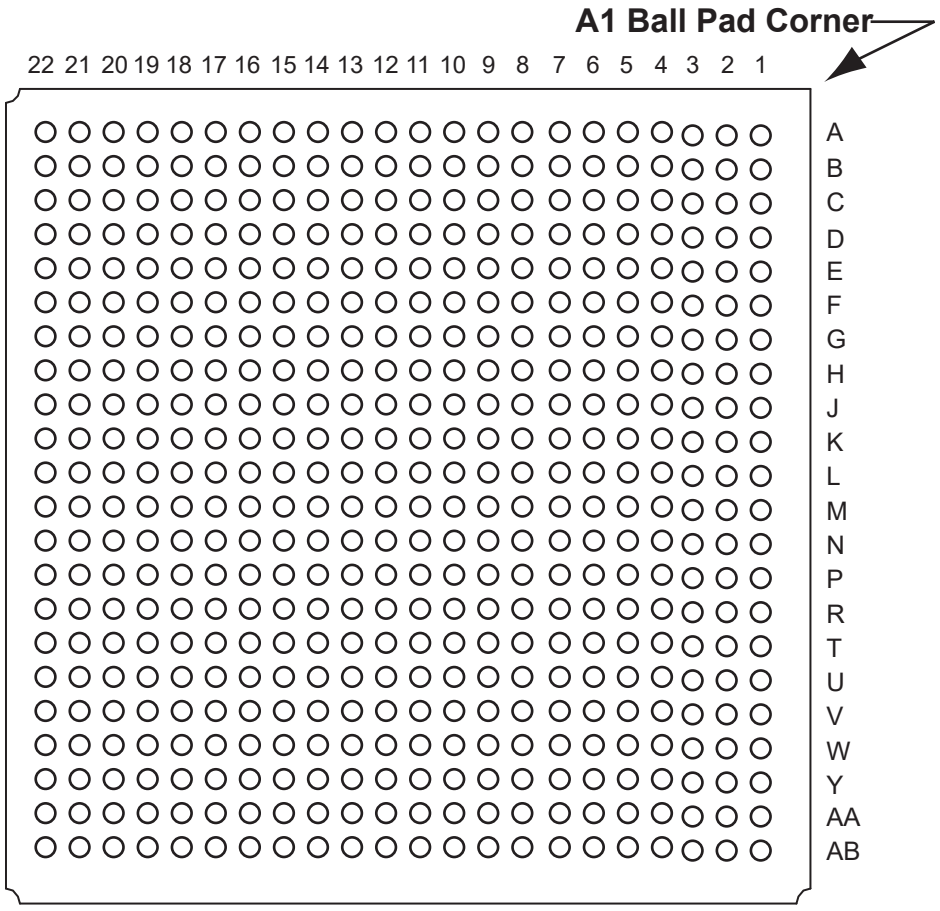
FG324	
Pin Number	**A3PE3000L Function**
M14	VCCIB3
M15	IO134NDB3V2
M16	IO134PDB3V2
M17	IO128PPB3V1
M18	GND
N1	IO247NDB6V1
N2	IO247PDB6V1
N3	IO251NPB6V2
N4	GEC0/IO236NDB6V0
N5	VCOMPLE
N6	IO212NDB5V2
N7	IO212PDB5V2
N8	IO192NPB4V4
N9	IO174PDB4V2
N10	IO170PDB4V2
N11	GDA2/IO154PPB4V0
N12	GDB2/IO155PPB4V0
N13	GDA1/IO153PPB3V4
N14	VCOMPLD
N15	GDB0/IO152NDB3V4
N16	GDB1/IO152PDB3V4
N17	IO138NDB3V3
N18	IO138PDB3V3
P1	IO245PDB6V1
P2	GNDQ
P2	GNDQ
P3	VMV6
P3	VMV6
P4	GEC1/IO236PDB6V0
P5	VCCPLE
P6	IO214PDB5V2
P7	VCCIB5
P8	GND
P9	IO174NDB4V2
P10	IO170NDB4V2
P11	GND
P12	VCCIB4
P13	IO155NPB4V0
P14	VCCPLD
P15	VJTAG
P16	GDC0/IO151NDB3V4
P17	GDC1/IO151PDB3V4
P18	IO142PDB3V3

FG324	
Pin Number	**A3PE3000L Function**
R1	IO245NDB6V1
R2	VCCIB6
R3	GEA1/IO234PPB6V0
R4	IO232NDB5V4
R5	FF/GEB2/IO232PDB5V4
R6	IO214NDB5V2
R7	IO202PDB5V1
R8	IO194PDB5V0
R9	IO186PDB4V4
R10	IO178PDB4V3
R11	IO168NSB4V1
R12	IO164PDB4V1
R13	GDC2/IO156PDB4V0
R14	TCK
R15	VPUMP
R16	TRST
R17	VCCIB3
R18	IO142NDB3V3
T1	IO241PDB6V0
T2	GEA0/IO234NPB6V0
T3	IO233NPB5V4
T4	IO231NPB5V4
T5	VMV5
T6	IO208NDB5V1
T7	IO202NDB5V1
T8	IO194NDB5V0
T9	IO186NDB4V4
T10	IO178NDB4V3
T11	IO166NPB4V1
T12	IO164NDB4V1
T13	IO156NDB4V0
T14	VMV4
T15	TDI
T16	GNDQ
T16	GNDQ
T17	TDO
T18	IO146PDB3V4
U1	IO241NDB6V0
U2	GEA2/IO233PPB5V4
U3	GEC2/IO231PPB5V4
U4	VCCIB5
U5	GNDQ
U6	IO208PDB5V1

FG324	
Pin Number	**A3PE3000L Function**
U7	IO198PPB5V0
U8	VCCIB5
U9	IO182NPB4V3
U10	IO180NPB4V3
U11	VCCIB4
U12	IO166PPB4V1
U13	IO162PDB4V1
U14	GNDQ
U15	VCCIB4
U16	TMS
U17	VMV3
U17	VMV3
U18	IO146NDB3V4
V1	GND
V2	IO218NDB5V3
V3	IO218PDB5V3
V4	IO206NDB5V1
V5	IO206PDB5V1
V6	IO198NPB5V0
V7	GND
V8	IO190NDB4V4
V9	IO190PDB4V4
V10	IO182PPB4V3
V11	IO180PPB4V3
V12	GND
V13	IO162NDB4V1
V14	IO160NDB4V0
V15	IO160PDB4V0
V16	IO158NDB4V0
V17	IO158PDB4V0
V18	GND

4.6 FG484 - Bottom View

Note: For Package Manufacturing and Environmental information, visit the Resource Center at *http://www.microsemi.com/soc/products/solutions/package/docs.aspx*.


A1 Ball Pad Corner
22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
A
B
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T
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V
W
Y
AA
AB

FG484	
Pin Number	**A3P600L Function**
A1	GND
A2	GND
A3	VCCIB0
A4	NC
A5	NC
A6	IO09RSB0
A7	IO15RSB0
A8	NC
A9	NC
A10	IO22RSB0
A11	IO23RSB0
A12	IO29RSB0
A13	IO35RSB0
A14	NC
A15	NC
A16	IO46RSB0
A17	IO48RSB0
A18	NC
A19	NC
A20	VCCIB0
A21	GND
A22	GND
AA1	GND
AA2	VCCIB3
AA3	NC
AA4	NC
AA5	NC
AA6	IO135RSB2
AA7	IO133RSB2
AA8	NC
AA9	NC
AA10	NC
AA11	NC
AA12	NC
AA13	NC
AA14	NC
AA15	NC
AA16	IO101RSB2
AA17	NC
AA18	NC
AA19	NC
AA20	NC
AA21	VCCIB1
AA22	GND

FG484	
Pin Number	**A3P600L Function**
AB1	GND
AB2	GND
AB3	VCCIB2
AB4	NC
AB5	NC
AB6	IO130RSB2
AB7	IO128RSB2
AB8	IO122RSB2
AB9	IO116RSB2
AB10	NC
AB11	NC
AB12	IO113RSB2
AB13	IO112RSB2
AB14	NC
AB15	NC
AB16	IO100RSB2
AB17	IO95RSB2
AB18	NC
AB19	NC
AB20	VCCIB2
AB21	GND
AB22	GND
B1	GND
B2	VCCIB3
B3	NC
B4	NC
B5	NC
B6	IO08RSB0
B7	IO12RSB0
B8	NC
B9	NC
B10	IO17RSB0
B11	NC
B12	NC
B13	IO36RSB0
B14	NC
B15	NC
B16	IO47RSB0
B17	IO49RSB0
B18	NC
B19	NC
B20	NC
B21	VCCIB1
B22	GND

FG484	
Pin Number	**A3P600L Function**
C1	VCCIB3
C2	NC
C3	NC
C4	NC
C5	GND
C6	NC
C7	NC
C8	VCC
C9	VCC
C10	NC
C11	NC
C12	NC
C13	NC
C14	VCC
C15	VCC
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC
C21	NC
C22	VCCIB1
D1	NC
D2	NC
D3	NC
D4	GND
D5	GAA0/IO00RSB0
D6	GAA1/IO01RSB0
D7	GAB0/IO02RSB0
D8	IO11RSB0
D9	IO16RSB0
D10	IO18RSB0
D11	IO28RSB0
D12	IO34RSB0
D13	IO37RSB0
D14	IO41RSB0
D15	IO43RSB0
D16	GBB1/IO57RSB0
D17	GBA0/IO58RSB0
D18	GBA1/IO59RSB0
D19	GND
D20	NC
D21	NC
D22	NC

FG484	
Pin Number	**A3P600L Function**
E1	NC
E2	NC
E3	GND
E4	GAB2/IO173PDB3
E5	GAA2/IO174PDB3
E6	GNDQ
E7	GAB1/IO03RSB0
E8	IO13RSB0
E9	IO14RSB0
E10	IO21RSB0
E11	IO27RSB0
E12	IO32RSB0
E13	IO38RSB0
E14	IO42RSB0
E15	GBC1/IO55RSB0
E16	GBB0/IO56RSB0
E17	IO52RSB0
E18	GBA2/IO60PDB1
E19	IO60NDB1
E20	GND
E21	NC
E22	NC
F1	NC
F2	NC
F3	NC
F4	IO173NDB3
F5	IO174NDB3
F6	VMV3
F7	IO07RSB0
F8	GAC0/IO04RSB0
F9	GAC1/IO05RSB0
F10	IO20RSB0
F11	IO24RSB0
F12	IO33RSB0
F13	IO39RSB0
F14	IO44RSB0
F15	GBC0/IO54RSB0
F16	IO51RSB0
F17	VMV0
F18	IO61NPB1
F19	IO63PDB1
F20	NC
F21	NC
F22	NC

FG484	
Pin Number	**A3P600L Function**
G1	IO170NDB3
G2	IO170PDB3
G3	NC
G4	IO171NDB3
G5	IO171PDB3
G6	GAC2/IO172PDB3
G7	IO06RSB0
G8	GNDQ
G9	IO10RSB0
G10	IO19RSB0
G11	IO26RSB0
G12	IO30RSB0
G13	IO40RSB0
G14	IO45RSB0
G15	GNDQ
G16	IO50RSB0
G17	GBB2/IO61PPB1
G18	IO53RSB0
G19	IO63NDB1
G20	NC
G21	NC
G22	NC
H1	NC
H2	NC
H3	VCC
H4	IO166PDB3
H5	IO167NPB3
H6	IO172NDB3
H7	IO169NDB3
H8	VMV0
H9	VCCIB0
H10	VCCIB0
H11	IO25RSB0
H12	IO31RSB0
H13	VCCIB0
H14	VCCIB0
H15	VMV1
H16	GBC2/IO62PDB1
H17	IO67PPB1
H18	IO64PPB1
H19	IO66PDB1
H20	VCC
H21	NC
H22	NC

FG484	
Pin Number	**A3P600L Function**
J1	NC
J2	NC
J3	NC
J4	IO166NDB3
J5	IO168NPB3
J6	IO167PPB3
J7	IO169PDB3
J8	VCCIB3
J9	GND
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	GND
J15	VCCIB1
J16	IO62NDB1
J17	IO64NPB1
J18	IO65PPB1
J19	IO66NDB1
J20	NC
J21	IO68PDB1
J22	IO68NDB1
K1	IO157PDB3
K2	IO157NDB3
K3	NC
K4	IO165NDB3
K5	IO165PDB3
K6	IO168PPB3
K7	GFC1/IO164PPB3
K8	VCCIB3
K9	VCC
K10	GND
K11	GND
K12	GND
K13	GND
K14	VCC
K15	VCCIB1
K16	GCC1/IO69PPB1
K17	IO65NPB1
K18	IO75PDB1
K19	IO75NDB1
K20	NC
K21	IO76NDB1
K22	IO76PDB1

FG484	
Pin Number	**A3P600L Function**
L1	NC
L2	IO155PDB3
L3	NC
L4	GFB0/IO163NPB3
L5	GFA0/IO162NDB3
L6	GFB1/IO163PPB3
L7	VCOMPLF
L8	GFC0/IO164NPB3
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	VCC
L15	GCC0/IO69NPB1
L16	GCB1/IO70PPB1
L17	GCA0/IO71NPB1
L18	IO67NPB1
L19	GCB0/IO70NPB1
L20	IO77PDB1
L21	IO77NDB1
L22	IO78NPB1
M1	NC
M2	IO155NDB3
M3	IO158NPB3
M4	GFA2/IO161PPB3
M5	GFA1/IO162PDB3
M6	VCCPLF
M7	IO160NDB3
M8	GFB2/IO160PDB3
M9	VCC
M10	GND
M11	GND
M12	GND
M13	GND
M14	VCC
M15	GCB2/IO73PPB1
M16	GCA1/IO71PPB1
M17	GCC2/IO74PPB1
M18	IO80PPB1
M19	GCA2/IO72PDB1
M20	IO79PPB1
M21	IO78PPB1
M22	NC

FG484	
Pin Number	**A3P600L Function**
N1	IO154NDB3
N2	IO154PDB3
N3	NC
N4	GFC2/IO159PDB3
N5	IO161NPB3
N6	IO156PPB3
N7	IO129RSB2
N8	VCCIB3
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB1
N16	IO73NPB1
N17	IO80NPB1
N18	IO74NPB1
N19	IO72NDB1
N20	NC
N21	IO79NPB1
N22	NC
P1	NC
P2	IO153PDB3
P3	IO153NDB3
P4	IO159NDB3
P5	IO156NPB3
P6	IO151PPB3
P7	IO158PPB3
P8	VCCIB3
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB1
P16	GDB0/IO87NPB1
P17	IO85NDB1
P18	IO85PDB1
P19	IO84PDB1
P20	NC
P21	IO81PDB1
P22	NC

FG484	
Pin Number	**A3P600L Function**
R1	NC
R2	NC
R3	VCC
R4	IO150PDB3
R5	IO151NPB3
R6	IO147NPB3
R7	GEC0/IO146NPB3
R8	VMV3
R9	VCCIB2
R10	VCCIB2
R11	IO117RSB2
R12	IO110RSB2
R13	VCCIB2
R14	VCCIB2
R15	VMV2
R16	IO94RSB2
R17	GDB1/IO87PPB1
R18	GDC1/IO86PDB1
R19	IO84NDB1
R20	VCC
R21	IO81NDB1
R22	IO82PDB1
T1	IO152PDB3
T2	IO152NDB3
T3	NC
T4	IO150NDB3
T5	IO147PPB3
T6	GEC1/IO146PPB3
T7	IO140RSB2
T8	GNDQ
T9	GEA2/IO143RSB2
T10	IO126RSB2
T11	IO120RSB2
T12	IO108RSB2
T13	IO103RSB2
T14	IO99RSB2
T15	GNDQ
T16	IO92RSB2
T17	VJTAG
T18	GDC0/IO86NDB1
T19	GDA1/IO88PDB1
T20	NC
T21	IO83PDB1
T22	IO82NDB1

FG484	
Pin Number	**A3P600L Function**
U1	IO149PDB3
U2	IO149NDB3
U3	NC
U4	GEB1/IO145PDB3
U5	GEB0/IO145NDB3
U6	VMV2
U7	IO138RSB2
U8	IO136RSB2
U9	IO131RSB2
U10	IO124RSB2
U11	IO119RSB2
U12	IO107RSB2
U13	IO104RSB2
U14	IO97RSB2
U15	VMV1
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO88NDB1
U20	NC
U21	IO83NDB1
U22	NC
V1	NC
V2	NC
V3	GND
V4	GEA1/IO144PDB3
V5	GEA0/IO144NDB3
V6	IO139RSB2
V7	GEC2/IO141RSB2
V8	IO132RSB2
V9	IO127RSB2
V10	IO121RSB2
V11	IO114RSB2
V12	IO109RSB2
V13	IO105RSB2
V14	IO98RSB2
V15	IO96RSB2
V16	GDB2/IO90RSB2
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	NC

FG484	
Pin Number	**A3P600L Function**
W1	NC
W2	IO148PDB3
W3	NC
W4	GND
W5	IO137RSB2
W6	FF/GEB2/IO142RSB2
W7	IO134RSB2
W8	IO125RSB2
W9	IO123RSB2
W10	IO118RSB2
W11	IO115RSB2
W12	IO111RSB2
W13	IO106RSB2
W14	IO102RSB2
W15	GDC2/IO91RSB2
W16	IO93RSB2
W17	GDA2/IO89RSB2
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	VCCIB3
Y2	IO148NDB3
Y3	NC
Y4	NC
Y5	GND
Y6	NC
Y7	NC
Y8	VCC
Y9	VCC
Y10	NC
Y11	NC
Y12	NC
Y13	NC
Y14	VCC
Y15	VCC
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	VCCIB1

FG484	
Pin Number	**A3PE3000L Function**
A1	GND
A2	GND
A3	VCCIB0
A4	IO10NDB0V1
A5	IO10PDB0V1
A6	IO16NDB0V1
A7	IO16PDB0V1
A8	IO18PDB0V2
A9	IO24PDB0V2
A10	IO28NDB0V3
A11	IO28PDB0V3
A12	IO46PDB1V0
A13	IO54PDB1V1
A14	IO56NDB1V1
A15	IO56PDB1V1
A16	IO64NDB1V2
A17	IO64PDB1V2
A18	IO72NDB1V3
A19	IO74NDB1V4
A20	VCCIB1
A21	GND
A22	GND
AA1	GND
AA2	VCCIB6
AA3	IO228PDB5V4
AA4	IO224PDB5V3
AA5	IO218NDB5V3
AA6	IO218PDB5V3
AA7	IO212NDB5V2
AA8	IO212PDB5V2
AA9	IO198PDB5V0
AA10	IO198NDB5V0
AA11	IO188PPB4V4
AA12	IO180NDB4V3
AA13	IO180PDB4V3
AA14	IO170NDB4V2
AA15	IO170PDB4V2
AA16	IO166NDB4V1
AA17	IO166PDB4V1
AA18	IO160NDB4V0
AA19	IO160PDB4V0
AA20	IO158NPB4V0
AA21	VCCIB3

FG484	
Pin Number	**A3PE3000L Function**
AA22	GND
AB1	GND
AB2	GND
AB3	VCCIB5
AB4	IO216NDB5V2
AB5	IO216PDB5V2
AB6	IO210NDB5V2
AB7	IO210PDB5V2
AB8	IO208NDB5V1
AB9	IO208PDB5V1
AB10	IO197NDB5V0
AB11	IO197PDB5V0
AB12	IO174NDB4V2
AB13	IO174PDB4V2
AB14	IO172NDB4V2
AB15	IO172PDB4V2
AB16	IO168NDB4V1
AB17	IO168PDB4V1
AB18	IO162NDB4V1
AB19	IO162PDB4V1
AB20	VCCIB4
AB21	GND
AB22	GND
B1	GND
B2	VCCIB7
B3	IO06PPB0V0
B4	IO08NDB0V0
B5	IO08PDB0V0
B6	IO14NDB0V1
B7	IO14PDB0V1
B8	IO18NDB0V2
B9	IO24NDB0V2
B10	IO34PDB0V4
B11	IO40PDB0V4
B12	IO46NDB1V0
B13	IO54NDB1V1
B14	IO62NDB1V2
B15	IO62PDB1V2
B16	IO68NDB1V3
B17	IO68PDB1V3
B18	IO72PDB1V3
B19	IO74PDB1V4
B20	IO76NPB1V4

FG484	
Pin Number	**A3PE3000L Function**
B21	VCCIB2
B22	GND
C1	VCCIB7
C2	IO303PDB7V3
C3	IO305PDB7V3
C4	IO06NPB0V0
C5	GND
C6	IO12NDB0V1
C7	IO12PDB0V1
C8	VCC
C9	VCC
C10	IO34NDB0V4
C11	IO40NDB0V4
C12	IO48NDB1V0
C13	IO48PDB1V0
C14	VCC
C15	VCC
C16	IO70NDB1V3
C17	IO70PDB1V3
C18	GND
C19	IO76PPB1V4
C20	IO88NDB2V0
C21	IO94PPB2V1
C22	VCCIB2
D1	IO293PDB7V2
D2	IO303NDB7V3
D3	IO305NDB7V3
D4	GND
D5	GAA0/IO00NDB0V0
D6	GAA1/IO00PDB0V0
D7	GAB0/IO01NDB0V0
D8	IO20PDB0V2
D9	IO22PDB0V2
D10	IO30PDB0V3
D11	IO38NDB0V4
D12	IO52NDB1V1
D13	IO52PDB1V1
D14	IO66NDB1V3
D15	IO66PDB1V3
D16	GBB1/IO80PDB1V4
D17	GBA0/IO81NDB1V4
D18	GBA1/IO81PDB1V4
D19	GND

FG484	
Pin Number	**A3PE3000L Function**
D20	IO88PDB2V0
D21	IO90PDB2V1
D22	IO94NPB2V1
E1	IO293NDB7V2
E2	IO299PPB7V3
E3	GND
E4	GAB2/IO308PDB7V4
E5	GAA2/IO309PDB7V4
E6	GNDQ
E7	GAB1/IO01PDB0V0
E8	IO20NDB0V2
E9	IO22NDB0V2
E10	IO30NDB0V3
E11	IO38PDB0V4
E12	IO44NDB1V0
E13	IO58NDB1V2
E14	IO58PDB1V2
E15	GBC1/IO79PDB1V4
E16	GBB0/IO80NDB1V4
E17	GNDQ
E18	GBA2/IO82PDB2V0
E19	IO86NDB2V0
E20	GND
E21	IO90NDB2V1
E22	IO98PDB2V2
F1	IO299NPB7V3
F2	IO301NDB7V3
F3	IO301PDB7V3
F4	IO308NDB7V4
F5	IO309NDB7V4
F6	VMV7
F7	VCCPLA
F8	GAC0/IO02NDB0V0
F9	GAC1/IO02PDB0V0
F10	IO32NDB0V3
F11	IO32PDB0V3
F12	IO44PDB1V0
F13	IO50NDB1V1
F14	IO60PDB1V2
F15	GBC0/IO79NDB1V4
F16	VCCPLB
F17	VMV2
F18	IO82NDB2V0

FG484	
Pin Number	**A3PE3000L Function**
F19	IO86PDB2V0
F20	IO96PDB2V1
F21	IO96NDB2V1
F22	IO98NDB2V2
G1	IO289NDB7V1
G2	IO289PDB7V1
G3	IO291PPB7V2
G4	IO295PDB7V2
G5	IO297PDB7V2
G6	GAC2/IO307PDB7V4
G7	VCOMPLA
G8	GNDQ
G9	IO26NDB0V3
G10	IO26PDB0V3
G11	IO36PDB0V4
G12	IO42PDB1V0
G13	IO50PDB1V1
G14	IO60NDB1V2
G15	GNDQ
G16	VCOMPLB
G17	GBB2/IO83PDB2V0
G18	IO92PDB2V1
G19	IO92NDB2V1
G20	IO102PDB2V2
G21	IO102NDB2V2
G22	IO105NDB2V2
H1	IO286PSB7V1
H2	IO291NPB7V2
H3	VCC
H4	IO295NDB7V2
H5	IO297NDB7V2
H6	IO307NDB7V4
H7	IO287PDB7V1
H8	VMV0
H9	VCCIB0
H10	VCCIB0
H11	IO36NDB0V4
H12	IO42NDB1V0
H13	VCCIB1
H14	VCCIB1
H15	VMV1
H16	GBC2/IO84PDB2V0
H17	IO83NDB2V0

FG484	
Pin Number	**A3PE3000L Function**
H18	IO100NDB2V2
H19	IO100PDB2V2
H20	VCC
H21	VMV2
H22	IO105PDB2V2
J1	IO285NDB7V1
J2	IO285PDB7V1
J3	VMV7
J4	IO279PDB7V0
J5	IO283PDB7V1
J6	IO281PDB7V0
J7	IO287NDB7V1
J8	VCCIB7
J9	GND
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	GND
J15	VCCIB2
J16	IO84NDB2V0
J17	IO104NDB2V2
J18	IO104PDB2V2
J19	IO106PPB2V3
J20	GNDQ
J21	IO109PDB2V3
J22	IO107PDB2V3
K1	IO277NDB7V0
K2	IO277PDB7V0
K3	GNDQ
K4	IO279NDB7V0
K5	IO283NDB7V1
K6	IO281NDB7V0
K7	GFC1/IO275PPB7V0
K8	VCCIB7
K9	VCC
K10	GND
K11	GND
K12	GND
K13	GND
K14	VCC
K15	VCCIB2
K16	GCC1/IO112PPB2V3

FG484	
Pin Number	**A3PE3000L Function**
K17	IO108NDB2V3
K18	IO108PDB2V3
K19	IO110NPB2V3
K20	IO106NPB2V3
K21	IO109NDB2V3
K22	IO107NDB2V3
L1	IO257PSB6V2
L2	IO276PDB7V0
L3	IO276NDB7V0
L4	GFB0/IO274NPB7V0
L5	GFA0/IO273NDB6V4
L6	GFB1/IO274PPB7V0
L7	VCOMPLF
L8	GFC0/IO275NPB7V0
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	VCC
L15	GCC0/IO112NPB2V3
L16	GCB1/IO113PPB2V3
L17	GCA0/IO114NPB3V0
L18	VCOMPLC
L19	GCB0/IO113NPB2V3
L20	IO110PPB2V3
L21	IO111NDB2V3
L22	IO111PDB2V3
M1	GNDQ
M2	IO255NPB6V2
M3	IO272NDB6V4
M4	GFA2/IO272PDB6V4
M5	GFA1/IO273PDB6V4
M6	VCCPLF
M7	IO271NDB6V4
M8	GFB2/IO271PDB6V4
M9	VCC
M10	GND
M11	GND
M12	GND
M13	GND
M14	VCC
M15	GCB2/IO116PPB3V0

FG484	
Pin Number	**A3PE3000L Function**
M16	GCA1/IO114PPB3V0
M17	GCC2/IO117PPB3V0
M18	VCCPLC
M19	GCA2/IO115PDB3V0
M20	IO115NDB3V0
M21	IO126PDB3V1
M22	IO124PSB3V1
N1	IO255PPB6V2
N2	IO253NDB6V2
N3	VMV6
N4	GFC2/IO270PPB6V4
N5	IO261PPB6V3
N6	IO263PDB6V3
N7	IO263NDB6V3
N8	VCCIB6
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB3
N16	IO116NPB3V0
N17	IO132NPB3V2
N18	IO117NPB3V0
N19	IO132PPB3V2
N20	GNDQ
N21	IO126NDB3V1
N22	IO128PDB3V1
P1	IO247PDB6V1
P2	IO253PDB6V2
P3	IO270NPB6V4
P4	IO261NPB6V3
P5	IO249PPB6V1
P6	IO259PDB6V3
P7	IO259NDB6V3
P8	VCCIB6
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND

FG484	
Pin Number	**A3PE3000L Function**
P15	VCCIB3
P16	GDB0/IO152NPB3V4
P17	IO136NDB3V2
P18	IO136PDB3V2
P19	IO138PDB3V3
P20	VMV3
P21	IO130PDB3V2
P22	IO128NDB3V1
R1	IO247NDB6V1
R2	IO245PDB6V1
R3	VCC
R4	IO249NPB6V1
R5	IO251NDB6V2
R6	IO251PDB6V2
R7	GEC0/IO236NPB6V0
R8	VMV5
R9	VCCIB5
R10	VCCIB5
R11	IO196NDB5V0
R12	IO196PDB5V0
R13	VCCIB4
R14	VCCIB4
R15	VMV3
R16	VCCPLD
R17	GDB1/IO152PPB3V4
R18	GDC1/IO151PDB3V4
R19	IO138NDB3V3
R20	VCC
R21	IO130NDB3V2
R22	IO134PDB3V2
T1	IO243PPB6V1
T2	IO245NDB6V1
T3	IO243NPB6V1
T4	IO241PDB6V0
T5	IO241NDB6V0
T6	GEC1/IO236PPB6V0
T7	VCOMPLE
T8	GNDQ
T9	GEA2/IO233PPB5V4
T10	IO206NDB5V1
T11	IO202NDB5V1
T12	IO194NDB5V0
T13	IO186NDB4V4

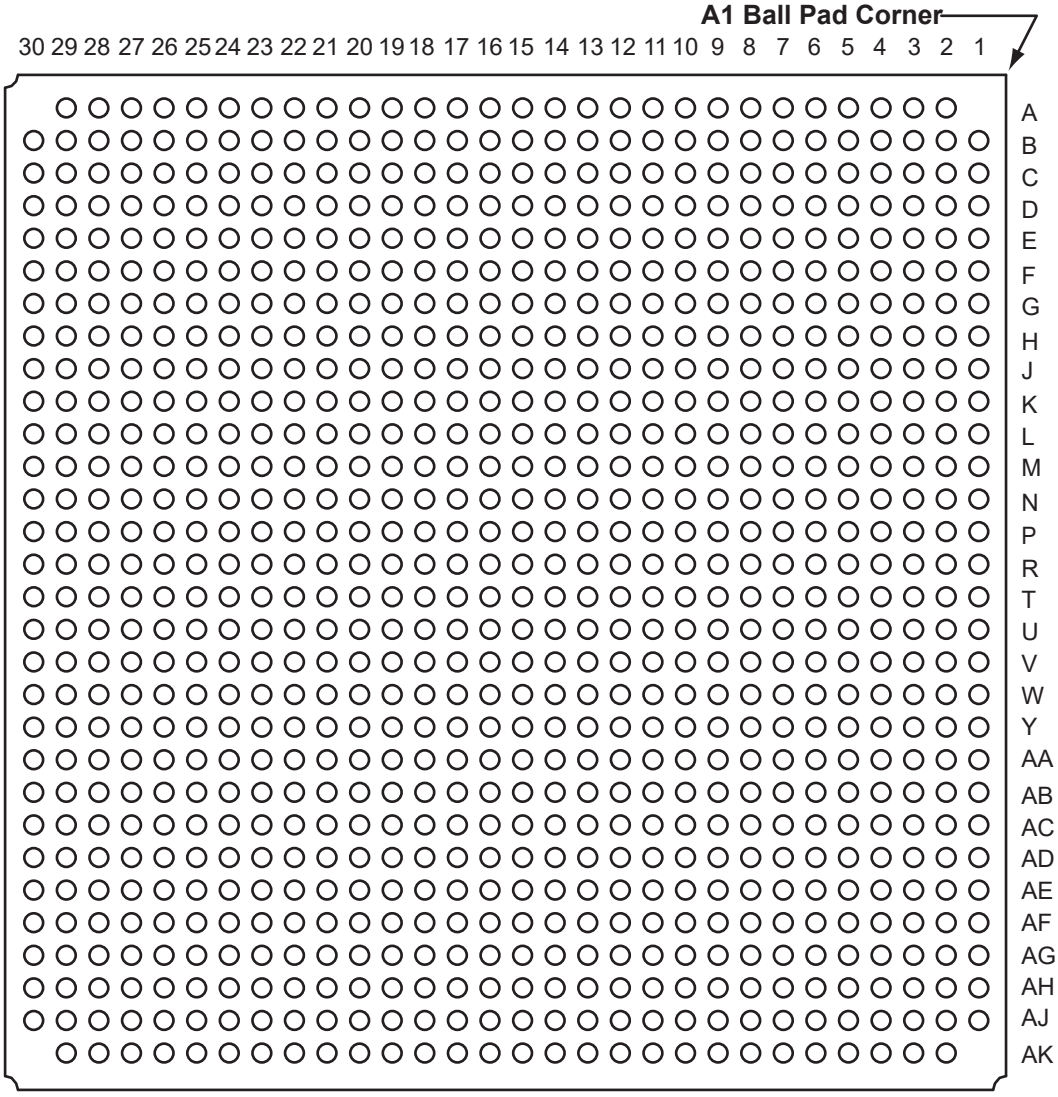
FG484	
Pin Number	**A3PE3000L Function**
T14	IO186PDB4V4
T15	GNDQ
T16	VCOMPLD
T17	VJTAG
T18	GDC0/IO151NDB3V4
T19	GDA1/IO153PDB3V4
T20	IO144PDB3V3
T21	IO140PDB3V3
T22	IO134NDB3V2
U1	IO240PPB6V0
U2	IO238PDB6V0
U3	IO238NDB6V0
U4	GEB1/IO235PDB6V0
U5	GEB0/IO235NDB6V0
U6	VMV6
U7	VCCPLE
U8	IO233NPB5V4
U9	IO222PPB5V3
U10	IO206PDB5V1
U11	IO202PDB5V1
U12	IO194PDB5V0
U13	IO176NDB4V2
U14	IO176PDB4V2
U15	VMV4
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO153NDB3V4
U20	IO144NDB3V3
U21	IO140NDB3V3
U22	IO142PDB3V3
V1	IO239PDB6V0
V2	IO240NPB6V0
V3	GND
V4	GEA1/IO234PDB6V0
V5	GEA0/IO234NDB6V0
V6	GNDQ
V7	GEC2/IO231PDB5V4
V8	IO222NPB5V3
V9	IO204NDB5V1
V10	IO204PDB5V1
V11	IO195NDB5V0
V12	IO195PDB5V0

FG484	
Pin Number	**A3PE3000L Function**
V13	IO178NDB4V3
V14	IO178PDB4V3
V15	IO155NDB4V0
V16	GDB2/IO155PDB4V0
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	IO146PDB3V4
V22	IO142NDB3V3
W1	IO239NDB6V0
W2	IO237PDB6V0
W3	IO230PSB5V4
W4	GND
W5	IO232NDB5V4
W6	FF/GEB2/ IO232PDB5V4
W7	IO231NDB5V4
W8	IO214NDB5V2
W9	IO214PDB5V2
W10	IO200NDB5V0
W11	IO192NDB4V4
W12	IO184NDB4V3
W13	IO184PDB4V3
W14	IO156NDB4V0
W15	GDC2/IO156PDB4V0
W16	IO154NDB4V0
W17	GDA2/IO154PDB4V0
W18	TMS
W19	GND
W20	IO150NDB3V4
W21	IO146NDB3V4
W22	IO148PPB3V4
Y1	VCCIB6
Y2	IO237NDB6V0
Y3	IO228NDB5V4
Y4	IO224NDB5V3
Y5	GND
Y6	IO220NDB5V3
Y7	IO220PDB5V3
Y8	VCC
Y9	VCC
Y10	IO200PDB5V0

FG484	
Pin Number	**A3PE3000L Function**
Y11	IO192PDB4V4
Y12	IO188NPB4V4
Y13	IO187PSB4V4
Y14	VCC
Y15	VCC
Y16	IO164NDB4V1
Y17	IO164PDB4V1
Y18	GND
Y19	IO158PPB4V0
Y20	IO150PDB3V4
Y21	IO148NPB3V4
Y22	VCCIB3

4.7 FG896

Note: For Package Manufacturing and Environmental information, visit the Resource Center at *http://www.microsemi.com/soc/products/solutions/package/docs.aspx*.


A1 Ball Pad Corner
30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
A
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G
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AA
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FG896	
Pin Number	**A3PE3000L Function**
A2	GND
A3	GND
A4	IO14NPB0V1
A5	GND
A6	IO07NPB0V0
A7	GND
A8	IO09NDB0V1
A9	IO17NDB0V2
A10	IO17PDB0V2
A11	IO21NDB0V2
A12	IO21PDB0V2
A13	IO33NDB0V4
A14	IO33PDB0V4
A15	IO35NDB0V4
A16	IO35PDB0V4
A17	IO41NDB1V0
A18	IO43NDB1V0
A19	IO43PDB1V0
A20	IO45NDB1V0
A21	IO45PDB1V0
A22	IO57NDB1V2
A23	IO57PDB1V2
A24	GND
A25	IO69PPB1V3
A26	GND
A27	GBC1/IO79PPB1V4
A28	GND
A29	GND
AA1	IO256PDB6V2
AA2	IO248PDB6V1
AA3	IO248NDB6V1
AA4	IO246NDB6V1
AA5	GEA1/IO234PDB6V0
AA6	GEA0/IO234NDB6V0
AA7	IO243PPB6V1
AA8	IO245NDB6V1
AA9	GEB1/IO235PPB6V0
AA10	VCC
AA11	IO226PPB5V4
AA12	VCCIB5
AA13	VCCIB5
AA14	VCCIB5
AA15	VCCIB5

FG896	
Pin Number	**A3PE3000L Function**
AA16	VCCIB4
AA17	VCCIB4
AA18	VCCIB4
AA19	VCCIB4
AA20	IO174PDB4V2
AA21	VCC
AA22	IO142NPB3V3
AA23	IO144NDB3V3
AA24	IO144PDB3V3
AA25	IO146NDB3V4
AA26	IO146PDB3V4
AA27	IO147PDB3V4
AA28	IO139NDB3V3
AA29	IO139PDB3V3
AA30	IO133NDB3V2
AB1	IO256NDB6V2
AB2	IO244PDB6V1
AB3	IO244NDB6V1
AB4	IO241PDB6V0
AB5	IO241NDB6V0
AB6	IO243NPB6V1
AB7	VCCIB6
AB8	VCCPLE
AB9	VCC
AB10	IO222PDB5V3
AB11	IO218PPB5V3
AB12	IO206NDB5V1
AB13	IO206PDB5V1
AB14	IO198NDB5V0
AB15	IO198PDB5V0
AB16	IO192NDB4V4
AB17	IO192PDB4V4
AB18	IO178NDB4V3
AB19	IO178PDB4V3
AB20	IO174NDB4V2
AB21	IO162NPB4V1
AB22	VCC
AB23	VCCPLD
AB24	VCCIB3
AB25	IO150PDB3V4
AB26	IO148PDB3V4
AB27	IO147NDB3V4
AB28	IO145PDB3V3

FG896	
Pin Number	**A3PE3000L Function**
AB29	IO143PDB3V3
AB30	IO137PDB3V2
AC1	IO254PDB6V2
AC2	IO254NDB6V2
AC3	IO240PDB6V0
AC4	GEC1/IO236PDB6V0
AC5	IO237PDB6V0
AC6	IO237NDB6V0
AC7	VCOMPLE
AC8	GND
AC9	IO226NPB5V4
AC10	IO222NDB5V3
AC11	IO216NPB5V2
AC12	IO210NPB5V2
AC13	IO204NDB5V1
AC14	IO204PDB5V1
AC15	IO194NDB5V0
AC16	IO188NDB4V4
AC17	IO188PDB4V4
AC18	IO182PPB4V3
AC19	IO170NPB4V2
AC20	IO164NDB4V1
AC21	IO164PDB4V1
AC22	IO162PPB4V1
AC23	GND
AC24	VCOMPLD
AC25	IO150NDB3V4
AC26	IO148NDB3V4
AC27	GDA1/IO153PDB3V4
AC28	IO145NDB3V3
AC29	IO143NDB3V3
AC30	IO137NDB3V2
AD1	GND
AD2	IO242NPB6V1
AD3	IO240NDB6V0
AD4	GEC0/IO236NDB6V0
AD5	VCCIB6
AD6	GNDQ
AD7	VCC
AD8	VMV5
AD9	VCCIB5
AD10	IO224PPB5V3
AD11	IO218NPB5V3

FG896	
Pin Number	**A3PE3000L Function**
AD12	IO216PPB5V2
AD13	IO210PPB5V2
AD14	IO202PPB5V1
AD15	IO194PDB5V0
AD16	IO190PDB4V4
AD17	IO182NPB4V3
AD18	IO176NDB4V2
AD19	IO176PDB4V2
AD20	IO170PPB4V2
AD21	IO166PDB4V1
AD22	VCCIB4
AD23	TCK
AD24	VCC
AD25	TRST
AD26	VCCIB3
AD27	GDA0/IO153NDB3V4
AD28	GDC0/IO151NDB3V4
AD29	GDC1/IO151PDB3V4
AD30	GND
AE1	IO242PPB6V1
AE2	VCC
AE3	IO239PDB6V0
AE4	IO239NDB6V0
AE5	VMV6
AE5	VMV6
AE6	GND
AE7	GNDQ
AE8	IO230NDB5V4
AE9	IO224NPB5V3
AE10	IO214NPB5V2
AE11	IO212NDB5V2
AE12	IO212PDB5V2
AE13	IO202NPB5V1
AE14	IO200NDB5V0
AE15	IO196PDB5V0
AE16	IO190NDB4V4
AE17	IO184PDB4V3
AE18	IO184NDB4V3
AE19	IO172PDB4V2
AE20	IO172NDB4V2
AE21	IO166NDB4V1
AE22	IO160PDB4V0
AE23	GNDQ

FG896	
Pin Number	**A3PE3000L Function**
AE24	VMV4
AE25	GND
AE26	GDB0/IO152NDB3V4
AE27	GDB1/IO152PDB3V4
AE28	VMV3
AE28	VMV3
AE29	VCC
AE30	IO149PDB3V4
AF1	GND
AF2	IO238PPB6V0
AF3	VCCIB6
AF4	IO220NPB5V3
AF5	VCC
AF6	IO228NDB5V4
AF7	VCCIB5
AF8	IO230PDB5V4
AF9	IO229NDB5V4
AF10	IO229PDB5V4
AF11	IO214PPB5V2
AF12	IO208NDB5V1
AF13	IO208PDB5V1
AF14	IO200PDB5V0
AF15	IO196NDB5V0
AF16	IO186NDB4V4
AF17	IO186PDB4V4
AF18	IO180NDB4V3
AF19	IO180PDB4V3
AF20	IO168NDB4V1
AF21	IO168PDB4V1
AF22	IO160NDB4V0
AF23	IO158NPB4V0
AF24	VCCIB4
AF25	IO154NPB4V0
AF26	VCC
AF27	TDO
AF28	VCCIB3
AF29	GNDQ
AF30	GND
AG1	IO238NPB6V0
AG2	VCC
AG3	IO232NPB5V4
AG4	GND
AG5	IO220PPB5V3

FG896	
Pin Number	**A3PE3000L Function**
AG6	IO228PDB5V4
AG7	IO231NDB5V4
AG8	GEC2/IO231PDB5V4
AG9	IO225NPB5V3
AG10	IO223NPB5V3
AG11	IO221PDB5V3
AG12	IO221NDB5V3
AG13	IO205NPB5V1
AG14	IO199NDB5V0
AG15	IO199PDB5V0
AG16	IO187NDB4V4
AG17	IO187PDB4V4
AG18	IO181NDB4V3
AG19	IO171PPB4V2
AG20	IO165NPB4V1
AG21	IO161NPB4V0
AG22	IO159NDB4V0
AG23	IO159PDB4V0
AG24	IO158PPB4V0
AG25	GDB2/IO155PDB4V0
AG26	GDA2/IO154PPB4V0
AG27	GND
AG28	VJTAG
AG29	VCC
AG30	IO149NDB3V4
AH1	GND
AH2	IO233NPB5V4
AH3	VCC
AH4	FF/GEB2/IO232PPB5V4
AH5	VCCIB5
AH6	IO219NDB5V3
AH7	IO219PDB5V3
AH8	IO227NDB5V4
AH9	IO227PDB5V4
AH10	IO225PPB5V3
AH11	IO223PPB5V3
AH12	IO211NDB5V2
AH13	IO211PDB5V2
AH14	IO205PPB5V1
AH15	IO195NDB5V0
AH16	IO185NDB4V3
AH17	IO185PDB4V3
AH18	IO181PDB4V3

FG896	
Pin Number	**A3PE3000L Function**
AH19	IO177NDB4V2
AH20	IO171NPB4V2
AH21	IO165PPB4V1
AH22	IO161PPB4V0
AH23	IO157NDB4V0
AH24	IO157PDB4V0
AH25	IO155NDB4V0
AH26	VCCIB4
AH27	TDI
AH28	VCC
AH29	VPUMP
AH30	GND
AJ1	GND
AJ2	GND
AJ3	GEA2/IO233PPB5V4
AJ4	VCC
AJ5	IO217NPB5V2
AJ6	VCC
AJ7	IO215NPB5V2
AJ8	IO213NDB5V2
AJ9	IO213PDB5V2
AJ10	IO209NDB5V1
AJ11	IO209PDB5V1
AJ12	IO203NDB5V1
AJ13	IO203PDB5V1
AJ14	IO197NDB5V0
AJ15	IO195PDB5V0
AJ16	IO183NDB4V3
AJ17	IO183PDB4V3
AJ18	IO179NPB4V3
AJ19	IO177PDB4V2
AJ20	IO173NDB4V2
AJ21	IO173PDB4V2
AJ22	IO163NDB4V1
AJ23	IO163PDB4V1
AJ24	IO167NPB4V1
AJ25	VCC
AJ26	IO156NPB4V0
AJ27	VCC
AJ28	TMS
AJ29	GND
AJ30	GND
AK2	GND

FG896	
Pin Number	**A3PE3000L Function**
AK3	GND
AK4	IO217PPB5V2
AK5	GND
AK6	IO215PPB5V2
AK7	GND
AK8	IO207NDB5V1
AK9	IO207PDB5V1
AK10	IO201NDB5V0
AK11	IO201PDB5V0
AK12	IO193NDB4V4
AK13	IO193PDB4V4
AK14	IO197PDB5V0
AK15	IO191NDB4V4
AK16	IO191PDB4V4
AK17	IO189NDB4V4
AK18	IO189PDB4V4
AK19	IO179PPB4V3
AK20	IO175NDB4V2
AK21	IO175PDB4V2
AK22	IO169NDB4V1
AK23	IO169PDB4V1
AK24	GND
AK25	IO167PPB4V1
AK26	GND
AK27	GDC2/IO156PPB4V0
AK28	GND
AK29	GND
B1	GND
B2	GND
B3	GAA2/IO309PPB7V4
B4	VCC
B5	IO14PPB0V1
B6	VCC
B7	IO07PPB0V0
B8	IO09PDB0V1
B9	IO15PPB0V1
B10	IO19NDB0V2
B11	IO19PDB0V2
B12	IO29NDB0V3
B13	IO29PDB0V3
B14	IO31PPB0V3
B15	IO37NDB0V4
B16	IO37PDB0V4

FG896	
Pin Number	**A3PE3000L Function**
B17	IO41PDB1V0
B18	IO51NDB1V1
B19	IO59PDB1V2
B20	IO53PDB1V1
B21	IO53NDB1V1
B22	IO61NDB1V2
B23	IO61PDB1V2
B24	IO69NPB1V3
B25	VCC
B26	GBC0/IO79NPB1V4
B27	VCC
B28	IO64NPB1V2
B29	GND
B30	GND
C1	GND
C2	IO309NPB7V4
C3	VCC
C4	GAA0/IO00NPB0V0
C5	VCCIB0
C6	IO03PDB0V0
C7	IO03NDB0V0
C8	GAB1/IO01PDB0V0
C9	IO05PDB0V0
C10	IO15NPB0V1
C11	IO25NDB0V3
C12	IO25PDB0V3
C13	IO31NPB0V3
C14	IO27NDB0V3
C15	IO39NDB0V4
C16	IO39PDB0V4
C17	IO55PPB1V1
C18	IO51PDB1V1
C19	IO59NDB1V2
C20	IO63NDB1V2
C21	IO63PDB1V2
C22	IO67NDB1V3
C23	IO67PDB1V3
C24	IO75NDB1V4
C25	IO75PDB1V4
C26	VCCIB1
C27	IO64PPB1V2
C28	VCC
C29	GBA1/IO81PPB1V4

FG896	
Pin Number	**A3PE3000L Function**
C30	GND
D1	IO303PPB7V3
D2	VCC
D3	IO305NPB7V3
D4	GND
D5	GAA1/IO00PPB0V0
D6	GAC1/IO02PDB0V0
D7	IO06NPB0V0
D8	GAB0/IO01NDB0V0
D9	IO05NDB0V0
D10	IO11NDB0V1
D11	IO11PDB0V1
D12	IO23NDB0V2
D13	IO23PDB0V2
D14	IO27PDB0V3
D15	IO40PDB0V4
D16	IO47NDB1V0
D17	IO47PDB1V0
D18	IO55NPB1V1
D19	IO65NDB1V3
D20	IO65PDB1V3
D21	IO71NDB1V3
D22	IO71PDB1V3
D23	IO73NDB1V4
D24	IO73PDB1V4
D25	IO74NDB1V4
D26	GBB0/IO80NPB1V4
D27	GND
D28	GBA0/IO81NPB1V4
D29	VCC
D30	GBA2/IO82PPB2V0
E1	GND
E2	IO303NPB7V3
E3	VCCIB7
E4	IO305PPB7V3
E5	VCC
E6	GAC0/IO02NDB0V0
E7	VCCIB0
E8	IO06PPB0V0
E9	IO24NDB0V2
E10	IO24PDB0V2
E11	IO13NDB0V1
E12	IO13PDB0V1

FG896	
Pin Number	**A3PE3000L Function**
E13	IO34NDB0V4
E14	IO34PDB0V4
E15	IO40NDB0V4
E16	IO49NDB1V1
E17	IO49PDB1V1
E18	IO50PDB1V1
E19	IO58PDB1V2
E20	IO60NDB1V2
E21	IO77PDB1V4
E22	IO68NDB1V3
E23	IO68PDB1V3
E24	VCCIB1
E25	IO74PDB1V4
E26	VCC
E27	GBB1/IO80PPB1V4
E28	VCCIB2
E29	IO82NPB2V0
E30	GND
F1	IO296PPB7V2
F2	VCC
F3	IO306PDB7V4
F4	IO297PDB7V2
F5	VMV7
F5	VMV7
F6	GND
F7	GNDQ
F8	IO12NDB0V1
F9	IO12PDB0V1
F10	IO10PDB0V1
F11	IO16PDB0V1
F12	IO22NDB0V2
F13	IO30NDB0V3
F14	IO30PDB0V3
F15	IO36PDB0V4
F16	IO48NDB1V0
F17	IO48PDB1V0
F18	IO50NDB1V1
F19	IO58NDB1V2
F20	IO60PDB1V2
F21	IO77NDB1V4
F22	IO72NDB1V3
F23	IO72PDB1V3
F24	GNDQ

FG896	
Pin Number	**A3PE3000L Function**
F25	GND
F26	VMV2
F27	IO86PDB2V0
F28	IO92PDB2V1
F29	VCC
F30	IO100NPB2V2
G1	GND
G2	IO296NPB7V2
G3	IO306NDB7V4
G4	IO297NDB7V2
G5	VCCIB7
G6	GNDQ
G7	VCC
G8	VMV0
G9	VCCIB0
G10	IO10NDB0V1
G11	IO16NDB0V1
G12	IO22PDB0V2
G13	IO26PPB0V3
G14	IO38NPB0V4
G15	IO36NDB0V4
G16	IO46NDB1V0
G17	IO46PDB1V0
G18	IO56NDB1V1
G19	IO56PDB1V1
G20	IO66NDB1V3
G21	IO66PDB1V3
G22	VCCIB1
G23	VMV1
G24	VCC
G25	GNDQ
G26	VCCIB2
G27	IO86NDB2V0
G28	IO92NDB2V1
G29	IO100PPB2V2
G30	GND
H1	IO294PDB7V2
H2	IO294NDB7V2
H3	IO300NDB7V3
H4	IO300PDB7V3
H5	IO295PDB7V2
H6	IO299PDB7V3
H7	VCOMPLA

FG896	
Pin Number	**A3PE3000L Function**
H8	GND
H9	IO08NDB0V0
H10	IO08PDB0V0
H11	IO18PDB0V2
H12	IO26NPB0V3
H13	IO28NDB0V3
H14	IO28PDB0V3
H15	IO38PPB0V4
H16	IO42NDB1V0
H17	IO52NDB1V1
H18	IO52PDB1V1
H19	IO62NDB1V2
H20	IO62PDB1V2
H21	IO70NDB1V3
H22	IO70PDB1V3
H23	GND
H24	VCOMPLB
H25	GBC2/IO84PDB2V0
H26	IO84NDB2V0
H27	IO96PDB2V1
H28	IO96NDB2V1
H29	IO89PDB2V0
H30	IO89NDB2V0
J1	IO290NDB7V2
J2	IO290PDB7V2
J3	IO302NDB7V3
J4	IO302PDB7V3
J5	IO295NDB7V2
J6	IO299NDB7V3
J7	VCCIB7
J8	VCCPLA
J9	VCC
J10	IO04NPB0V0
J11	IO18NDB0V2
J12	IO20NDB0V2
J13	IO20PDB0V2
J14	IO32NDB0V3
J15	IO32PDB0V3
J16	IO42PDB1V0
J17	IO44NDB1V0
J18	IO44PDB1V0
J19	IO54NDB1V1
J20	IO54PDB1V1

FG896	
Pin Number	**A3PE3000L Function**
J21	IO76NPB1V4
J22	VCC
J23	VCCPLB
J24	VCCIB2
J25	IO90PDB2V1
J26	IO90NDB2V1
J27	GBB2/IO83PDB2V0
J28	IO83NDB2V0
J29	IO91PDB2V1
J30	IO91NDB2V1
K1	IO288NDB7V1
K2	IO288PDB7V1
K3	IO304NDB7V3
K4	IO304PDB7V3
K5	GAB2/IO308PDB7V4
K6	IO308NDB7V4
K7	IO301PDB7V3
K8	IO301NDB7V3
K9	GAC2/IO307PPB7V4
K10	VCC
K11	IO04PPB0V0
K12	VCCIB0
K13	VCCIB0
K14	VCCIB0
K15	VCCIB0
K16	VCCIB1
K17	VCCIB1
K18	VCCIB1
K19	VCCIB1
K20	IO76PPB1V4
K21	VCC
K22	IO78PPB1V4
K23	IO88NDB2V0
K24	IO88PDB2V0
K25	IO94PDB2V1
K26	IO94NDB2V1
K27	IO85PDB2V0
K28	IO85NDB2V0
K29	IO93PDB2V1
K30	IO93NDB2V1
L1	IO286NDB7V1
L2	IO286PDB7V1
L3	IO298NDB7V3

FG896	
Pin Number	**A3PE3000L Function**
L4	IO298PDB7V3
L5	IO283PDB7V1
L6	IO291NDB7V2
L7	IO291PDB7V2
L8	IO293PDB7V2
L9	IO293NDB7V2
L10	IO307NPB7V4
L11	VCC
L12	VCC
L13	VCC
L14	VCC
L15	VCC
L16	VCC
L17	VCC
L18	VCC
L19	VCC
L20	VCC
L21	IO78NPB1V4
L22	IO104NPB2V2
L23	IO98NDB2V2
L24	IO98PDB2V2
L25	IO87PDB2V0
L26	IO87NDB2V0
L27	IO97PDB2V1
L28	IO101PDB2V2
L29	IO103PDB2V2
L30	IO119NDB3V0
M1	IO282NDB7V1
M2	IO282PDB7V1
M3	IO292NDB7V2
M4	IO292PDB7V2
M5	IO283NDB7V1
M6	IO285PDB7V1
M7	IO287PDB7V1
M8	IO289PDB7V1
M9	IO289NDB7V1
M10	VCCIB7
M11	VCC
M12	GND
M13	GND
M14	GND
M15	GND
M16	GND

FG896	
Pin Number	**A3PE3000L Function**
M17	GND
M18	GND
M19	GND
M20	VCC
M21	VCCIB2
M22	NC
M23	IO104PPB2V2
M24	IO102PDB2V2
M25	IO102NDB2V2
M26	IO95PDB2V1
M27	IO97NDB2V1
M28	IO101NDB2V2
M29	IO103NDB2V2
M30	IO119PDB3V0
N1	IO276PDB7V0
N2	IO278PDB7V0
N3	IO280PDB7V0
N4	IO284PDB7V1
N5	IO279PDB7V0
N6	IO285NDB7V1
N7	IO287NDB7V1
N8	IO281NDB7V0
N9	IO281PDB7V0
N10	VCCIB7
N11	VCC
N12	GND
N13	GND
N14	GND
N15	GND
N16	GND
N17	GND
N18	GND
N19	GND
N20	VCC
N21	VCCIB2
N22	IO106NDB2V3
N23	IO106PDB2V3
N24	IO108PDB2V3
N25	IO108NDB2V3
N26	IO95NDB2V1
N27	IO99NDB2V2
N28	IO99PDB2V2
N29	IO107PDB2V3

FG896	
Pin Number	**A3PE3000L Function**
N30	IO107NDB2V3
P1	IO276NDB7V0
P2	IO278NDB7V0
P3	IO280NDB7V0
P4	IO284NDB7V1
P5	IO279NDB7V0
P6	GFC1/IO275PDB7V0
P7	GFC0/IO275NDB7V0
P8	IO277PDB7V0
P9	IO277NDB7V0
P10	VCCIB7
P11	VCC
P12	GND
P13	GND
P14	GND
P15	GND
P16	GND
P17	GND
P18	GND
P19	GND
P20	VCC
P21	VCCIB2
P22	GCC1/IO112PDB2V3
P23	IO110PDB2V3
P24	IO110NDB2V3
P25	IO109PPB2V3
P26	IO111NPB2V3
P27	IO105PDB2V2
P28	IO105NDB2V2
P29	GCC2/IO117PDB3V0
P30	IO117NDB3V0
R1	GFC2/IO270PDB6V4
R2	GFB1/IO274PPB7V0
R3	VCOMPLF
R4	GFA0/IO273NDB6V4
R5	GFB0/IO274NPB7V0
R6	IO271NDB6V4
R7	GFB2/IO271PDB6V4
R8	IO269PDB6V4
R9	IO269NDB6V4
R10	VCCIB7
R11	VCC
R12	GND

FG896	
Pin Number	**A3PE3000L Function**
R13	GND
R14	GND
R15	GND
R16	GND
R17	GND
R18	GND
R19	GND
R20	VCC
R21	VCCIB2
R22	GCC0/IO112NDB2V3
R23	GCB2/IO116PDB3V0
R24	IO118PDB3V0
R25	IO111PPB2V3
R26	IO122PPB3V1
R27	GCA0/IO114NPB3V0
R28	VCOMPLC
R29	GCB1/IO113PPB2V3
R30	IO115NPB3V0
T1	IO270NDB6V4
T2	VCCPLF
T3	GFA2/IO272PPB6V4
T4	GFA1/IO273PDB6V4
T5	IO272NPB6V4
T6	IO267NDB6V4
T7	IO267PDB6V4
T8	IO265PDB6V3
T9	IO263PDB6V3
T10	VCCIB6
T11	VCC
T12	GND
T13	GND
T14	GND
T15	GND
T16	GND
T17	GND
T18	GND
T19	GND
T20	VCC
T21	VCCIB3
T22	IO109NPB2V3
T23	IO116NDB3V0
T24	IO118NDB3V0
T25	IO122NPB3V1

FG896	
Pin Number	**A3PE3000L Function**
T26	GCA1/IO114PPB3V0
T27	GCB0/IO113NPB2V3
T28	GCA2/IO115PPB3V0
T29	VCCPLC
T30	IO121PDB3V0
U1	IO268PDB6V4
U2	IO264NDB6V3
U3	IO264PDB6V3
U4	IO258PDB6V3
U5	IO258NDB6V3
U6	IO257PPB6V2
U7	IO261PPB6V3
U8	IO265NDB6V3
U9	IO263NDB6V3
U10	VCCIB6
U11	VCC
U12	GND
U13	GND
U14	GND
U15	GND
U16	GND
U17	GND
U18	GND
U19	GND
U20	VCC
U21	VCCIB3
U22	IO120PDB3V0
U23	IO128PDB3V1
U24	IO124PDB3V1
U25	IO124NDB3V1
U26	IO126PDB3V1
U27	IO129PDB3V1
U28	IO127PDB3V1
U29	IO125PDB3V1
U30	IO121NDB3V0
V1	IO268NDB6V4
V2	IO262PDB6V3
V3	IO260PDB6V3
V4	IO252PDB6V2
V5	IO257NPB6V2
V6	IO261NPB6V3
V7	IO255PDB6V2
V8	IO259PDB6V3

FG896	
Pin Number	**A3PE3000L Function**
V9	IO259NDB6V3
V10	VCCIB6
V11	VCC
V12	GND
V13	GND
V14	GND
V15	GND
V16	GND
V17	GND
V18	GND
V19	GND
V20	VCC
V21	VCCIB3
V22	IO120NDB3V0
V23	IO128NDB3V1
V24	IO132PDB3V2
V25	IO130PPB3V2
V26	IO126NDB3V1
V27	IO129NDB3V1
V28	IO127NDB3V1
V29	IO125NDB3V1
V30	IO123PDB3V1
W1	IO266NDB6V4
W2	IO262NDB6V3
W3	IO260NDB6V3
W4	IO252NDB6V2
W5	IO251NDB6V2
W6	IO251PDB6V2
W7	IO255NDB6V2
W8	IO249PPB6V1
W9	IO253PDB6V2
W10	VCCIB6
W11	VCC
W12	GND
W13	GND
W14	GND
W15	GND
W16	GND
W17	GND
W18	GND
W19	GND
W20	VCC
W21	VCCIB3

FG896	
Pin Number	**A3PE3000L Function**
W22	IO134PDB3V2
W23	IO138PDB3V3
W24	IO132NDB3V2
W25	IO136NPB3V2
W26	IO130NPB3V2
W27	IO141PDB3V3
W28	IO135PDB3V2
W29	IO131PDB3V2
W30	IO123NDB3V1
Y1	IO266PDB6V4
Y2	IO250PDB6V2
Y3	IO250NDB6V2
Y4	IO246PDB6V1
Y5	IO247NDB6V1
Y6	IO247PDB6V1
Y7	IO249NPB6V1
Y8	IO245PDB6V1
Y9	IO253NDB6V2
Y10	GEB0/IO235NPB6V0
Y11	VCC
Y12	VCC
Y13	VCC
Y14	VCC
Y15	VCC
Y16	VCC
Y17	VCC
Y18	VCC
Y19	VCC
Y20	VCC
Y21	IO142PPB3V3
Y22	IO134NDB3V2
Y23	IO138NDB3V3
Y24	IO140NDB3V3
Y25	IO140PDB3V3
Y26	IO136PPB3V2
Y27	IO141NDB3V3
Y28	IO135NDB3V2
Y29	IO131NDB3V2
Y30	IO133PDB3V2

5.0 REVISION HISTORY

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
B	03/2022	The following is the list of changes in revision B of the document: • Updated the ProASIC3L Ordering Information section: Interchanged the position of I and Y values.
A	02/2022	The following is the list of changes in revision A of the document: • The document number was changed from 51700097 to DS50003268. • The document was migrated to the Microchip template.
Revision 15	November, 2019	Removed the A3P250L device and its related details across this document.
		Migrated to Microchip-Microchip template change.
Revision 14	June, 2015	Updated "ProASIC3L Ordering Information" Interchanged the positions of Y-Security Feature and I- Application (Temperature Range) (SAR 67298). Added Note "Only devices with package size greater than or equal to 5x5 are supported".
		Added A3P1000L device to the PQFP package in Table 2-5 (SAR 58737).
		Added drive strengths 2 and 4 to 3.3 V LVTTL / 3.3 V LVCMOS in Table 2-40 (SAR 57185).
		Changed A3P3000L to A3PE3000L in Table 3-1 (SAR 44121).
		Removed duplicate pin numbers in the FG896 packages (SAR 60051).
		Updated "VCCIBx I/O Supply Voltage" (SAR 43323).
Revision 13	January, 2013	The "ProASIC3L Ordering Information" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43221).
		Added following notes to Table 2-2 • Recommended Operating Conditions [1]: "All ProASIC3L devices must be programmed with the VCC core voltage at 1.5 V" (SAR 39910) and "The programming temperature range supported is Tambient = 0°C to 85°C" (SAR 43645).
		The note in Table 2-210 • ProASIC3L CCC/PLL Specification and Table 2-211 • ProASIC3L CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42572).
		Signal names have been made consistent (SAR 38910).
		Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 40286). Live at Power-Up (LAPU) has been replaced with 'Instant On'.
Revision 12	September, 2012	The "Security" section was modified to clarify that Microchip does not support read-back of programmed data.

Revision	Date	Description
Revision 11	August, 2012	Added a Note stating "VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information." to Table 2-1 • Absolute Maximum Ratings and Table 2-2 • Recommended Operating Conditions [1] (SAR 38316).
		The "Quiescent Supply Current" section was updated. Table 2-7 • Power Supply State per Mode is new, and Table 2-9 • Quiescent Supply Current (IDD) Characteristics, ProASIC3L Sleep Mode* and Table 2-11 • Quiescent Supply Current (IDD) Characteristics, No Flash*Freeze Mode[1] were updated for Core Voltage 1.2 V. Notes were also updated for Table 2-9, Table 2-10, and Table 2-11 (SAR 34746).
		The drive strength, IOL, and IOH value for 3.3 V GTL and 2.5 V GTL was changed from 25 mA to 20 mA in the following tables (SAR 37364): Table 2-23 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings Table 2-29 • Summary of I/O Timing Characteristics—Software Default Settings Table 2-32 • Summary of I/O Timing Characteristics—Software Default Settings Table 2-36 • I/O Output Buffer Maximum Resistances[1] Table 2-40 • I/O Short Currents IOSH/IOSL Table 2-134 • Minimum and Maximum DC Input and Output Levels Table 2-138 • Minimum and Maximum DC Input and Output Levels Also added note stating "Output drive strength is below JEDEC specification." for Tables Table 2-29, Table 2-32, Table 2-36, and Table 2-40. Additionally, the IOL and IOH values for 3.3 V GTL+ and 2.5 V GTL+ were corrected from 51 to 35 (for 3.3 V GTL+) and from 40 to 33 (for 2.5 V GTL+) in table Table 2-23 (SAR 39715).
Revision 11 continued		Figure 2-12 • AC Loading in the "3.3 V PCI, 3.3 V PCI-X" section was updated to match Table 2-127 • AC Waveforms, Measuring Points, and Capacitive Loads (SAR 34890).
		In Table 2-180 • Minimum and Maximum DC Input and Output Levels, VIL and VIH were revised so that the maximum is 3.6 V for all listed values of VCCI (SAR 37690).
		The following sentence was removed from the "VMVx I/O Supply Voltage (quiet)" section in the "Pin Descriptions and Packaging" chapter: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with “Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks” (SAR 38316). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement.
		Pin K15 of the "FG484" pin table for A3P600L was corrected from VvB1 to VCCIB1 (SAR 38788).

Revision	Date	Description
Revision 10	May, 2012	The "In-System Programming (ISP) and Security" section and "Security" section were revised to clarify that although no existing security measures can give an absolute guarantee, Microchip FPGAs implement the best security available in the industry (SAR 34670).
		The Y security option and Licensed DPA Logo were added to the "ProASIC3L Ordering Information" section. The trademarked Licensed DPA Logo identifies that a product is covered by a DPA counter-measures license from Cryptography Research (SAR 34728).
		The "ProASIC3L Device Status" table was updated to show that all ProASIC3L devices have changed in status from Advance to Production (SAR 38198).
		The opening sentence of the "General Description" section was revised for clarity to "The ProASIC3L family of Microchip flash FPGAs dramatically reduces dynamic power consumption by 40% and static power by 50% compared to the equivalent ProASIC3 device" (SAR 22661).
		The following sentence was removed from the "Advanced Architecture" section: "In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of ProASIC3L devices via an IEEE 1532 JTAG interface" (SAR 34690).
		The "Specifying I/O States During Programming" section is new (SAR 34700).
		Table 1-1 • I/O Standards Supported is new. The "I/Os with Advanced I/O Standards" section was revised to add definitions of hot-swap and cold-sparing (SAR 37732).
		In Table 2-2 • Recommended Operating Conditions [1], VPUMP programming voltage for operation was changed from "0 to 3.45 V" to "0 to 3.6 V" (SAR 32257).
		Values for 1.5 V were added to Table 2-8 • Quiescent Supply Current (IDD) Characteristics, ProASIC3L Flash*Freeze Mode* and Table 2-11 • Quiescent Supply Current (IDD) Characteristics, No Flash*Freeze Mode[1] (SAR 30578).
		The reference to guidelines for global spines and VersaTile rows, given in the "Global Clock Contribution—P_{CLOCK}" section, was corrected to the "Spine Architecture" section of the Global Resources chapter in the *ProASIC3L FPGA Fabric User's Guide* (SAR 34737).
		t_{DOUT} was corrected to t_{DIN} in Figure 2-4 • Input Buffer Timing Model and Delays (example) (SAR 37110).

Revision	Date	Description
Revision 10 continued		3.3 V LVCMOS and 1.2 V LVCMOS wide range were added to applicable tables in the "Overview of I/O Performance" section and "Detailed I/O DC Characteristics" section. Values for 1.2 V LVCMOS were added to tables in the "Detailed I/O DC Characteristics" section. The "3.3 V LVCMOS Wide Range" section and "1.2 V LVCMOS Wide Range" section, with Minimum and Maximum DC Input and Output Levels tables, are new. Complete timing data for wide range will be available in a later revision of the datasheet (SARs 37161, 38188).
		The notes regarding drive strength in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section tables were revised for clarification. They now state that the minimum drive strength for the default software configuration when run in wide range is ±100 µA. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, refer to the IBIS models (SAR 34761).
		Table 2-39 • I/O Weak Pull-Up/Pull-Down Resistances was updated with additional values and the definitions of $R_{WEAK\ PULL\text{-}UP\text{-}MAX}$ and $R_{WEAK\ PULL\text{-}DOWN\text{-}MAX}$ were corrected (SAR 34756).
		The paragraph above Table 2-44 • Duration of Short Circuit Event before Failure was revised to change the maximum temperature from 110°C to 100°C, with an example of six months instead of three months. The row for 110°C was removed from the table for consistency with Table 2-2 • Recommended Operating Conditions [1] (SAR 34744).
		The AC Loading figures in the "Single-Ended I/O Characteristics" section were updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34890).
		The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 34797): "It uses a 5 V–tolerant input buffer and push-pull output buffer."
		The table notes were revised for LVDS Table 2-174 • Minimum and Maximum DC Input and Output Levels (SAR 34813).
		Values for the maximum frequency for input and output DDR were added to tables in the "DDR Module Specifications" section (SAR 34805).
		Minimum pulse width High and Low values were added to the tables in the "Global Tree Timing Characteristics" section. The maximum frequency for global clock parameter was removed from these tables because a frequency on the global is only an indication of what the global network can do. There are other limiters such as the SRAM, I/Os, and PLL. SmartTime software should be used to determine the design frequency (SAR 36965).
		Table 2-210 • ProASIC3L CCC/PLL Specification and Table 2-210 • ProASIC3L CCC/PLL Specification were updated. A note was added to indicate that when the CCC/PLL core is generated by Microchip core generator software, not all delay values of the specified delay increments are available (SAR 34825).
		Figure 2-46 • Write Access after Write onto Same Address, Figure 2-47 • Read Access after Write onto Same Address, and Figure 2-48 • Write Access after Read onto Same Address were deleted. Reference was made to a new application note, *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*, which covers these cases in detail (SAR 34873). The port names in the SRAM "Timing Waveforms", SRAM "Timing Characteristics" tables, Figure 2-50 • FIFO Reset, and the FIFO "Timing Characteristics" tables were revised to ensure consistency with the software names (SAR 35751).
		Figure 2-48 • FIFO Read and Figure 2-49 • FIFO Write are new (SAR 34849).
		The "Pin Descriptions and Packaging" chapter is new (SAR 34773).

Revision	Date	Description
Revision 10 (continued)		Package names used in the "Package Pin Assignments" section were revised to match standards given in *Package Mechanical Drawings* (SAR 34773).
July 2010		The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "ProASIC3L Device Status" table on page IV indicates the status for each device in the device family.

Revision	Date	Changes
Revision 9 Product Brief v1.3	Feb, 2009	The "I/Os Per Package [1]" table was revised to change the number of differential I/O pairs for A3PE3000L from 300 to 310.
		Table 2 • ProASIC3L FPGAs Package Sizes Dimensions is new.
Revision8 Product Brief v1.2	Feb, 2009	The "Advanced and Pro (Professional) I/Os" section was revised to add two bullets regarding wide range power supply voltage support.
		3.0 V wide range was added to the list of supported voltages in the "I/Os with Advanced I/O Standards" section. The "Wide Range I/O Support" section is new.
Revision 7 DC and Switching Characteristics Advance v0.6	Aug, 2008	3.0 V LVCMOS wide range support data was added to Table 2-2 • Recommended Operating Conditions [1].
		3.3 V LVCMOS wide range support data was added to Table 2-23 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings to Table 2-25 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings.
		3.3 V LVCMOS wide range support data was added to Table 2-27 • Summary of AC Measuring Points.
		3.3 V LVCMOS wide range support text was added to the "3.3 V LVTTL / 3.3 V LVCMOS" section.
		Table 2-62 • Minimum and Maximum DC Input and Output Levels for LVCMOS 3.3 V Wide Range is new.
Revision 6 DC and Switching Characteristics Advance v0.5	Aug, 2008	Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays was updated to add several new rows of values.
		Table 2-8 • Quiescent Supply Current (IDD) Characteristics, ProASIC3L Flash*Freeze Mode* through Table 2-11 • Quiescent Supply Current (IDD) Characteristics, No Flash*Freeze Mode[1] were updated to add 1.5 V core voltage.
		Table 2-19 • Different Components Contributing to Dynamic Power Consumption in ProASIC3L Devices at 1.5 V VCC is new.
		Table 2-20 • Different Components Contributing to the Static Power Consumption in ProASIC3L Devices was updated to add the static PLL contribution at 1.5 V core operation.
		Timing tables were updated to include tables for 1.5 V core voltage.
		Table 2-210 • ProASIC3L CCC/PLL Specification was updated for core voltage 1.2 V and Table 2-211 • ProASIC3L CCC/PLL Specification for 1.5 V is new.

Revision	Date	Changes
Revision 5 Product Brief v1.1 DC and Switching Characteristics Advance v0.4	July, 2008	As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change 1.2 V / 1.5 V to 1.2 V to 1.5 V.
Revision 4 DC and Switching Characteristics Advance v0.3	June, 2008	Tables have been updated to include the LVCMOS 1.2 V I/O set. DDR Tables have two additional data points added to reflect both edges for Input DDR setup and hold time. Power data table has been updated to match SmartPower data rather then simulation values.
		Table 2-1 • Absolute Maximum Ratings was updated to add VMV to the VCCI parameter row and to remove the word "output" from the parameter description for VCCI. Table note 3 was added.
		Table 2-2 • Recommended Operating Conditions [1] was updated to add table note references and rearrange the order of notes. VMV was added to the VCCI parameter row. A new row was added for VCC, 1.5 V DC core supply voltage. The table note stating that 1.5 V data will be released at a later date is new. The table note on VMV pins is new.
		Table 2-4 • Overshoot and Undershoot Limits [1]. The title was revised to remove "as measured on quiet I/Os." Table note 2 was revised to remove "estimated SSO density over cycles." Table note 3 was revised to remove "refers only to overshoot/ undershoot limits for simultaneous switching I/Os."
		EQ 2 was updated. The temperature was changed to 100°C, and therefore the end result changed.
		The table notes for Table 2-8 • Quiescent Supply Current (IDD) Characteristics, ProASIC3L Flash*Freeze Mode* and Table 2-9 • Quiescent Supply Current (IDD) Characteristics, ProASIC3L Sleep Mode* were updated to remove VMV and include P_{DC6} and P_{DC7}. The table note for Table 2-8 • Quiescent Supply Current (IDD) Characteristics, ProASIC3L Flash*Freeze Mode* was updated to include VJTAG.
		Table 2-10 • Quiescent Supply Current (IDD) Characteristics, Shutdown Mode is new.
		Note 2 of Table 2-11 • Quiescent Supply Current (IDD) Characteristics, No Flash*Freeze Mode[1] was updated to include VCCPLL. Note 4 was updated to include PDC6 and PDC7.
		Table 2-12 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings through Table 2-17 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings [1]were updated to change PDC2 to PDC6 and PDC3 to PDC7. The table notes were updated to reflect that power was measured on VCCI. The subtitle of the table was changed from "Applicable to Advanced I/O Banks" to "Applicable to Pro I/O Banks."
		The word "input" in the titles of Table 2-15 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings [1] and Table 2-16 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings [1], was changed to "output."
		The value of C_{LOAD} for single-ended 3.3 V PCI was changed to 10 from 5 in Table 2-15 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings [1] through Table 2-17 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings [1].

Revision	Date	Changes
Revision 4 (cont'd)		The last section of Table 2-18 • Different Components Contributing to Dynamic Power Consumption in ProASIC3L Devices at 1.2 V VCC was made into a new table: Table 2-19 • Different Components Contributing to Dynamic Power Consumption in ProASIC3L Devices at 1.5 V VCC. The table numbers referenced for device-specific dynamic power for P_{AC9} and P_{AC10} were changed in Table 2-18 • Different Components Contributing to Dynamic Power Consumption in ProASIC3L Devices at 1.2 V VCC. The definition of P_{DC5} was updated and parameters P_{DC6} and P_{DC7} were added to Table 2-20 • Different Components Contributing to the Static Power Consumption in ProASIC3L Devices.
		The "Total Static Power Consumption—P_{STAT}" section was updated to revise the calculation of P_{STAT}, including P_{DC6} and P_{DC7}.
		Footnote 1 was updated to include information about P_{AC13}.
		Table 2-43 • Schmitt Trigger Input Hysteresis, Hysteresis Voltage Value (Typ) for Schmitt Mode Input Buffers was updated to include the hysteresis value for 1.2 V LVCMOS.
		The "1.2 V LVCMOS (JESD8-12A)" section is new.
Revision 3 (Apri2008) Product Brief v1.0		The product brief was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview.
Packaging v1.1		The "FG324" package diagram was replaced.
Revision 2 Product Brief rev. 1	Apr, 2008	Reference to M1A3P250L was removed from Table 1 • ProASIC3 Low-Power Product Family, the "I/Os Per Package [1]" table, the "ProASIC3L Ordering Information" section, and the "Temperature Grade Offerings" table. The table note regarding M1A3P250L was removed from the "I/Os Per Package [1]" table.
Revision 1	Feb, 2008	The "PLL Behavior at Brownout Condition" section is new.
DC and Switching Characteristics Advance v0.2		Table 2-204 • A3P250L Global Resource – Applies to 1.5 V DC Core Voltage, Table 2-204 • A3P600L Global Resource – Applies to 1.5 V DC Core Voltage, Table 2-206 • A3P1000L Global Resource – Applies to 1.5 V DC Core Voltage, and Table 2-208 • A3PE3000L Global Resource – Applies to 1.5 V DC Core Voltage were updated with values for t_{RCKL}, t_{RCKH}, and t_{RCKSW}.
		The worst-case commercial conditions were added to Table 2-219 • Embedded FlashROM Access Time– Applies to 1.2 V DC Core Voltage.
		Table 2-18 • Different Components Contributing to Dynamic Power Consumption in ProASIC3L Devices at 1.2 V VCC was updated to revise the value for P_{AC14} and add parameters P_{DC1} through P_{DC5} to the table.

5.1 Datasheet Categories

5.1.1 CATEGORIES

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "ProASIC3L Device Status" table on page IV, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

5.1.2 PRODUCT BRIEF

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

5.1.3 ADVANCE

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

5.1.4 PRELIMINARY

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

5.1.5 PRODUCTION

This version contains information that is considered to be final.

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