HARRIS SEMICONDUCTOR

CD54/74FCT240, CD54/74FCT240AT, CD54/74FCT241, CD54/74FCT244, CD54/74FCT244AT

FCT Interface Logic
Octal Buffers/Line Drivers, Three-State

February 1996

Features

- CD54/74FCT240, CD54/74FCT240AT - Inverting
- CD54/74FCT241, CD54/74FCT244, CD54/74FCT244AT - Non-Inverting
- Buffered Inputs
- Typical Propagation Delay: 4.1ns at VCC = 5V, TA = 25°C (FCT240AT, FCT244AT)
- SCR-Latchup-Resistant BiCMOS Process and Circuit Design
- FCTXXX Types - Speed of Bipolar FAST®/AS/S; FCTXXXAT Types - 30% Faster Than FAST/AS/S with Significantly Reduced Power Consumption
- 48mA to 64mA Output Sink Current (Commercial/Extended Industrial)
- Output Voltage Swing Limited to 3.7V at VCC = 5V
- Controlled Output-Edge Rates
- Input/Output Isolation to VCC
- BiCMOS Technology with Low Quiescent Power

Ordering Information

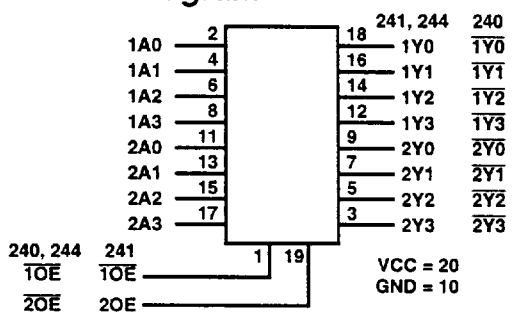
PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54/74FCT240E	-55 to 125, 0 to 70	20 Ld PDIP
CD54/74FCT240ATE	-55 to 125, 0 to 70	20 Ld PDIP
CD54/74FCT241E	-55 to 125, 0 to 70	20 Ld PDIP
CD54/74FCT244E	-55 to 125, 0 to 70	20 Ld PDIP
CD54/74FCT244ATE	-55 to 125, 0 to 70	20 Ld PDIP
CD54/74FCT240M	-55 to 125, 0 to 70	20 Ld SOIC
CD54/74FCT240ATM	-55 to 125, 0 to 70	20 Ld SOIC
CD54/74FCT241M	-55 to 125, 0 to 70	20 Ld SOIC
CD54/74FCT244M	-55 to 125, 0 to 70	20 Ld SOIC
CD54/74FCT244ATM	-55 to 125, 0 to 70	20 Ld SOIC
CD54/74FCT240SM	-55 to 125, 0 to 70	20 Ld SSOP
CD54/74FCT241SM	-55 to 125, 0 to 70	20 Ld SSOP
CD54/74FCT244SM	-55 to 125, 0 to 70	20 Ld SSOP
CD54FCT240H	-55 to 125	
CD54FCT241H	-55 to 125	
CD54FCT244H	-55 to 125	

Description

The CD54/74FCT240, 240AT, 241, 244 and 244AT three-state octal buffers/line drivers use a small-geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below VCC. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes VCC bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48mA to 64mA.

The CD54/74FCT240, 240AT, 244 and 244AT have active-LOW output enables ($\overline{1OE}$, $\overline{2OE}$). The CD54/74FCT241 and CD54/74FCT241AT have one active-LOW ($\overline{1OE}$) and one active-HIGH (2OE) output enable.

Functional Diagram



CD54/74FCT240, CD54/74FCT240AT TRUTH TABLE

INPUT	INPUT	OUTPUT
$\overline{1OE}$, $\overline{2OE}$	A	$\overline{Y}$
L	L	H
L	H	L
H	X	Z

CD54/74FCT244, CD54/74FCT244AT TRUTH TABLE

INPUT	INPUT	OUTPUT
$\overline{1OE}$, $\overline{2OE}$	A	Y
L	L	H
L	H	L
H	X	Z

CD54/74FCT241 TRUTH TABLE

INPUT		OUTPUT	INPUT		OUTPUT
$\overline{1OE}$	1A	1Y	2OE	2A	2Y
L	L	L	L	X	Z
L	H	H	H	L	L
H	X	Z	H	H	H

NOTE: H = High Voltage Level, L = LOW Voltage Level
X = Immaterial, Z = HIGH Impedance

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CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 2227.3

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5V to 6V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5V$) ..... -20mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5V$) ..... -50mA
DC OUTPUT SINK CURRENT per Output Pin, I_O ..... +70mA
DC OUTPUT SOURCE CURRENT per Output Pin, I_O ..... -30mA
DC V_{CC} CURRENT (I_{CC}) 140mA
DC GROUND CURRENT (I_{GND}) 528mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C (PACKAGE TYPE E) 500mW
For T_A = +100°C to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8mW/°C to 300mW
For T_A = -55°C to +70°C (PACKAGE TYPE M) 400mW
For T_A = +70°C to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6mW/°C to 70mW
For T_A = -55°C to +70°C (PACKAGE TYPE SM) 500mW
For T_A = +70°C to +125°C (PACKAGE TYPE SM) ..... Derate Linearly at 6.6mW/°C to 135mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE E, M, SM ..... -55°C to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) from case for 10s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only ..... +300°C

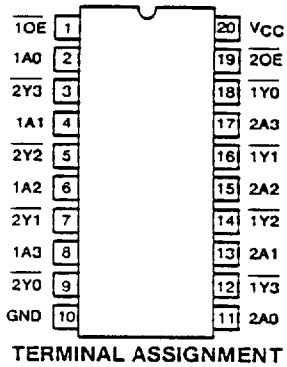
RECOMMENDED OPERATING CONDITIONS:

The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

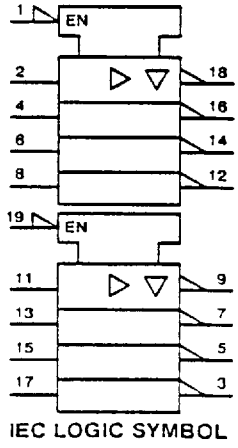
CHARACTERISTIC		MIN	MAX	UNITS
Supply-Voltage Range, V_{CC}*:	CD74 Series, T_A = 0°C to 70°C	4.75	5.25	V
	CD54 Series, T_A = -55°C to +125°C	4.5	5.5	V
DC Input Voltage, V_I		0	V_{CC}	V
DC Output Voltage, V_O		0	$\leq V_{CC}$	V
Operating Temperature, T_A		-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv		0	10	ns/V

* Unless otherwise specified, all voltages are referenced to ground.

CD54/74FCT240/240AT TYPES

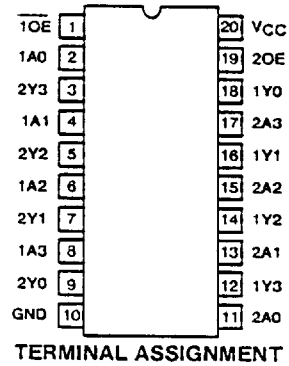


TERMINAL ASSIGNMENT



IEC LOGIC SYMBOL

CD54/74FCT241 TYPE



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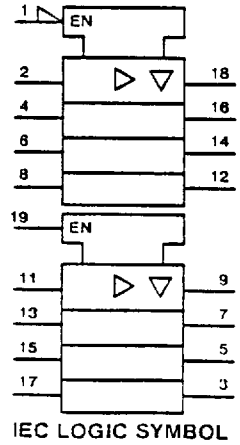
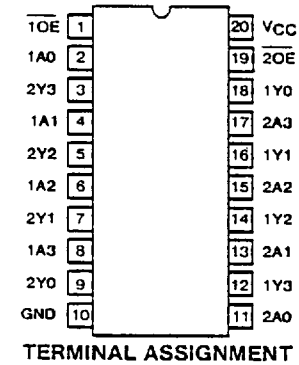


IEC LOGIC SYMBOL

CD54/74FCT244/244AT TYPES



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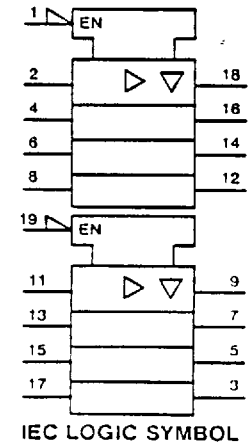


IEC LOGIC SYMBOL

STATIC ELECTRICAL CHARACTERISTICS

FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; V_{CC} max = 5.25V, V_{CC} min = 4.75V
54FCT Extended Industrial Temperature Range, -55°C to +125°C; V_{CC} max = 5.5V, V_{CC} min = 4.5V

CHARACTERISTICS		TEST CONDITIONS			AMBIENT TEMPERATURE (T_A)						UNITS
					+25°C		0°C to +70°C		-55°C to +125°C		
		V_I (V)	I_O (mA)	V_{CC} (V)	MIN	MAX	MIN	MAX	MIN	MAX	
High-Level Input Voltage	V_{IH}			4.5 to 5.5	2	-	2	-	2	-	V
Low-Level Input Voltage	V_{IL}			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High-Level Output Voltage	V_{OH}	V_{IH} or	-15	MIN	2.4	-	2.4	-	-	-	V
		V_{IL}	-12	MIN	2.4	-	-	-	2.4	-	V
Low-Level Output Voltage	V_{OL}	V_{IH} or	64	MIN	-	0.55	-	0.55	-	-	V
		V_{IL}	48	MIN	-	0.55	-	-	-	0.55	V
High-Level Input Current	I_{IH}	V_{CC}		MAX	-	0.1	-	1	-	1	µA
Low-Level Input Current	I_{IL}	GND		MAX	-	-0.1	-	-1	-	-1	µA
3-State Leakage Current	I_{OZH}	V_{CC}		MAX	-	0.5	-	10	-	10	µA
	I_{OZL}	GND		MAX	-	-0.5	-	-10	-	-10	µA
Short-Circuit Output Current *	I_{OS}	V_{CC} or GND $V_O = 0$		MAX	-60	-	-60	-	-60	-	mA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	MIN	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	MAX	-	8	-	80	-	500	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4V †		MAX	-	1.6	-	1.6	-	2	mA

* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
† Inputs that are not measured are at V_{CC} or GND.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

Switching Specifications FCT Series tr, tf = 2.5ns, C_L = 50pF, R_L - See Figure 2

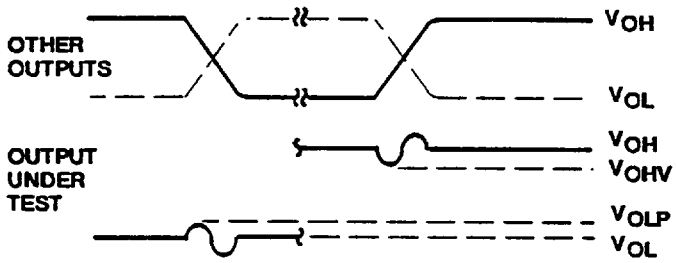
PARAMETER		SYMBOL	V_{CC} (V)	+25°C	0°C to +70°C		-55°C to +125°C		+25°C	0°C to +70°C		-55°C to +125°C		UNITS
				TYP	MIN	MAX	MIN	MAX	TYP	MIN	MAX	MIN	MAX	
Propagation Delays														
Data to Outputs	FCT240/AT	t_{PLH}, t_{PHL}	5†	5	1.5	8	1.5	9	4.4	1.5	5.6	1.5	6.7	ns
	FCT241	t_{PLH}, t_{PHL}	5	4	1.5	6.5	1.5	7	-	-	-	-	-	ns
	FCT244/AT	t_{PLH}, t_{PHL}	5	4.5	1.5	6.5	1.5	7	3.8	1.5	5.3	1.5	6.2	µs
Output Enable Times	FCT240/AT	t_{PZL}, t_{PZH}	5	7	1.5	10	1.5	10.5	4.7	1.5	6.2	1.5	7.7	µs
	FCT241	t_{PZL}, t_{PZH}	5	5.5	1.5	8	1.5	8.5	-	-	-	-	-	ns
	FCT244/AT	t_{PZL}, t_{PZH}	5	6	1.5	8	1.5	8.5	4.8	1.5	6.5	1.5	7.8	ns
Output Disable Times	FCT240/AT	t_{PLZ}, t_{PHZ}	5	6	1.5	9.5	1.5	10	4	1.5	5.6	1.5	6.5	µs
	FCT241	t_{PLZ}, t_{PHZ}	5	4.5	1.5	7	1.5	7.5	-	-	-	-	-	ns
	FCT244/AT	t_{PLZ}, t_{PHZ}	5	5	1.5	7	1.5	7.5	4.5	1.5	5.8	1.5	6.8	µs
Power Dissipation Capacitance	FCT240/AT	C_{PD}§	-	38 Typical					38 Typical					pF
	FCT241	C_{PD}§	-	33 Typical					-					pF
	FCT244/AT	C_{PD}§		35 Typical					35 Typical					pF
Min. (Valley) V_{OHV} During Switching of Other Outputs (Output Under Test Not Switching)		V_{OHV} See Figure 1	5	0.5 Typical at +25°C										V
Max. (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)		V_{OLP} See Figure 1	5	1 Typical at +25°C										V
Input Capacitance		C_I	-	-	-	10	-	10	-	-	10	-	10	pF
3-State Output Capacitance		C_O	-	-	-	15	-	15	-	-	15	-	15	pF

† 5V: min. is at 5.5V, max. is at 4.5V.
5V: min. is at 5.25V for 0°C to +70°C, max. is at 4.75V for 0°C to +70°C, typ. is at 5V

§ C_{PD}, measured per function, is used to determine the dynamic power consumption. P_D (per package) = V_{CC} I_{CC} + Σ (V_{CC}^2 fi C_{PD} + V_O^2 fo C_L + V_{CC} ΔI_{CC} D) where:

V_{CC} = supply voltage
ΔI_{CC} = flow through current x unit load
C_L = output load capacitance
D = duty cycle of input high
fo = output frequency
fi = input frequency

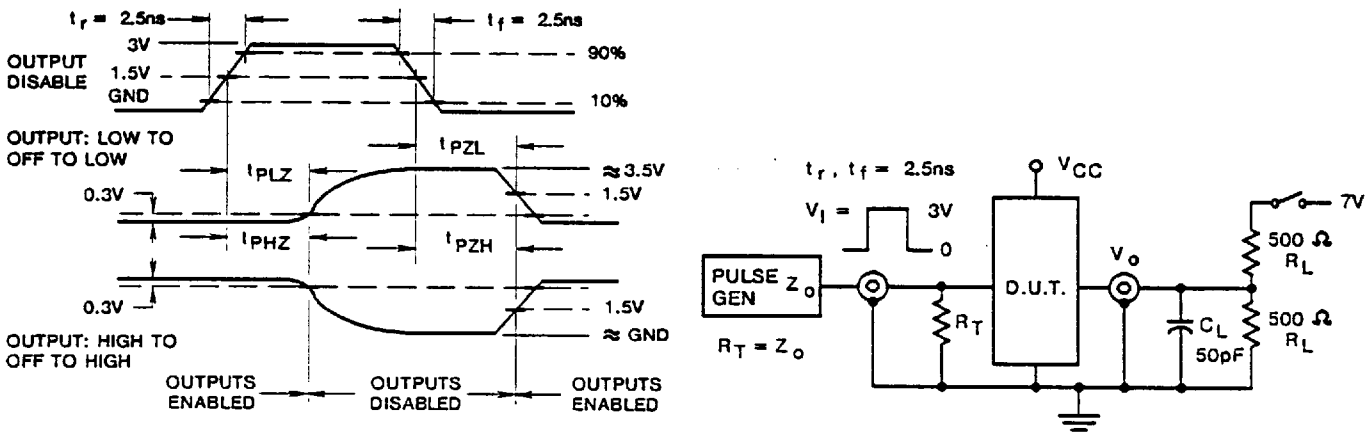
PARAMETER MEASUREMENT INFORMATION



NOTES:

1. V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH}.
2. Input pulses have the following characteristics: PRR ≤ 1MHz, t_r = 2.5ns, t_f = 2.5ns, skew 1ns.
3. R.F. fixture with 700-MHz design rules required. IC should be soldered into test board and bypassed with 0.1μF capacitor. Scope and probes require 700-MHz bandwidth.

Figure 1 - Simultaneous switching transient waveforms.



TEST	SWITCH POSITION
t_{PLZ}, t_{PZL}, OPEN DRAIN	CLOSED
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	OPEN

Figure 2 - Three-state propagation delay times and test circuit.

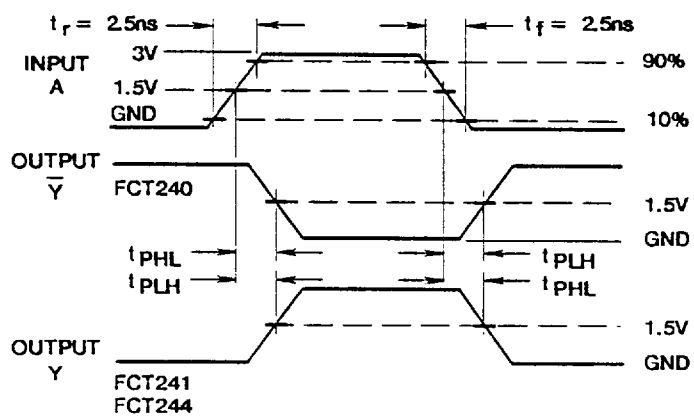


Figure 3 - Propagation delay times.