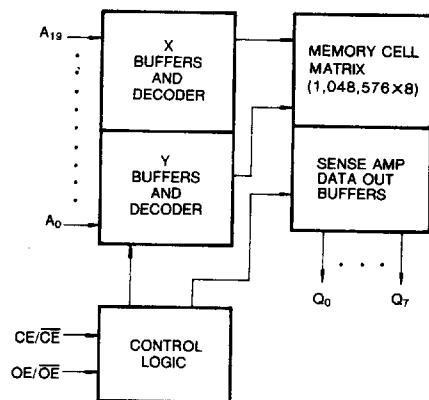


KM23C8005B(G)**CMOS MASK ROM****8M-Bit (1M × 8) CMOS MASK ROM****FEATURES**

- 1,048,576 × 8 bit organization
- Fast access time
Random access: 100ns (max.)
Page access: 50ns (max.)
- Supply voltage: single +5V
- Current consumption
Operating: 80 mA(max.)
Standby: 50 μ A(max.)
- Fully static operation
- All inputs and outputs TTL compatible
- Three state outputs
- Polarity programmable chip enable and output enable pin
- Package: 32-pin, 600 mil, plastic DIP
(JEDEC standard)
32-pin, 525 mil, plastic SOP

FUNCTIONAL BLOCK DIAGRAM**GENERAL DESCRIPTION**

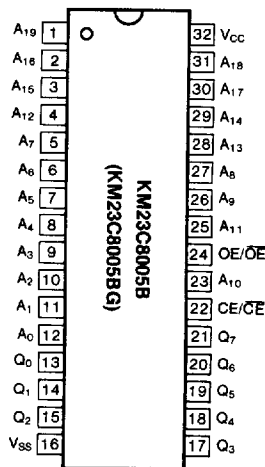
The KM23C8005B is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organized either as 1,048,576 × 8 bit.

This device includes PAGE read mode function, page read mode allows two to four words of data to be read fast in the same page. CE and A₂-A₁₉ should not be changed.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of micro-processor, and data memory, character generator.

The KM23C8005B is packaged in a 32-DIP and the KM23C8005B in a 32-SOP, provides polarity programmable CE and OE buffer as user option mode.

PIN CONFIGURATION

Pin Name	Pin Function
A ₀ -A ₁	Page Address Inputs
A ₂ -A ₁₉	Address Inputs
Q ₀ -Q ₈	Data Outputs
CE/ $\overline{\text{CE}}$ *	Chip Enable
OE/ $\overline{\text{OE}}$ *	Output Enable
V _{CC}	Power (+5V)
V _{SS}	Ground

* User Selectable Polarity

KM23C8005B(G)**CMOS MASK ROM****ABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	-0.3 to +7.0	V
Temperature Under Bias	T_{bias}	-10 to +85	°C
Storage Temperature	T_{stg}	-55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS} , $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, $f = 6.7\text{MHz}$ all output open	—	80	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC}$, all output open	—	50	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	$V_{CC} + 0.3$	V
Input Low Voltage, All Inputs	V_{IL}		-0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu\text{A}$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1\text{mA}$	—	0.4	V

CAPACITANCE ($T_A = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0\text{V}$	—	12.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0\text{V}$	—	12.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/\overline{CE}	OE/\overline{OE}	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	D_{OUT}	Active

KM23C8005B(G)

CMOS MASK ROM

AC CHARACTERISTICS ($T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

TEST CONDITIONS

Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and $C_L = 100\text{pF}$

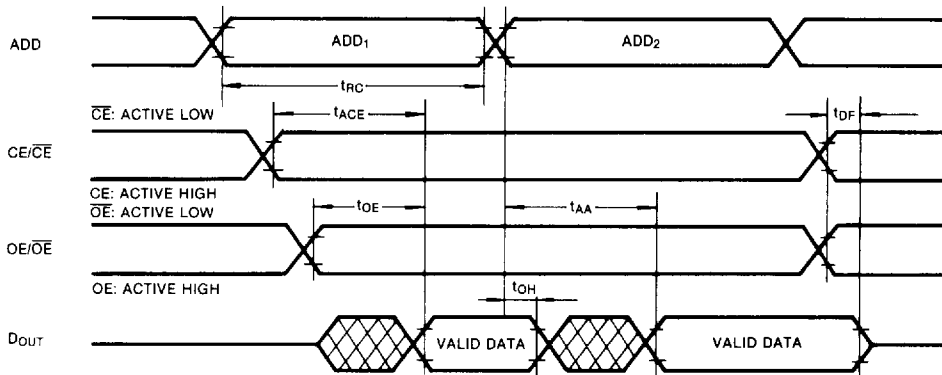
READ CYCLE

Parameter	Symbol	KM23C8005B(G)-10		KM23C8005B(G)-12		KM23C8005B(G)-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		120		150		ns
Chip Enable Access Time	t_{ACE}		100		120		150	ns
Address Access Time	t_{AA}		100		120		150	ns
Page Address Access Time	t_{PA}		50		60		70	ns
Output Enable Access Time	t_{OE}		50		60		70	ns
Output or Chip Disable to Output High-Z	t_{DF}		20		20		30	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

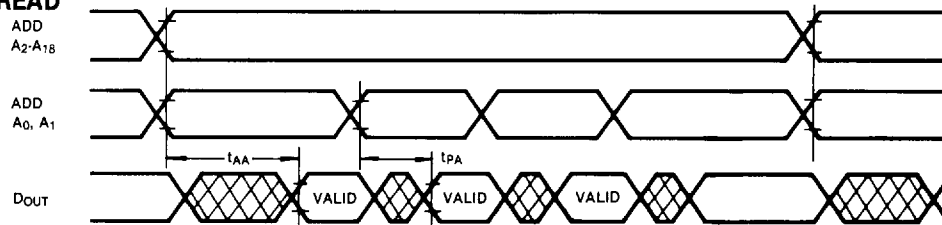
* Page Address: A_0, A_1

TIMING DIAGRAM

READ



PAGE READ



3

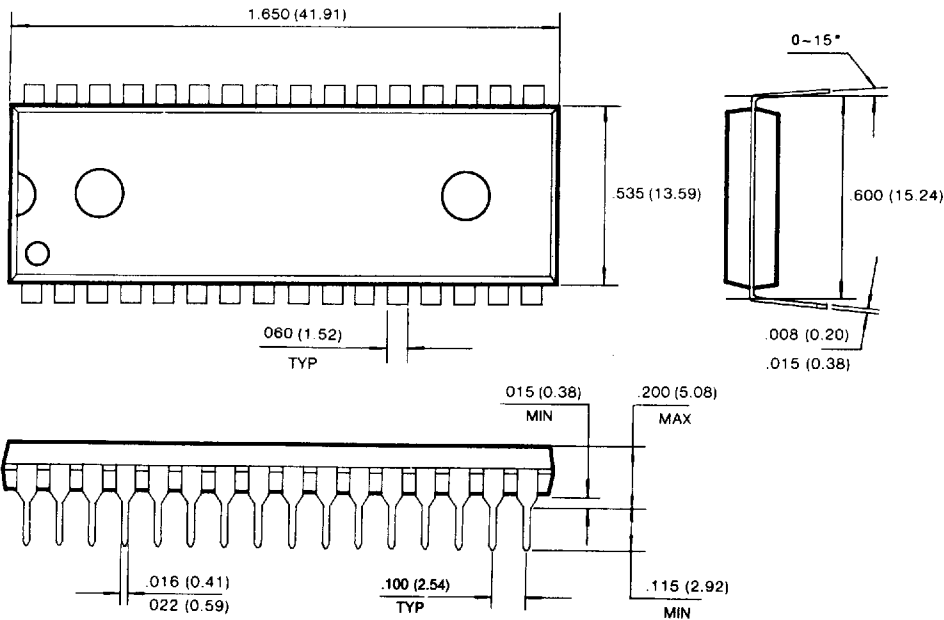
KM23C8005B(G)

CMOS MASK ROM

PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C8005B)

Units: Inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23C8005BG)

