FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **Inputs accept voltages upto 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **Output drive capability 50 Ω transmission lines @ 85 °C**
- **Non-inverting data path**

DESCRIPTION

The 74LVC257 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC257 is a quad 2-input multiplexer with 3-state outputs, which select 4 bits of data from two sources under the control of a common data select input (S). The data inputs from source 0 ($1I_0$ to $4I_0$) are selected when input S is LOW and the data inputs from source 1 ($1I_1$ to $4I_1$) are selected when S is HIGH. Data appears at the outputs (1Y to 4Y) in true (non-inverting) form from the selected inputs. The "257" is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.
The outputs are forced to a high impedance OFF-state when $\overline{OE}$ is HIGH.

The logic equations for the outputs are:

$1Y = \overline{OE} \cdot (1I_1 \cdot S + 1I_0 \cdot \overline{S})$
$2Y = \overline{OE} \cdot (2I_1 \cdot S + 2I_0 \cdot \overline{S})$
$3Y = \overline{OE} \cdot (3I_1 \cdot S + 3I_0 \cdot \overline{S})$
$4Y = \overline{OE} \cdot (4I_1 \cdot S + 4I_0 \cdot \overline{S})$

The "257" is identical to the "258" but has non-inverting (true) outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nI_0, nI_1 to nY S to nY	C_L = 50 pF V_{CC} = 3.3 V	4.0 4.5	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	30	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC257D	16	SO	plastic	SOT109-1
74LVC257DB	16	SSOP	plastic	SOT338-1
74LVC257PW	16	TSSOP	plastic	SOT403-1

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	S	common data select input
2, 5, 11, 14	$1I_0$ to $4I_0$	data inputs from source 0
3, 6, 10, 13	$1I_1$ to $4I_1$	data inputs from source 1
4, 7, 9, 12	1Y to 4Y	3-state multiplexer outputs
8	GND	ground (0 V)
15	$\overline{OE}$	3-state output enable input (active LOW)
16	V_{CC}	positive supply voltage

Fig.1 Pin configuration.

Fig.2 Logic symbol.

Fig.3 IEC Logic symbol.

Fig.4 Functional diagram.
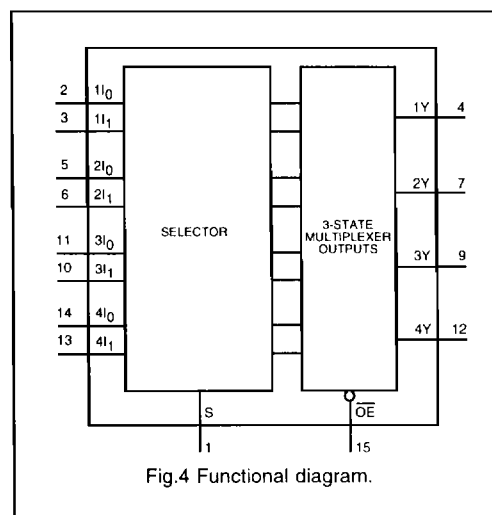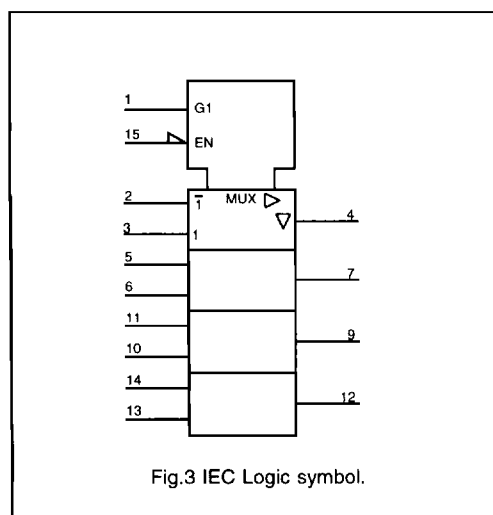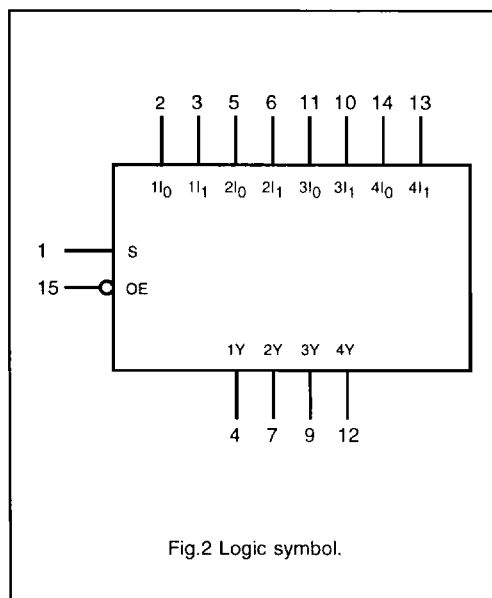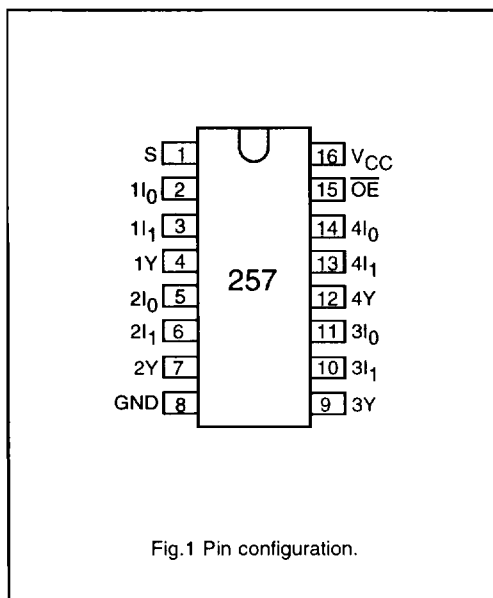
FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	S	nI_0	nI_1	nY
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = high impedance OFF-state
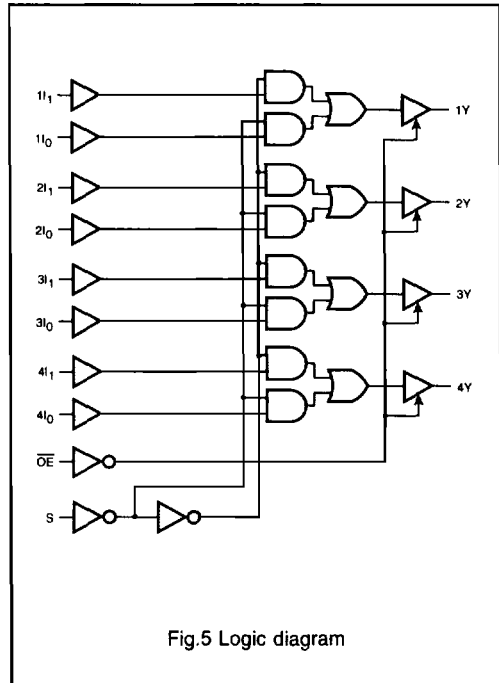
Fig.5 Logic diagram

DC CHARACTERISTICS FOR 74LVC257

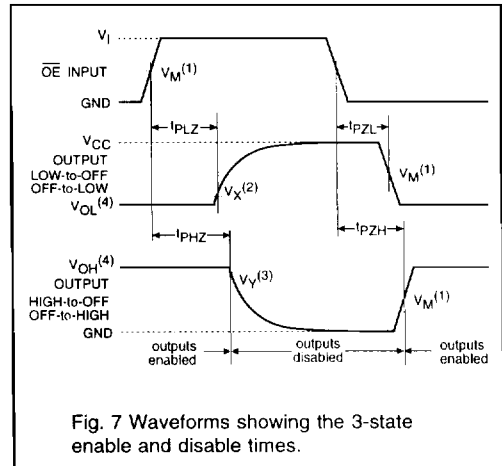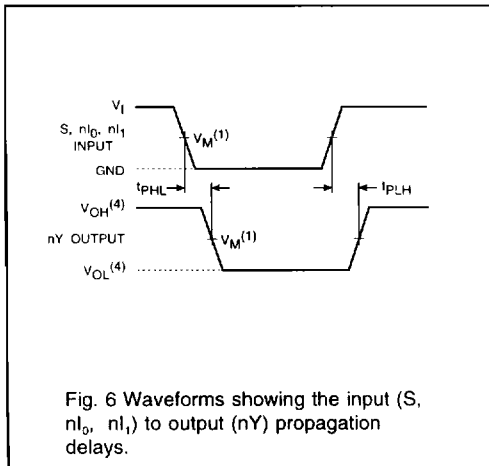For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74LVC257

GND = 0 V; $t_r = t_f \leq 2.5$ ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) –40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay nI_0 to nY; nI_1 to nY	– – –	– 4.8 4.0*	– 8.0 7.0	ns	1.2 2.7 3.0 to 3.6	Figs 6, 8
t_{PHL}/t_{PLH}	propagation delay S to nY	– – –	– 5.2 4.5*	– 9.0 8.0	ns	1.2 2.7 3.0 to 3.6	Figs 6, 8
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to nY	– – –	– 5.2 4.5*	– 9.0 8.0	ns	1.2 2.7 3.0 to 3.6	Figs 7, 8
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to nY	– – –	– 4.0 3.8*	– 6.5 6.0	ns	1.2 2.7 3.0 to 3.6	Figs 7, 8

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

Fig. 6 Waveforms showing the input (S, nI_0, nI_1) to output (nY) propagation delays.

Fig. 7 Waveforms showing the 3-state enable and disable times.

Notes:
(1) $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
  $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
(2) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
  $V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
(3) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
  $V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
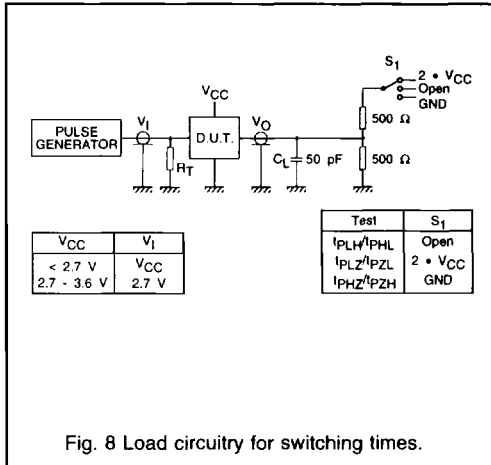(4) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

Fig. 8 Load circuitry for switching times.

V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \cdot V_{CC}$
t_{PHZ}/t_{PZH}	GND