HARRIS

# HI-307/883

January 1989

## Dual SPDT CMOS Analog Switch

### Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Analog Signal Range (±15V Supplies) ..... ±15V**
- **Low Leakage (+25°C) ..... 1nA (Max)**
- **Low Leakage (+125°C) ..... 100nA (Max)**
- **Low ON Resistance ..... 50Ω (Max)**
- **Charge Injection ..... 30pC (Typ)**
- **CMOS Compatible**
- **Symmetrical Switch Elements**
- **Low Operating Power**
- **Compatible with DG307**

### Applications

- **Sample and Hold, i.e. Low Leakage Switching**
- **Op Amp Gain Switching, i.e. Low ON Resistance**
- **Portable, Battery Operated Circuits**
- **Low Level Switching Circuits**
- **Dual or Single Supply Systems**

### Description

The HI-307/883 switch is a monolithic device fabricated using CMOS technology and the Harris Dielectric Isolation process. This switch features break-before-make switching, low and nearly constant ON resistance over the full analog signal range, and low power dissipation.

The HI-307/883 is CMOS compatible and has a logic "0" condition with an input less than 3.5V and a logic "1" condition with an input greater than 11V.

The HI-307/883 is pin-for-pin compatible with the industry standard Siliconix DG307. The device is available in a 14 pin Ceramic DIP. The HI-307/883 operates over the -55°C to +125°C temperature range.

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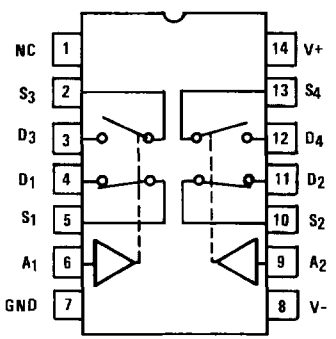
CMOS ANALOG SWITCHES

### Pinout

**HI1-307/883 (CERAMIC DIP)**
TOP VIEW




| LOGIC | SW 1<br>SW 2 | SW 3<br>SW 4 |
|---|---|---|
| 0 | OFF | ON |
| 1 | ON | OFF |

## Absolute Maximum Ratings

Voltage Between V+ and V- Terminals ..... 44V
±$V_{SUPPLY}$ to Ground (V+, V-) ..... ±22V
Analog Input Voltage +$V_S$ ..... +$V_{SUPPLY}$ +1.5V
-$V_S$ ..... -$V_{SUPPLY}$ -1.5V
Digital Input Voltage +$V_A$ ..... +$V_{SUPPLY}$ +4V
-$V_A$ ..... -$V_{SUPPLY}$ -4V
Peak Current (S or D)
(Pulse at 1ms, 10% Duty Cycle Max) ..... 40mA
Continuous Current ..... 30mA
Junction Temperature ..... +175°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... ≤275°C

## Thermal Information

| Thermal Resistance | $\theta_{ja}$ | $\theta_{jc}$ |
|---|---|---|
| Ceramic DIP Package | 88°C/W | 24°C/W |

Package Power Dissipation at +75°C
Ceramic DIP Package ..... 0.85W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package ..... 11.36mW/°C

*CAUTION: Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.*

## Recommended Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Supply Voltage (±$V_{SUPPLY}$) ..... ±15V
Analog Input Voltage ($V_S$) ..... ±$V_{SUPPLY}$
Logic Low Level ($V_{AL}$) ..... 0V to 3.5V
Logic High Level ($V_{AH}$) ..... 11V to +$V_{SUPPLY}$

**TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS**

Device Tested at: +$V_{SUPPLY}$ = +15V, -$V_{SUPPLY}$ = -15V, GND = 0V, Unless Otherwise Specified

| D.C. PARAMETERS | SYMBOL | CONDITIONS | GROUP A SUBGROUPS | TEMPERATURE | LIMITS MIN | LIMITS MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Switch "ON" Resistance | $R_{DS}$ | $V_{A1}$ = 11V, $V_D$ = 10V, $I_S$ = -10mA<br>$V_{A2}$ = 3.5V S1/S2/S3/S4 | 1 | +25°C | - | 50 | Ω |
| | | | 2, 3 | -55°C to +125°C | - | 75 | Ω |
| | | $V_{A1}$ = 11V, $V_D$ = -10V, $I_S$ = 10mA<br>$V_{A2}$ = 3.5V S1/S2/S3/S4 | 1 | +25°C | - | 50 | Ω |
| | | | 2, 3 | -55°C to +125°C | - | 75 | Ω |
| Source "OFF" Leakage Current | $I_{S(OFF)}$ | $V_S$ = +14V, $V_D$ = -14V, $V_{A1}$ = 3.5V<br>$V_{A2}$ = 11V S1/S2/S3/S4 | 1 | +25°C | -1 | 1 | nA |
| | | | 2, 3 | -55°C to +125°C | -100 | 100 | nA |
| | | $V_S$ = -14V, $V_D$ = +14V, $V_{A1}$ = 3.5V<br>$V_{A2}$ = 11V S1/S2/S3/S4 | 1 | +25°C | -1 | 1 | nA |
| | | | 2, 3 | -55°C to +125°C | -100 | 100 | nA |
| Drain "OFF" Leakage Current | $I_{D(OFF)}$ | $V_S$ = -14V, $V_D$ = +14V, $V_{A1}$ = 3.5V<br>$V_{A2}$ = 11V S1/S2/S3/S4 | 1 | +25°C | -1 | 1 | nA |
| | | | 2, 3 | -55°C to +125°C | -100 | 100 | nA |
| | | $V_S$ = +14V, $V_D$ = -14V, $V_{A1}$ = 3.5V<br>$V_{A2}$ = 11V S1/S2/S3/S4 | 1 | +25°C | -1 | 1 | nA |
| | | | 2, 3 | -55°C to +125°C | -100 | 100 | nA |
| Channel "ON" Leakage Current | $I_{D(ON)}$ | $V_D$ = $V_S$ = +14V, $V_{A1}$ = 11V<br>$V_{A2}$ = 3.5V S1/S2/S3/S4 | 1 | +25°C | -1 | 1 | nA |
| | | | 2, 3 | -55°C to +125°C | -100 | 100 | nA |
| | | $V_D$ = $V_S$ = -14V, $V_{A1}$ = 11V<br>$V_{A2}$ = 3.5V S1/S2/S3/S4 | 1 | +25°C | -1 | 1 | nA |
| | | | 2, 3 | -55°C to +125°C | -100 | 100 | nA |
| Low Level Input Current | $I_{AL}$ | All Channels $V_{AL}$ = 3.5V | 1 | +25°C | -1.0 | 1.0 | µA |
| | | | 2, 3 | -55°C to +125°C | -1.0 | 1.0 | µA |
| High Level Input Current | $I_{AH}$ | All Channels $V_{AH}$ = 11V | 1 | +25°C | -1.0 | 1.0 | µA |
| | | | 2, 3 | -55°C to +125°C | -1.0 | 1.0 | µA |
| Supply Current | $+I_{CC}$ | All Channels $V_A$ = 0V | 1 | +25°C | - | 10 | µA |
| | | | 2, 3 | -55°C to +125°C | - | 100 | µA |
| | | All Channels $V_A$ = 15V | 1 | +25°C | - | 10 | µA |
| | | | 2, 3 | -55°C to +125°C | - | 100 | µA |
| Supply Current | $-I_{CC}$ | All Channels $V_A$ = 0V | 1 | +25°C | -10 | - | µA |
| | | | 2, 3 | -55°C to +125°C | -100 | - | µA |
| | | All Channels $V_A$ = 15V | 1 | +25°C | -10 | - | µA |
| | | | 2, 3 | -55°C to +125°C | -100 | - | µA |

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

**TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS**

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, GND = 0V, Unless Otherwise Specified

| PARAMETERS | SYMBOL | CONDITIONS | GROUP A SUBGROUPS | TEMPERATURE | LIMITS MIN | LIMITS MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Turn "ON" Time | $t_{(ON)}$ | $C_L$ = 33pF, $R_L$ = 300Ω | 9 | +25°C | - | 250 | ns |
| | | | 10, 11 | -55°C, +125°C | - | 500 | ns |
| Turn "OFF" Time | $t_{(OFF)}$ | $C_L$ = 33pF, $R_L$ = 300Ω | 9 | +25°C | - | 150 | ns |
| | | | 10, 11 | -55°C, +125°C | - | 450 | ns |

**TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS** (NOTE 1)

Device Characterized at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, GND = 0V, Unless Otherwise Specified

| PARAMETERS | SYMBOL | CONDITIONS | NOTE | TEMPERATURE | LIMITS MIN | LIMITS MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Switch Input Capacitance | $C_{IS(OFF)}$ | Measured Source to GND | 1 | +25°C | - | 28 | pF |
| Driver Input Capacitance | $C_{C1}$ | $V_A$ = 0V | 1 | +25°C | - | 10 | pF |
| | $C_{C2}$ | $V_A$ = 15V | 1 | +25°C | - | 10 | pF |
| Switch Output Capacitance | $C_{OS}$ | Measured Drain to GND | 1 | +25°C | - | 28 | pF |
| Off Isolation | $V_{ISO}$ | f = 1MHz, $V_{GEN}$ = $1V_{p-p}$ | 1 | +25°C | 40 | - | dB |
| Crosstalk | $V_{CT}$ | f = 1MHz, $V_{GEN}$ = $1V_{p-p}$ | 1 | +25°C | 40 | - | dB |
| Charge Transfer | $V_{CTE}$ | $V_S$ = GND, $C_L$ = 0.01µF | 1 | +25°C | - | 15 | mV |

NOTE 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

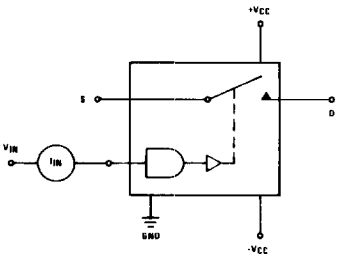
**TABLE 4. ELECTRICAL TEST REQUIREMENTS**

| MIL-STD-883 TEST REQUIREMENTS | SUBGROUPS (SEE TABLES 1 & 2) |
|---|---|
| Interim Electrical Parameters (Pre Burn-in) | 1 |
| Final Electrical Test Parameters | 1*, 2, 3, 9, 10, 11 |
| Group A Test Requirements | 1, 2, 3, 9, 10, 11 |
| Groups C & D Endpoints | 1 |

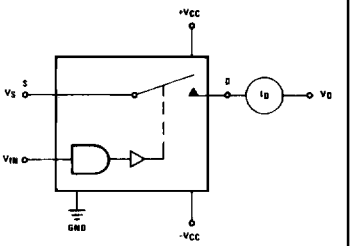
* PDA applies to Subgroup 1 only.

## Test Circuits

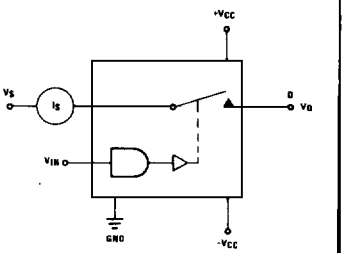
### INPUT LEAKAGE CURRENT



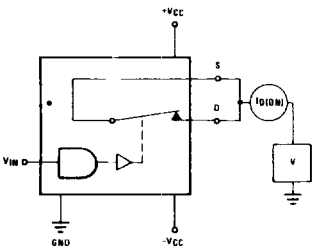

### $I_{D(OFF)}$



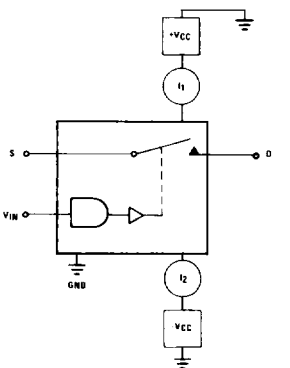

### $I_{S(OFF)}$



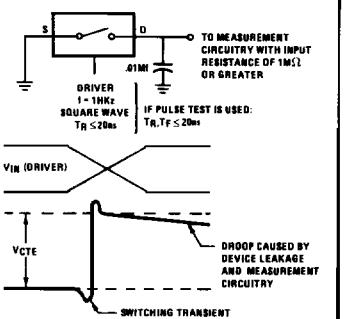

### $I_{D(ON)}$




### SUPPLY CURRENTS

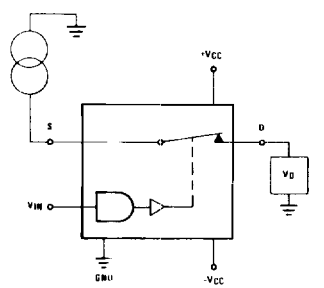



### CHARGE TRANSFER ERROR

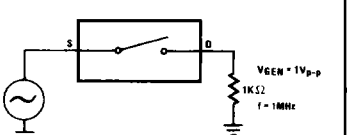



NOTE: $V_{CTE}$ may be a positive or negative value

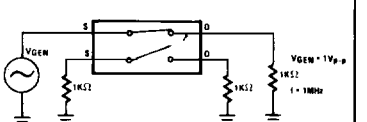
### $R_{DS}$




### OFF CHANNEL ISOLATION

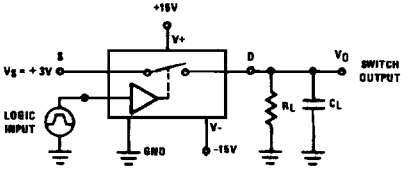


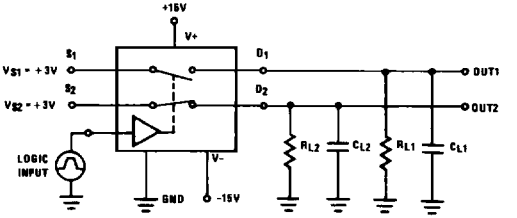

### CROSSTALK BETWEEN CHANNELS

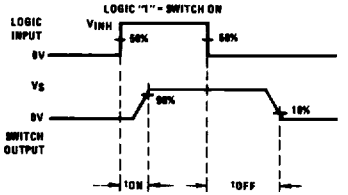


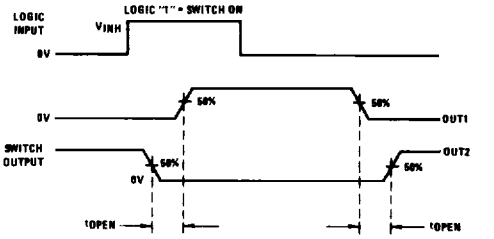

For Detail Information Refer to HI-307/883 Test Tech Brief

## Test Waveforms



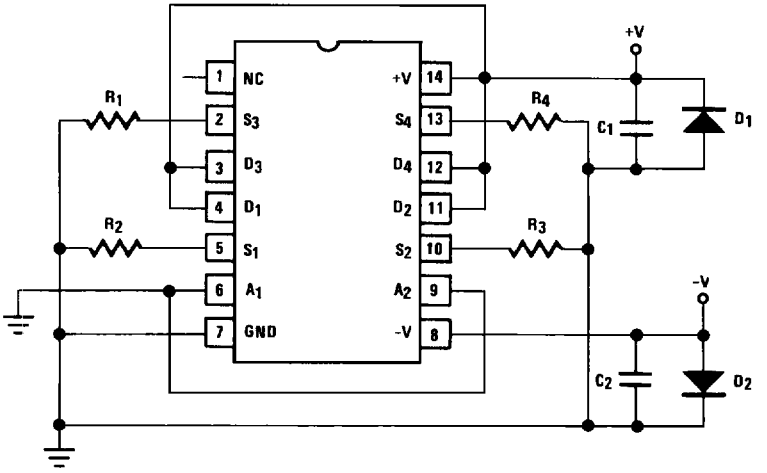




NOTES:

1. $R_L = R_L1 = R_L2 = 300\Omega$; $C_L = C_L1 = C_L2 = 33pF$
2. $V_{INH} = 15V$
   RISETIME (1.5V to 13.5V) $\leq$ 20ns
   FALLTIME (13.5V to 1.5V) $\leq$ 20ns

## Burn-In Circuit

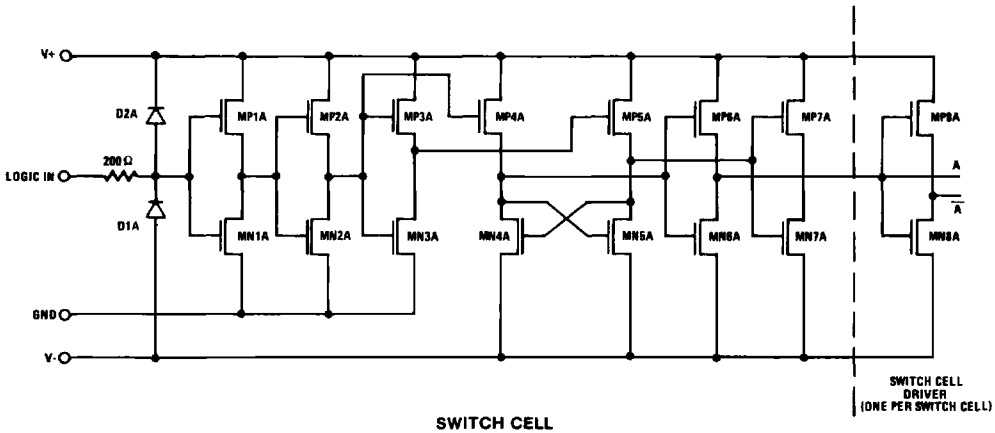
HI-307/883 CERAMIC DIP



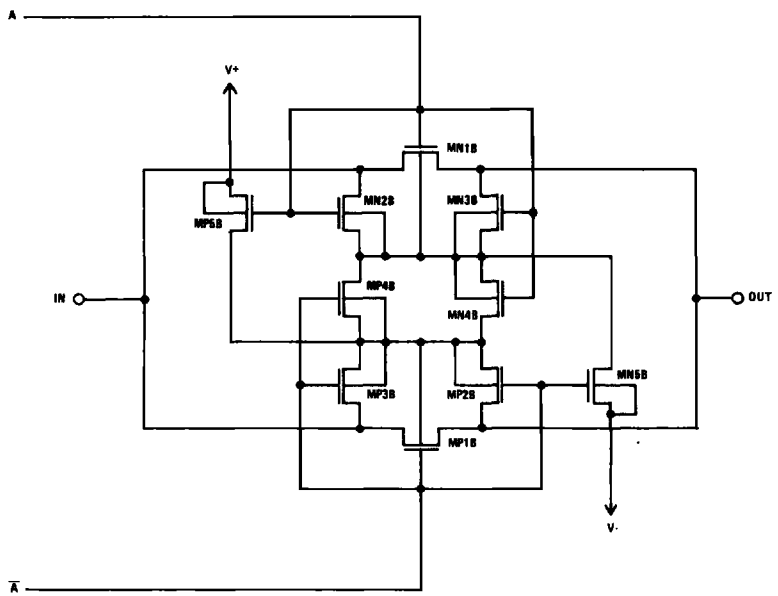

NOTES:
$R_1 = R_2 = R_3 = R_4 = 10K\Omega$, 5%, 1/4 or 1/2 watt
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
$D_1 = D_2$ = IN4002 (per board)
$|(V+) - (V-)| = 30V$

## Schematic Diagram

DIGITAL INPUT BUFFER AND LEVEL SHIFTER




SWITCH CELL



## Die Characteristics

**DIE DIMENSIONS:**
76 x 83.9 x 19 mils

**METALLIZATION:**
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

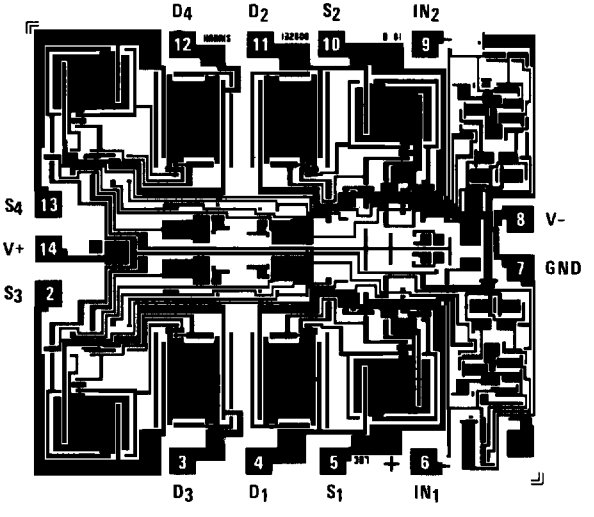
**GLASSIVATION:**
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

**DIE ATTACH:**
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)

**WORST CASE CURRENT DENSITY:**
$3.9 \times 10^5 A/cm^2$ at 30mA
This device meets Glassivation Integrity Test requirement per Mil-Std-883 Method 2021 and Mil-M-38510 paragraph 3.5.5.4.

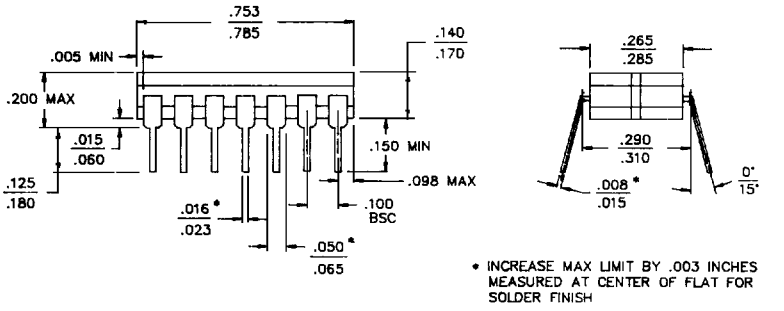
## Metallization Mask Layout

HI-307/883



## Packaging†

**14 PIN CERAMIC DIP**




**LEAD MATERIAL:** Type B
**LEAD FINISH:** Type A
**PACKAGE MATERIAL:** Ceramic, 90% Alumina
**PACKAGE SEAL:**
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

**INTERNAL LEAD WIRE:**
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
**COMPLIANT OUTLINE:** 38510 D-1



NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

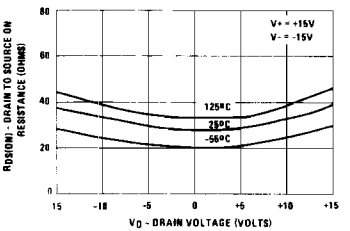
# HI-307

## Dual SPDT CMOS Analog Switch

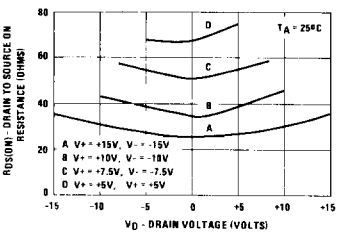
*The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.*

### *Typical Performance Characteristics* Unless Otherwise Specified: V+ = +15V, V- = -15V, $T_A$ = +25°C

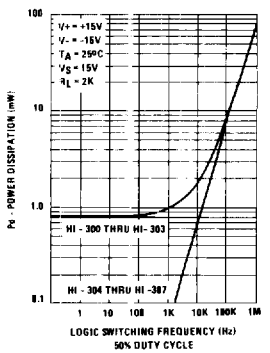
**$R_{DS(ON)}$ vs. $V_D$ AND TEMPERATURE**



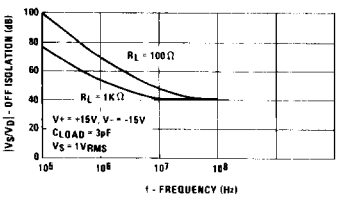

**$R_{DS(ON)}$ vs. $V_D$ AND POWER SUPPLY VOLTAGE**



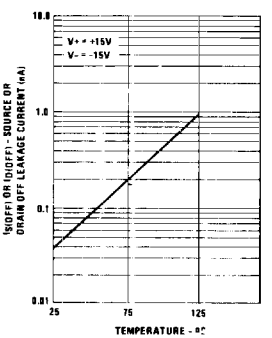

**DEVICE POWER DISSIPATION vs. SWITCHING FREQUENCY SIGNAL LOGIC INPUT**



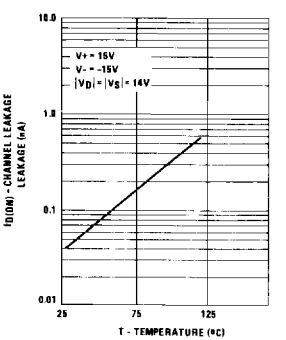

**OFF ISOLATION vs. FREQUENCY**




**$I_{S(OFF)}$ or $I_{D(OFF)}$ vs. TEMPERATURE***




**$I_{D(ON)}$ vs. TEMPERATURE***




* The net leakage into the source or drain is the N-channel leakage minus the P-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

# DESIGN INFORMATION (Continued)

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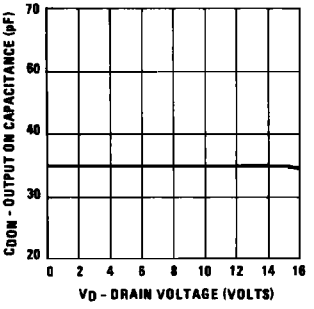
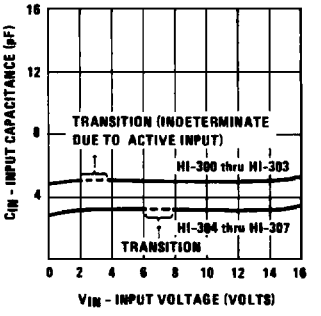
## *Typical Performance Characteristics* Unless Otherwise Specified: V+ = +15V, V- = -15V, $T_A$ = +25°C

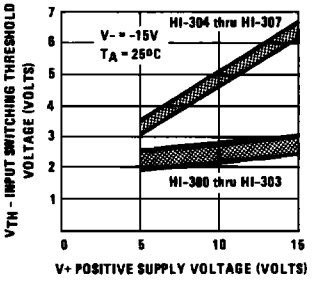
**OUTPUT ON CAPACITANCE vs. DRAIN VOLTAGE**



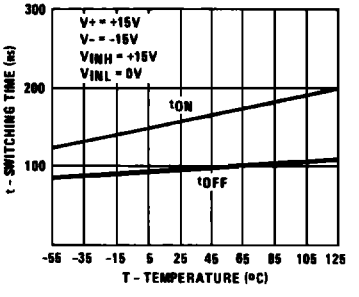

**DIGITAL INPUT CAPACITANCE vs. INPUT VOLTAGE**



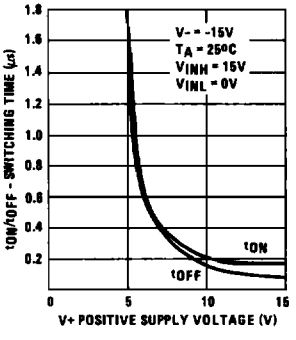

**INPUT SWITCHING THRESHOLD vs. POSITIVE SUPPLY VOLTAGE**




**SWITCHING TIME vs. TEMPERATURE**




**SWITCHING TIME vs. POSITIVE SUPPLY VOLTAGE**




**SWITCHING TIME vs. NEGATIVE SUPPLY VOLTAGE**