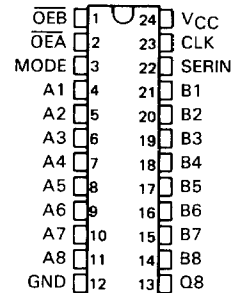


SN54AS856, SN74AS856 8-BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS

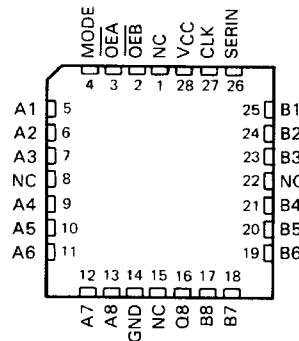
D2814, DECEMBER 1983—REVISED MARCH 1985

- Included Among the Package Options are Compact, 24-Pin, 300-mil-Wide DIPs and Both 28-Pin Plastic and Ceramic Chip Carriers
- Buffered 3-State Outputs Drive Bus Lines Directly
- Cascadable to n-Bits
- Eight Selectable Transceiver/Port Functions:
 - B to A
 - Register to A and/or B
 - Off-Line Shifts (A and B Ports in High-Impedance State)
 - Shifted to A and/or B
- Particularly Suitable for Use in Diagnostics Analysis Circuitry
- Serial Register Provides:
 - Parallel Storage of Either A or B Input Data
 - Serial Transmission of Data from Either A or B Port
 - Readback Mode B to A
- Dependable Texas Instruments Quality and Reliability

SN54AS856 . . . JT PACKAGE
SN74AS856 . . . DW or NT PACKAGE
(TOP VIEW)



SN54AS856 . . . FK PACKAGE
SN74AS856 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

The 'AS856 features two 8-bit I/O ports (A1-A8 and B1-B8), an 8-bit parallel-load, serial-in, parallel-out shift register, and control logic. With these features, this device is capable of performing eight selectable transceiver or port functions, depending on the state of the three control lines \overline{OEA} , \overline{OEB} , and MODE. These functions include: transferring data from port A to port B or vice versa (i.e., the transceiver function), serial shifting data to either or both ports, and performing off-line shifts (with A and B ports active as transceivers in a high-impedance state). Synchronous parallel loading of the internal register can be accomplished from either port on the positive transition of the clock while serially shifting data in via the SERIN input. The 'AS856 is ideally suited for applications needing signature-analysis circuitry to enhance system verification and/or fault analysis. All serial data is shifted right. All outputs are buffer-type outputs designed specifically to drive bus lines directly and all are 3-state except for QB, which is a totem-pole output.

The SN54AS856 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AS856 is characterized for operation from 0°C to 70°C .

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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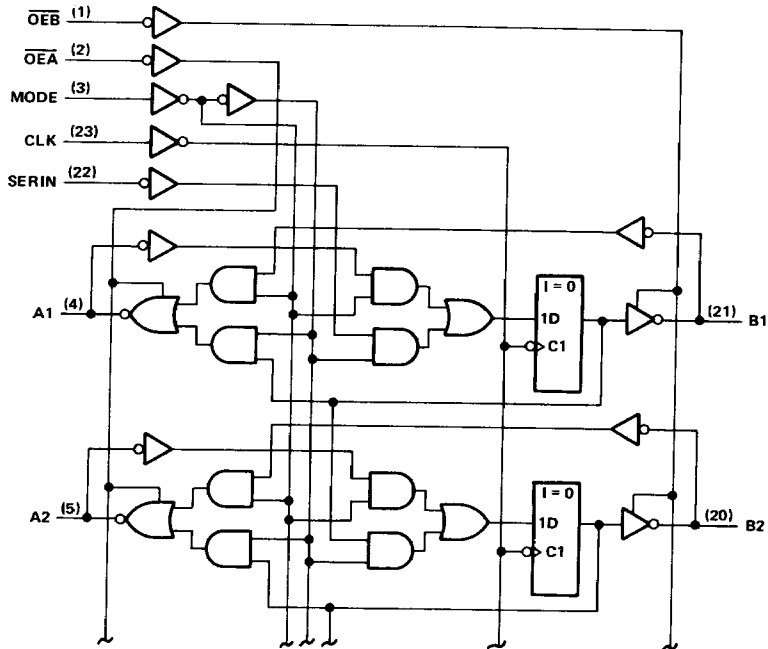
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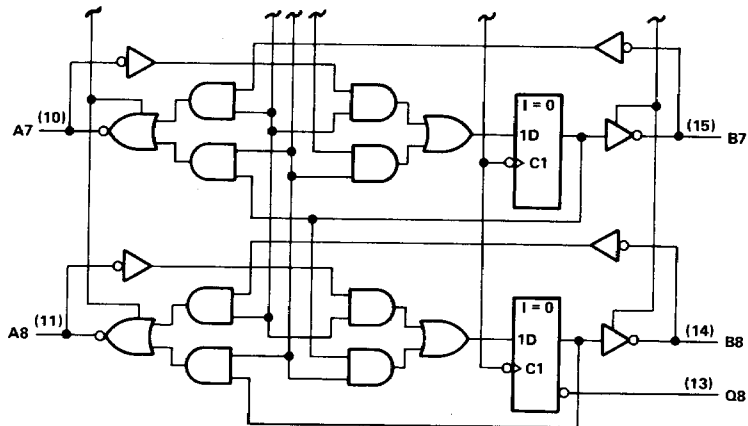
SN54AS856, SN74AS856 8-BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS

logic diagram (positive logic)



FOUR IDENTICAL CHANNELS NOT SHOWN
INPUTS/OUTPUTS NOT SHOWN:

- | | |
|--------|---------|
| (6) A3 | (19) B3 |
| (7) A4 | (18) B4 |
| (8) A5 | (17) B5 |
| (9) A6 | (16) B6 |



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LSI Devices

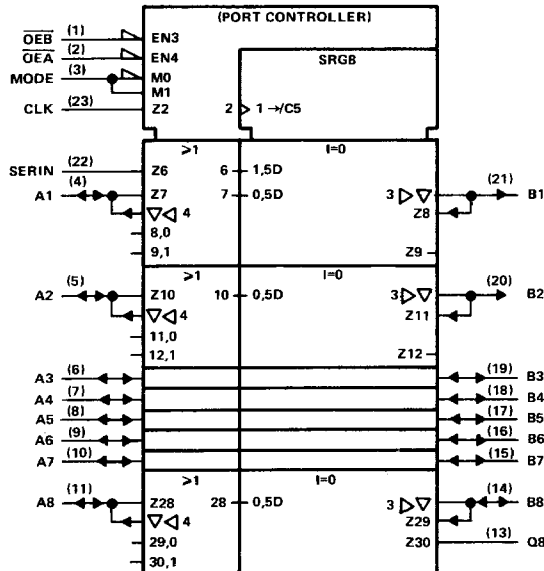
SN54AS856, SN74AS856 8-BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS

FUNCTION TABLE

MODE			CLOCK	SERIN	A1 Q1 B1		A2 Q2 B2		A3 Q3 B3		A4 Q4 B4		A5 Q5 B5		A6 Q6 B6		A7 Q7 B7		A8 Q8 B8		FUNCTION
MODE	OEA	OEB																			
L	L	L	H or L	X	Q1 Q1 Q1	Q2 Q2 Q2	Q3 Q3 Q3	Q4 Q4 Q4	Q5 Q5 Q5	Q6 Q6 Q6	Q7 Q7 Q7	Q8 Q8 Q8	FEEDBACK								
L	L	L	↑	X	Q1 Q1 Q1	Q2 Q2 Q2	Q3 Q3 Q3	Q4 Q4 Q4	Q5 Q5 Q5	Q6 Q6 Q6	Q7 Q7 Q7	Q8 Q8 Q8	FEEDBACK								
L	L	H	H or L	X	B1 Q1 Z	B2 Q2 Z	B3 Q3 Z	B4 Q4 Z	B5 Q5 Z	B6 Q6 Z	B7 Q7 Z	B8 Q8 Z	B to A								
L	L	H	↑	X	B1 B1 Z	B2 B2 Z	B3 B3 Z	B4 B4 Z	B5 B5 Z	B6 B6 Z	B7 B7 Z	B8 B8 Z	A to Q								
L	H	L	H or L	X	Z Q1 Q1	Z Q2 Q2	Z Q3 Q3	Z Q4 Q4	Z Q5 Q5	Z Q6 Q6	Z Q7 Q7	Z Q8 Q8	A to Q								
L	H	L	↑	X	Z A1 A1	Z A2 A2	Z A3 A3	Z A4 A4	Z A5 A5	Z A6 A6	Z A7 A7	Z A8 A8	Q to B								
L	H	H	H or L	X	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	Z Q8 Z	A to Q								
L	H	H	↑	X	Z A1 Z	Z A2 Z	Z A3 Z	Z A4 Z	Z A5 Z	Z A6 Z	Z A7 Z	Z A8 Z	A to Q								
H	L	L	H or L	X	Q1 Q _n Q1	Q2 Q _n Q2	Q3 Q _n Q3	Q4 Q _n Q4	Q5 Q _n Q5	Q6 Q _n Q6	Q7 Q _n Q7	Q8 Q _n Q8	SHIFT TO A and B								
H	L	L	↑	H	H H H	Q1 Q1 Q1	Q2 Q2 Q2	Q3 Q3 Q3	Q4 Q4 Q4	Q5 Q5 Q5	Q6 Q6 Q6	Q7 Q7 Q7	TO A								
H	L	L	↑	L	L L L	Q1 Q1 Q1	Q2 Q2 Q2	Q3 Q3 Q3	Q4 Q4 Q4	Q5 Q5 Q5	Q6 Q6 Q6	Q7 Q7 Q7	TO B								
H	L	H	H or L	X	Q1 Q _n Z	Q2 Q _n Z	Q3 Q _n Z	Q4 Q _n Z	Q5 Q _n Z	Q6 Q _n Z	Q7 Q _n Z	Q8 Q _n Z	SHIFT TO A								
H	L	H	↑	H	H H Z	Q1 Q1 Z	Q2 Q2 Z	Q3 Q3 Z	Q4 Q4 Z	Q5 Q5 Z	Q6 Q6 Z	Q7 Q7 Z	TO A								
H	L	H	↑	L	L L Z	Q1 Q1 Z	Q2 Q2 Z	Q3 Q3 Z	Q4 Q4 Z	Q5 Q5 Z	Q6 Q6 Z	Q7 Q7 Z	TO B								
H	H	L	H or L	X	Z Q _n Q1	Z Q _n Q2	Z Q _n Q3	Z Q _n Q4	Z Q _n Q5	Z Q _n Q6	Z Q _n Q7	Z Q _n Q8	SHIFT TO B								
H	H	L	↑	H	Z H H	Z Q1 Q1	Z Q2 Q2	Z Q3 Q3	Z Q4 Q4	Z Q5 Q5	Z Q6 Q6	Z Q7 Q7	TO B								
H	H	L	↑	L	Z L L	Z Q1 Q1	Z Q2 Q2	Z Q3 Q3	Z Q4 Q4	Z Q5 Q5	Z Q6 Q6	Z Q7 Q7	TO B								
H	H	H	H or L	X	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	SHIFT								
H	H	H	↑	H	Z H Z	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	SHIFT								
H	H	H	↑	L	Z L H	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	SHIFT								

n = level of Q_n (n = 1, 2, . . . 8) established on most recent ↑ transition of CLK. Q1 through Q8 are the shift register outputs; only Q8 is available externally. The double inversions that take place as data travels from port to port are ignored in this table.

logic symbol †



Pin numbers shown are for DW, JT, and NT packages.

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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SN54AS856, SN74AS856

8-BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS

absolute maximum ratings over free-air temperature range

Supply voltage, V_{CC}	7 V
Input voltage: All inputs	7 V
I/O ports	5.5 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range: SN54AS856	-55°C to 125°C
SN74AS856	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54AS856			SN74AS856			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current	A1-A8, B1-B8		-12			-15	mA
		Q8		-2			-2	
I_{OL}	Low-level output current	A1-A8, B1-B8		32			48	mA
		Q8		20			20	
f_{clock}	Clock frequency	0		45	0		50	MHz
t_w	Duration of clock pulse		11			10		ns
t_{su}	Setup time before CLK↑	A1-A8, B1-B8 SERIN		5.5			5.5	ns
		OEB, OEA, MODE		5.5			5.5	
t_h	Hold-time, data after CLK↑	A1-A8, B1-B8 SERIN		0			0	ns
		OEB, OEA, MODE		0			0	
T_A	Operating free-air temperature	-55		125	0		70	°C

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LSI Devices

SN54AS856, SN74AS856 8-BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS

electrical characteristics over recommended operating free-air temperature range
(unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS856			SN74AS856			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2			-1.2	V
V _{OH}	A1-A8	V _{CC} = 4.5 V, I _{OH} = -12 mA	2	3.2				V
	B1-B8	V _{CC} = 4.5 V, I _{OH} = -15 mA			2	3.3		
	All outputs	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -2 mA	V _{CC} -2		V _{CC} -2			
V _{OL}	All outputs except Q8	V _{CC} = 4.5 V, I _{OL} = 32 mA	0.25	0.5				V
		V _{CC} = 4.5 V, I _{OL} = 48 mA			0.35	0.5		
	Q8	V _{CC} = 4.5 V, I _{OL} = 20 mA					0.5	
I _I	\overline{OEB} , \overline{OEA} , MODE	V _{CC} = 5.5 V, V _I = 7 V		0.2		0.2		mA
	CLK and SERIN			0.1		0.1		
	A1-A8, B1-B8	V _{CC} = 5.5 V, V _I = 5.5 V		0.2		0.2		
I _{IH}	\overline{OEB} , \overline{OEA} , MODE	V _{CC} = 5.5 V, V _I = 2.7 V		40		40		μA
	CLK and SERIN			20		20		
	A1-A8, B1-B8‡			70		70		
I _{IL}	\overline{OEB} , \overline{OEA} , MODE	V _{CC} = 5.5 V, V _I = 0.4 V		-1		-1		mA
	CLK and SERIN			-0.5		-0.5		
	A1-A8, B1-B8‡			-0.5		-0.5		
I _O §	Except Q8	V _{CC} = 5.5 V, V _O = 2.25 V	-30	-112	-30	-112		mA
	Q8		-20	-112	-20	-112		
I _{CC}	V _{CC} = 5.5 V		118	200	118	200		mA

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the output currents I_{OZH} and I_{OZL}, respectively.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OCS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX				UNIT
			SN54AS856		SN74AS856		
			MIN	MAX	MIN	MAX	
f _{max}			45		50	MHz	
t _{PLH}	Any B port	Any A port	2	8	2	7	ns
t _{PHL}			2	10.5	2	9.5	
t _{PLH}	↑MODE†	Any A or B port	2	8.5	2	7.5	ns
t _{PHL}			5	20	5	19	
t _{PLH}	↓MODE	Any A or B port	2	8.5	2	7.5	ns
t _{PHL}			2	9.5	2	8	
t _{PLH}	CLK	Any A or B port	3	12	3	9	ns
t _{PHL}			3	12	3	11	
t _{PLH}	CLK	Q8	2	9	2	7.5	ns
t _{PHL}			2	10	2	9	
t _{PHZ}	\overline{OEA} or \overline{OEB}	Any A or B port	2	9	2	7	ns
t _{PLZ}			2	12	2	9.5	
t _{PZH}			2	8	2	7	
t _{PZL}			2	11	2	10	

† The positive transition of the MODE control will cause low-level data at the A output Bus or stored in Q to be invalid for 12 ns.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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