AS7C33512FT32A
AS7C33512FT36A

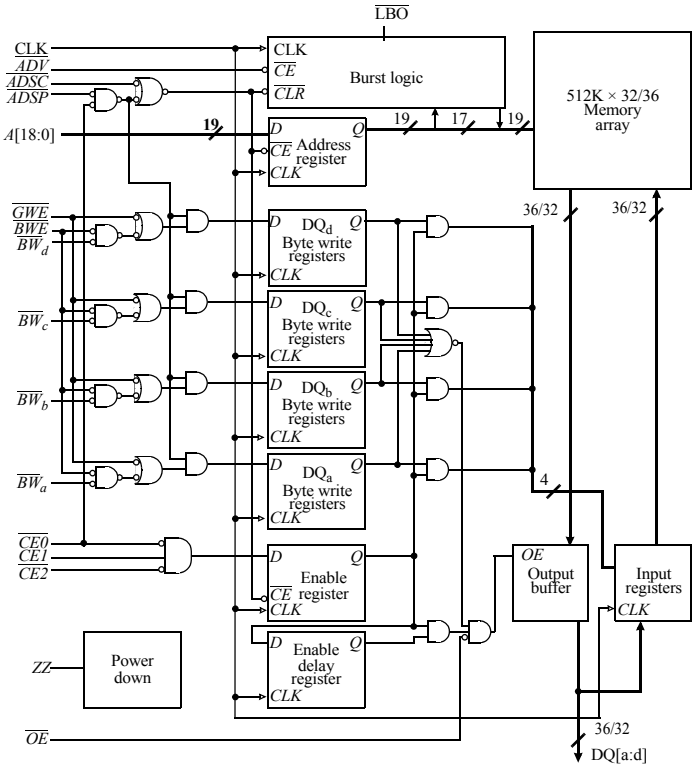
3.3V 512K × 32/36 Flow-through synchronous SRAM

Features

- Organization: 524,288 words × 32 or 36 bits
- Fast clock to data access: 8.5/10 ns
- Fast $\overline{OE}$ access time: 3.4/3.8 ns
- Fully synchronous flow-through operation
- Asynchronous output enable control
- Available in 100-pin TQFP package and 165-ball BGA
- Individual byte write and global write
- Multiple chip enables for easy expansion
- 3.3V core power supply
- 2.5V or 3.3V I/O operation with separate V_{DDQ}
- Linear or interleaved burst control
- Snooze mode for reduced power-standby
- Common data inputs and data outputs
- Boundary scan using IEEE 1149.1 JTAG function
- NTD™[1] pipelined architecture available (AS7C331MNTD18A, AS7C33512NTD32A/ AS7C33512NTD36A)

1 NTD™ is a trademark of Alliance Semiconductor Corporation. All trademarks mentioned in this document are the property of their respective owners.

Logic block diagram

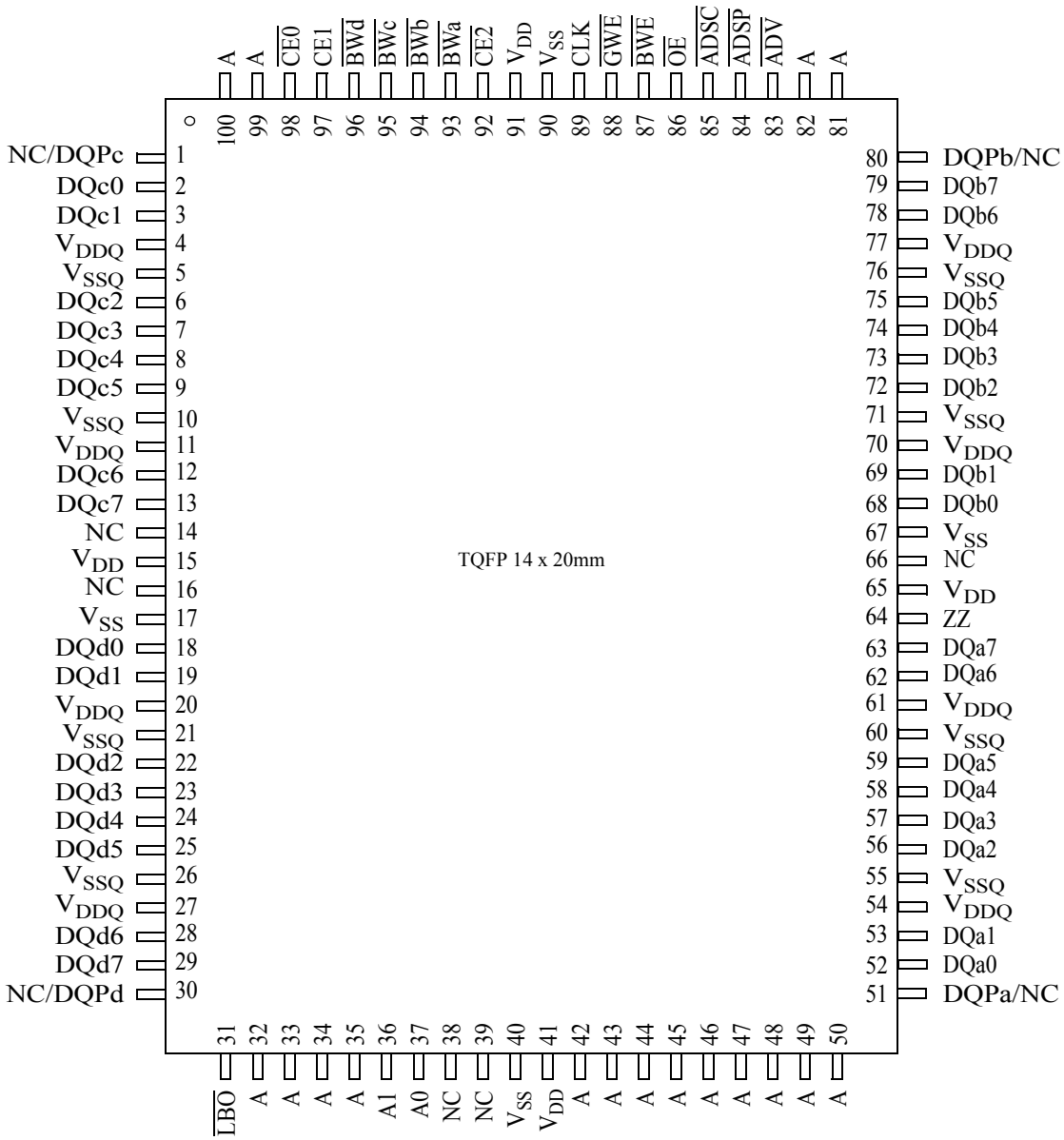


Selection guide

	-85	-10	Units
Minimum cycle time	10	12	ns
Maximum clock access time	8.5	10	
Maximum operating current	250	230	ns
Maximum standby current	85	75	mA
Maximum CMOS standby current (DC)	40	40	mA

Pin and ball assignment

100-pin TQFP - top view



Note: For pins 1, 30, 51, and 80, NC applies to the x32 configuration. DQPn applies to the x36

Ball assignment for 165-ball BGA for 512K x 36

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CE0}$	$\overline{BWc}$	$\overline{BWb}$	$\overline{CE2}$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	NC
B	NC	A	CE1	$\overline{BWd}$	$\overline{BWa}$	CLK	$\overline{GWE}$	$\overline{OE}$	$\overline{ADSP}$	A	NC
C	DQPc	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQPb
D	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
E	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
F	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
G	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQd	DQd	V_{DDQ}	V_{DD}	Vss	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
K	DQd	DQd	V_{DDQ}	V_{DD}	Vss	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
L	DQd	DQd	V_{DDQ}	V_{DD}	Vss	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
M	DQd	DQd	V_{DDQ}	V_{DD}	Vss	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
N	DQPd	NC	V_{DDQ}	V_{SS}	NC	A	NC	V_{SS}	V_{DDQ}	NC	DQPa
P	NC	NC	A	A	TDI	A1[1]	TDO	A	A	A	A
R	$\overline{LBO}$	NC	A	A	TMS	A0[1]	TCK	A	A	A	A

1 A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

Functional description

The AS7C33512FT32A/36A is a high-performance CMOS 16-Mbit synchronous Static Random Access Memory (SRAM) device organized as 524,288 words x 32/36.

Fast cycle times of 10/12 ns with clock access times (t_{CD}) of 8.5/10 ns. Three chip enable ($\overline{CE}$) inputs permit easy memory expansion. Burst operation is initiated in one of two ways: the controller address strobe ($\overline{ADSC}$), or the processor address strobe ($\overline{ADSP}$). The burst advance pin ($\overline{ADV}$) allows subsequent internally generated burst addresses.

Read cycles are initiated with $\overline{ADSP}$ (regardless of $\overline{WE}$ and $\overline{ADSC}$) using the new external address clocked into the on-chip address register when $\overline{ADSP}$ is sampled low, the chip enables are sampled active, and the output buffer is enabled with $\overline{OE}$. In a read operation, the data accessed by the current address registered in the address registers by the positive edge of CLK are carried to the data-out buffer. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on all subsequent clock edges. Address is incremented internally for the next access of the burst when $\overline{ADV}$ is sampled low and both address strobes are high. Burst mode is selectable with the $\overline{LBO}$ input. With $\overline{LBO}$ unconnected or driven high, burst operations use an interleaved count sequence. With $\overline{LBO}$ driven low, the device uses a linear count sequence.

Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting a write command. A global write enable $\overline{GWE}$ writes all 32/36 regardless of the state of individual $\overline{BW}$[a:d] inputs. Alternately, when $\overline{GWE}$ is high, one or more bytes may be written by asserting $\overline{BWE}$ and the appropriate individual byte $\overline{BWn}$ signals.

$\overline{BWn}$ is ignored on the clock edge that samples $\overline{ADSP}$ low, but it is sampled on all subsequent clock edges. Output buffers are disabled when $\overline{BWn}$ is sampled LOW regardless of $\overline{OE}$. Data is clocked into the data input register when $\overline{BWn}$ is sampled low. Address is incremented internally to the next burst address if $\overline{BWn}$ and $\overline{ADV}$ are sampled low.

Read or write cycles may also be initiated with $\overline{ADSC}$ instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ follow.

- $\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
- $\overline{WE}$ signals are sampled on the clock edge that samples $\overline{ADSC}$ low (and $\overline{ADSP}$ high).
- Master chip enable $\overline{CE0}$ blocks $\overline{ADSP}$, but not $\overline{ADSC}$.

The AS7C33512FT32A and AS7C33512FT36A family operates from a core 3.3V power supply. I/Os use a separate power supply that can operate at 2.5V or 3.3V. These devices are available in a 100-pin TQFP and 165-ball BGA.

TQFP and BGA capacitance

Parameter	Symbol	Test conditions	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	-	5	pF
I/O capacitance	$C_{I/O}$	V_{OUT} = 0V	-	7	pF

TQFP and BGA thermal resistance

Description	Conditions		Symbol	Typical	Units
Thermal resistance (junction to ambient)[1]	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	1–layer	θ_{JA}	40	°C/W
		4–layer	θ_{JA}	22	°C/W
Thermal resistance (junction to top of case)[1]			θ_{JC}	8	°C/W

1 This parameter is sampled

Signal descriptions

Pin	I/O	Properties	Description
CLK	I	CLOCK	Clock. All inputs except $\overline{OE}$, ZZ, and $\overline{LBO}$ are synchronous to this clock.
A,A0,A1	I	SYNC	Address. Sampled when all chip enables are active and when $\overline{ADSC}$ or $\overline{ADSP}$ are asserted.
DQ[a,b,c,d]	I/O	SYNC	Data. Driven as output when the chip is enabled and when $\overline{OE}$ is active.
$\overline{CE0}$	I	SYNC	Master chip enable. Sampled on clock edges when $\overline{ADSP}$ or $\overline{ADSC}$ is active. When $\overline{CE0}$ is inactive, $\overline{ADSP}$ is blocked. Refer to the "Synchronous truth table" for more information.
CE1, $\overline{CE2}$	I	SYNC	Synchronous chip enables, active high, and active low, respectively. Sampled on clock edges when $\overline{ADSC}$ is active or when $\overline{CE0}$ and $\overline{ADSP}$ are active.
$\overline{ADSP}$	I	SYNC	Address strobe processor. Asserted low to load a new address or to enter standby mode.
$\overline{ADSC}$	I	SYNC	Address strobe controller. Asserted low to load a new address or to enter standby mode.
$\overline{ADV}$	I	SYNC	Advance. Asserted low to continue burst read/write.
$\overline{GWE}$	I	SYNC	Global write enable. Asserted low to write all 32/36 and 18 bits. When high, $\overline{BWE}$ and $\overline{BW[a:d]}$ control write enable.
$\overline{BWE}$	I	SYNC	Byte write enable. Asserted low with $\overline{GWE}$ high to enable effect of $\overline{BW[a:d]}$ inputs.
$\overline{BW[a,b,c,d]}$	I	SYNC	Write enables. Used to control write of individual bytes when $\overline{GWE}$ is high and $\overline{BWE}$ is low. If any of $\overline{BW[a:d]}$ is active with $\overline{GWE}$ high and $\overline{BWE}$ low, the cycle is a write cycle. If all $\overline{BW[a:d]}$ are inactive, the cycle is a read cycle.
$\overline{OE}$	I	ASYNC	Asynchronous output enable. I/O pins are driven when $\overline{OE}$ is active and chip is in read mode.
$\overline{LBO}$	I	STATIC	Selects Burst mode. When tied to V_{DD} or left floating, device follows interleaved Burst order. When driven Low, device follows linear Burst order. *This signal is internally pulled High.*
TDO	O	SYNC	Serial data-out to the JTAG circuit. Delivers data on the negative edge of TCK (BGA only).
TDI	I	SYNC	Serial data-in to the JTAG circuit. Sampled on the rising edge of TCK (BGA only).
TMS	I	SYNC	This pin controls the Test Access Port state machine. Sampled on the rising edge of TCK (BGA only).
TCK	I	Test Clock	Test Clock. All inputs are sampled on the rising edge of TCK. All outputs are driven from the falling edge of TCK.
ZZ	I	ASYNC	Snooze. Places device in low power mode; data is retained. Connect to GND if unused.
NC	-	-	No connects

Write enable truth table (per byte)

Function	$\overline{GWE}$	$\overline{BWE}$	$\overline{BWa}$	$\overline{BWb}$	$\overline{BWc}$	$\overline{BWd}$
Write All Bytes	L	X	X	X	X	X
	H	L	L	L	L	L
Write Byte a	H	L	L	H	H	H
Write Byte c and d	H	L	H	H	L	L
Read	H	H	X	X	X	X
	H	L	H	H	H	H

Key: X = don't care, L = low, H = high, n = a, b, c, d; $\overline{BWE}$, $\overline{BWn}$ = internal write signal.

Burst sequence table

Interleaved burst address					Linear burst address				
	A1 A0	A1 A0	A1 A0	A1 A0		A1 A0	A1 A0	A1 A0	A1 A0
1st Address	0 0	0 1	1 0	1 1	1st Address	0 0	0 1	1 0	1 1
2nd Address	0 1	0 0	1 1	1 0	2nd Address	0 1	1 0	1 1	0 0
3rd Address	1 0	1 1	0 0	0 1	3rd Address	1 0	1 1	0 0	0 1
4th Address	1 1	1 0	0 1	0 0	4th Address	1 1	1 0	0 1	1 0

Synchronous truth table

$\overline{CE0}$[1]	CE1	$\overline{CE2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$[2]	$\overline{OE}$	Address accessed	CLK	Operation	DQ
H	X	X	X	L	X	X	X	NA	L to H	Deselect	Hi–Z
L	L	X	L	X	X	X	X	NA	L to H	Deselect	Hi–Z
L	L	X	H	L	X	X	X	NA	L to H	Deselect	Hi–Z
L	X	H	L	X	X	X	X	NA	L to H	Deselect	Hi–Z
L	X	H	H	L	X	X	X	NA	L to H	Deselect	Hi–Z
L	H	L	L	X	X	X	L	External	L to H	Begin read	Q
L	H	L	L	X	X	X	H	External	L to H	Begin read	Hi–Z
L	H	L	H	L	X	H	L	External	L to H	Begin read	Q
L	H	L	H	L	X	H	H	External	L to H	Begin read	Hi–Z
X	X	X	H	H	L	H	L	Next	L to H	Continue read	Q
X	X	X	H	H	L	H	H	Next	L to H	Continue read	Hi–Z
X	X	X	H	H	H	H	L	Current	L to H	Suspend read	Q
X	X	X	H	H	H	H	H	Current	L to H	Suspend read	Hi–Z
H	X	X	X	H	L	H	L	Next	L to H	Continue read	Q
H	X	X	X	H	L	H	H	Next	L to H	Continue read	Hi–Z
H	X	X	X	H	H	H	L	Current	L to H	Suspend read	Q
H	X	X	X	H	H	H	H	Current	L to H	Suspend read	Hi–Z
L	H	L	H	L	X	L	X	External	L to H	Begin write	D[3]
X	X	X	H	H	L	L	X	Next	L to H	Continue write	D
H	X	X	X	H	L	L	X	Next	L to H	Continue write	D
X	X	X	H	H	H	L	X	Current	L to H	Suspend write	D
H	X	X	X	H	H	L	X	Current	L to H	Suspend write	D

1 X = don't care, L = low, H = high

2 For $\overline{WRITE}$, L means any one or more byte write enable signals ($\overline{BWa}$, $\overline{BWb}$, $\overline{BWc}$ or $\overline{BWd}$) and $\overline{BWE}$ are LOW or $\overline{GWE}$ is LOW. $\overline{WRITE}$ = HIGH for all $\overline{BWx}$, $\overline{BWE}$, $\overline{GWE}$ HIGH. See "Write enable truth table (per byte)," on page 6 for more information.

3 For write operation following a READ, $\overline{OE}$ must be high before the input data set up time and held high throughout the input hold time

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Power supply voltage relative to GND	V_{DD}, V_{DDQ}	–0.5	+4.6	V
Input voltage relative to GND (input pins)	V_{IN}	–0.5	V_{DD} + 0.5	V
Input voltage relative to GND (I/O pins)	V_{IN}	–0.5	V_{DDQ} + 0.5	V
Power dissipation	P_d	–	1.8	W
Short circuit output current	I_{OUT}	–	20	mA
Storage temperature (TQFP)	T_{stg} (TQFP)	–65	+150	°C
Storage temperature (BGA)	T_{stg} (BGA)	–65	+125	°C
Temperature under bias	T_{bias}	–65	+135	°C

Stresses greater than those listed under “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect reliability.

Recommended operating conditions at 3.3V I/O

Parameter	Symbol	Min	Nominal	Max	Unit
Supply voltage for inputs	V_{DD}	3.135	3.3	3.465	V
Supply voltage for I/O	V_{DDQ}	3.135	3.3	3.465	V
Ground supply	Vss	0	0	0	V

Recommended operating conditions at 2.5V I/O

Parameter	Symbol	Min	Nominal	Max	Unit
Supply voltage for inputs	V_{DD}	3.135	3.3	3.465	V
Supply voltage for I/O	V_{DDQ}	2.375	2.5	2.625	V
Ground supply	Vss	0	0	0	V

DC electrical characteristics for 3.3V I/O operation

Parameter	Sym	Conditions	Min	Max	Unit
Input leakage current[1]	$\|I_{LI}\|$	V_{DD} = Max, OV ≤ V_{IN} ≤ V_{DD}	-2	2	µA
Output leakage current	$\|I_{LO}\|$	OE ≥ V_{IH}, V_{DD} = Max, OV ≤ V_{OUT} ≤ V_{DDQ}	-2	2	µA
Input high (logic 1) voltage	V_{IH}	Address and control pins	2	V_{DD}+0.3	V
		I/O pins	2	V_{DDQ}+0.3	
Input low (logic 0) voltage	V_{IL}	Address and control pins	-0.3*	0.8	V
		I/O pins	-0.5*	0.8	
Output high voltage	V_{OH}	I_{OH} = –4 mA, V_{DDQ} = 3.135V	2.4	–	V
Output low voltage	V_{OL}	I_{OL} = 8 mA, V_{DDQ} = 3.465V	–	0.4	V

1 $\overline{FT}$, $\overline{LBO}$, and ZZ pins and the 165 BGA JTAG pins (TMS, TDI, and TCK) have an internal pull-up or pull-down, and input leakage = ±10 µa.

DC electrical characteristics for 2.5V I/O operation

Parameter	Sym	Conditions	Min	Max	Unit
Input leakage current	$\|I_{LI}\|$	V_{DD} = Max, OV ≤ V_{IN} ≤ V_{DD}	-2	2	µA
Output leakage current	$\|I_{LO}\|$	OE ≥ V_{IH}, V_{DD} = Max, OV ≤ V_{OUT} ≤ V_{DDQ}	-2	2	µA
Input high (logic 1) voltage	V_{IH}	Address and control pins	1.7	V_{DD}+0.3	V
		I/O pins	1.7	V_{DDQ}+0.3	V
Input low (logic 0) voltage	V_{IL}	Address and control pins	-0.3*	0.7	V
		I/O pins	-0.3*	0.7	V
Output high voltage	V_{OH}	I_{OH} = –4 mA, V_{DDQ} = 2.375V	1.7	–	V
Output low voltage	V_{OL}	I_{OL} = 8 mA, V_{DDQ} = 2.625V	–	0.7	V

*V_{IL} min = -1.5 for pulse width less than 0.2 X t_{CYC}

I_{DD} operating conditions and maximum limits

Parameter	Sym	Conditions	-85	-10	Unit
Operating power supply current[1]	I_{CC}	$\overline{CE0}$ = V_{IL}, CE1 = V_{IH}, $\overline{CE2}$ = V_{IL}, f = f_{Max}, I_{OUT} = 0 mA	250	230	mA
Standby power supply current	I_{SB}	Deselected, f = f_{Max}, ZZ ≤ V_{IL}	90	80	mA
	I_{SB1}	Deselected, f = 0, ZZ ≤ 0.2V, all V_{IN} ≤ 0.2V or ≥ V_{DD} – 0.2V	40	40	
	I_{SB2}	Deselected, f = f_{Max}, ZZ ≥ V_{DD} – 0.2V, all V_{IN} ≤ V_{IL} or ≥ V_{IH}	40	40	

1 I_{CC} given with no output loading. I_{CC} increases with faster cycle times and greater output loading.

Timing characteristics over operating range

Parameter	Sym	–85		–10		Unit	Notes[1]
		Min	Max	Min	Max		
Cycle time	t_{CYC}	10	–	12	–	ns	
Clock access time	t_{CD}	–	8.5	–	10	ns	
Output enable low to data valid	t_{OE}	–	3.5	–	3.8	ns	
Clock high to output low Z	t_{LZC}	0	–	0	–	ns	2,3,4
Data output invalid from clock high	t_{OH}	3.0	–	3.0	–	ns	2
Output enable low to output low Z	t_{LZOE}	0	–	0	–	ns	2,3,4
Output enable high to output high Z	t_{HZOE}	–	3.5	-	3.8	ns	2,3,4
Clock high to output high Z	t_{HZC}	–	3.5	-	3.8	ns	2,3,4
Output enable high to invalid output	t_{OHOE}	0	–	0	–	ns	
Clock high pulse width	t_{CH}	2.4	–	2.4	–	ns	5
Clock low pulse width	t_{CL}	2.3	–	2.4	–	ns	5
Address setup to clock high	t_{AS}	1.5	–	1.5	–	ns	6
Data setup to clock high	t_{DS}	1.5	–	1.5	–	ns	6
Write setup to clock high	t_{WS}	1.5	–	1.5	–	ns	6,7
Chip select setup to clock high	t_{CSS}	1.5	–	1.5	–	ns	6,8
Address hold from clock high	t_{AH}	0.5	–	0.5	–	ns	6
Data hold from clock high	t_{DH}	0.5	–	0.5	–	ns	6
Write hold from clock high	t_{WH}	0.5	–	0.5	–	ns	6,7
Chip select hold from clock high	t_{CSH}	0.5	–	0.5	–	ns	6,8
$\overline{ADV}$ setup to clock high	t_{ADVS}	1.5	–	1.5	–	ns	6
$\overline{ADSP}$ setup to clock high	t_{ADSPS}	1.5	–	1.5	–	ns	6
$\overline{ADSC}$ setup to clock high	t_{ADSCS}	1.5	–	1.5	–	ns	6
$\overline{ADV}$ hold from clock high	t_{ADVH}	0.5	–	0.5	–	ns	6
$\overline{ADSP}$ hold from clock high	t_{ADSPH}	0.5	–	0.5	–	ns	6
$\overline{ADSC}$ hold from clock high	t_{ADSCH}	0.5	–	0.5	–	ns	6

1 See “Notes” on page 20.

IEEE 1149.1 serial boundary scan (JTAG)

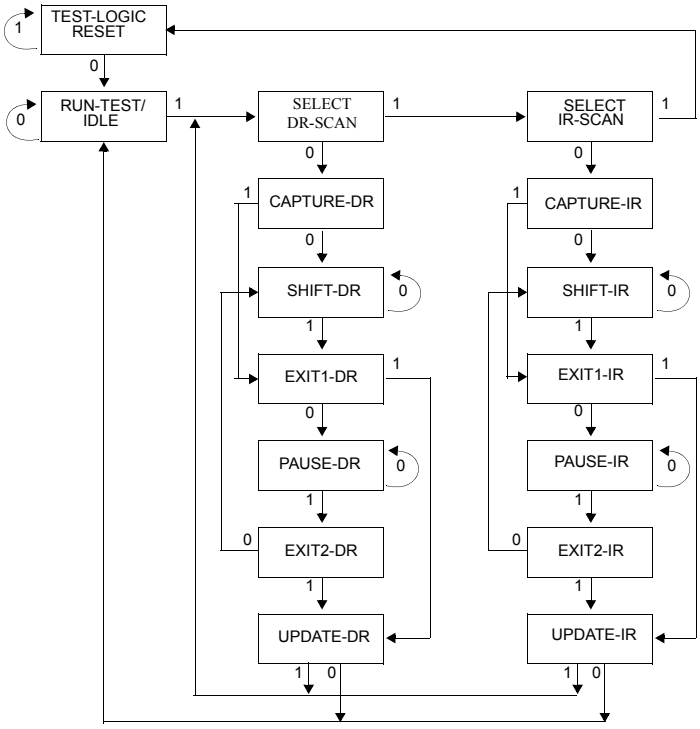
The SRAM incorporates a serial boundary scan test access port (TAP). The port operates in accordance with IEEE Standard 1149.1-1990 but does not have the set of functions required for full 1149.1 compliance. The inclusion of these functions would place an added delay in the critical speed path of the SRAM. The TAP controller functionality does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. It uses JEDEC-standard 2.5V I/O logic levels.

The SRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG feature

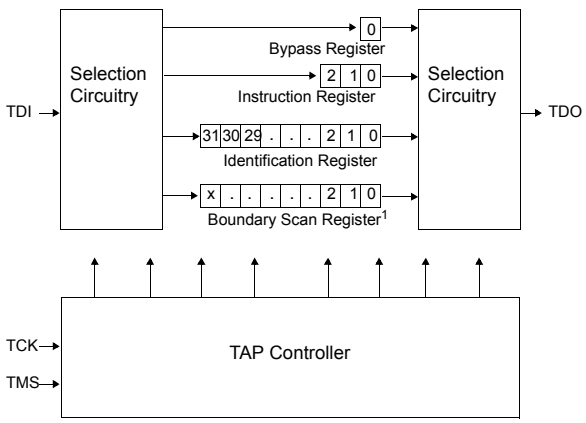
If the JTAG function is not being implemented, TCK should be tied to VSS, TMS and TDI can be left unconnected. At power-up, the device will come up in a reset state which will not interfere with the operation of the device. TDO should be left unconnected.

TAP controller state diagram



Note: The 0 or 1 next to each state represents the value of TMS at the rising edge of TCK.

TAP controller block diagram



[1] x = 53 for the x18 configuration, x = 72 for the x36 configuration.

Test access port (TAP)

Test clock (TCK)

The test clock is used with only the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test mode select (TMS)

The TAP controller receives commands from TMS input. It is sampled on the rising edge of TCK. You can leave this pin/ball unconnected if the TAP is not used. The pin/ball is pulled up internally, resulting in a logic high level.

Test data-in (TDI)

The TDI pin/ball serially inputs information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP Controller State Diagram. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register.

Test data-out (TDO)

The TDO output pin/ball serially clocks data-out from the registers. The output is active depending upon the current state of the TAP state machine. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. (See the TAP Controller State Diagram.)

Performing a TAP RESET

You can perform a RESET by forcing TMS high (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and can be performed while the SRAM is operating.

TAP registers

Registers are connected between the TDI and TDO pins/balls. They allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI pin/ball on the rising edge of TCK. Data is output on the TDO pin/ball on the falling edge of TCK.

Instruction register

You can serially load three-bit instructions into the instruction register. The register is loaded when it is placed between the TDI and TDO pins/balls as shown in the TAP Controller Block Diagram. The instruction register is loaded with the IDCODE instruction at power up and also if the controller is placed in a reset state, as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board-level series test data path.

Bypass register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO pins/balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set low (Vss) when the BYPASS instruction is executed.

Boundary scan register

The boundary scan register is connected to all the input and bidirectional pins/balls on the SRAM. The x36 configuration has a 72-bit-long register and the x18 configuration has a 53-bit-long register.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins/balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/RELOAD, and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The boundary scan order table shows the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The most significant bit (MSB) of the register is connected to TDI, and the least significant bit (LSB) is connected to TDO.

Identification (ID) register

The ID register has a vendor code and other information described in the Identification Register Definitions table. The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state.

TAP instruction set

Eight different instructions are possible with the 3-bit instruction register. All combinations are listed in the Instruction Codes table. Three of these instructions are reserved and should not be used.

Note that the TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented. The TAP controller cannot be used to load address, data, or control signals into the SRAM and cannot preload the I/O buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD. Instead, it performs a capture of the I/O ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins/balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

The EXTEST instruction, which executes whenever the instruction register is loaded with all 0s, is not implemented in this SRAM TAP controller. The TAP controller, however, does recognize an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a high-Z state.

EXTEST is a mandatory 1149.1 instruction. this device, therefore, is not compliant with 1149.1.

IDCODE

The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state. The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins/balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins/balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a high-Z state.

SAMPLE/PRELOAD

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and bidirectional pins/balls is captured in the boundary scan register. Note that the SAMPLE/PRELOAD is a 1149.1 mandatory instruction, but the PRELOAD portion of this instruction is not implemented in this device. The TAP controller, therefore, is not fully 1149.1 compliant.

Be aware that the TAP controller clock can operate only at a frequency up to 10 Mhz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output can undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time (^{t}CS plus ^{t}CH). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is possible to capture all other signals and ignore the value of the CK and CK# captured in the bounder scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

Note that since the PRELOAD part of the command is not implemented, putting the TAP to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

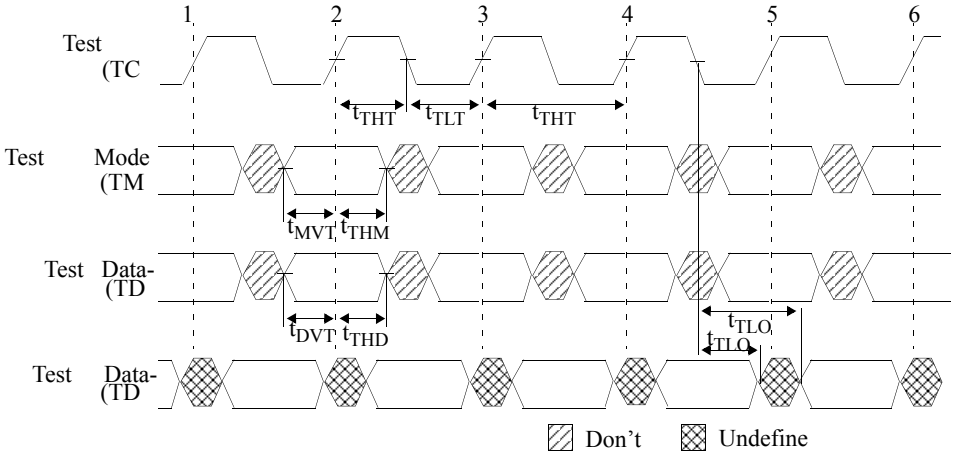
BYPASS

The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board. When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between TDI and TDO.

Reserved

Do not use a reserved instruction. These instructions are not implemented but are reserved for future use.

TAP timing diagram



TAP AC electrical characteristics

For notes 1 and 2, +10°C ≤ T_J ≤ +110°C and +2.4V ≤ V_{DD} ≤ +2.6V.

Description	Symbol	Min	Max	Units
Clock				
Clock cycle time	^{t}THTH	100		ns
Clock frequency	^{f}TF		10	MHz
Clock high time	^{t}THTL	40		ns
Clock low time	^{t}TLTH	40		ns
Output Times				
TCK low to TDO unknown	^{t}TLOX	0		ns
TCK low to TDO valid	^{t}TLOV		20	ns
TDI valid to TCK high	^{t}DVTH	10		ns
TCK high to TDI invalid	^{t}THDX	10		ns
Setup Times				
TMS setup	^{t}MVTH	10		ns
Capture setup	^{t}CS[1]	10		ns
Hold Times				
TMS hold	^{t}THMX	10		ns
Capture hold	^{t}CH[1]	10		ns

1 ^{t}CS and ^{t}CH refer to the setup and hold time requirements of latching data from the boundary scan register.

2 Test conditions are specified using the load in the figure TAP AC output load equivalent.

TAP AC test conditions

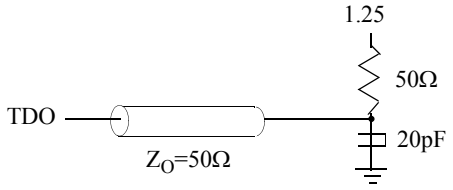
Input pulse levels. . . . . Vss to 2.5V

Input rise and fall times. . . . . 1 ns

Input timing reference levels. 1.25V

Output reference levels 1.25V

TAP AC output load equivalent



3.3V V_{DD}, TAP DC electrical characteristics and operating conditions

(+10°C ≤ T_J ≤ +110°C and +3.135V ≤ V_{DD} ≤ +3.465V unless otherwise noted)

Description	Conditions	Symbol	Min	Max	Units	Notes
Input high (logic 1) voltage		V_{IH}	2.0	V_{DD} + 0.3	V	1, 2
Input low (logic 0) voltage		V_{IL}	-0.3	0.8	V	1, 2
Input leakage current	0V ≤ V_{IN} ≤ V_{DD}	IL_I	-5.0	5.0	µA	
Output leakage current	Outputs disabled, 0V ≤ V_{IN} ≤ V_{DDQ}(DQx)	IL_O	-5.0	5.0	µA	
Output low voltage	I_{OLC} = 100µA	V_{OL1}		0.7	V	1
Output low voltage	I_{OLT} = 2mA	V_{OL2}		0.8	V	1
Output high voltage	I_{OHS} = -100µA	V_{OH1}	2.9		V	1
Output high voltage	I_{OHT} = -2mA	V_{OH2}	2.0		V	1

2.5V V_{DD}, TAP DC electrical characteristics and operating conditions

(+10°C ≤ T_J ≤ +110°C and +2.4V ≤ V_{DD} ≤ +2.6V unless otherwise noted)

Description	Conditions	Symbol	Min	Max	Units	Notes
Input high (logic 1) voltage		V_{IH}	1.7	V_{DD} + 0.3	V	1, 2
Input low (logic 0) voltage		V_{IL}	-0.3	0.7	V	1, 2
Input leakage current	0V ≤ V_{IN} ≤ V_{DD}	IL_I	-5.0	5.0	µA	
Output leakage current	Outputs disabled, 0V ≤ V_{IN} ≤ V_{DDQ}(DQx)	IL_O	-5.0	5.0	µA	
Output low voltage	I_{OLC} = 100µA	V_{OL1}		0.2	V	1
Output low voltage	I_{OLT} = 2mA	V_{OL2}		0.7	V	1
Output high voltage	I_{OHS} = -100µA	V_{OH1}	2.1		V	1
Output high voltage	I_{OHT} = -2mA	V_{OH2}	1.7		V	1

1. All voltage referenced to V_{SS}(GND).

2. Overshoot: V_{IH}(AC) ≤ V_{DD} + 1.5V for t ≤ ^{t}KHKH/2

Undershoot:V_{IL}(AC) ≥ -0.5 for t ≤ ^{t}KHKH/2

Power-up:V_{IH} ≤ +2.6V and V_{DD} ≤ 2.4V and V_{DDQ} ≤ 1.4V for t ≤ 200ms

During normal operation, V_{DDQ} must not exceed V_{DD}. Control input signals (such as $\overline{LD}$, R/$\overline{W}$, etc.) may not have pulsed widths less than t_{KHKL}(Min) or operate at frequencies exceeding f_{KF}(Max).

Identification register definitions

Instruction field	512K x 36	Description
Revision number (31:28)	xxxx	Reserved for version number.
Device depth (27:23)	xxxxx/xxxxx	Defines the depth of 512K words.
Device width (22:18)	xxxxx/xxxxx	Defines the width of x32 or x36 bits.
Device ID (17:12)	xxxxxx	Reserved for future use.
JEDEC ID code (11:1)	00001010010	Allows unique identification of SRAM vendor.
ID register presence indicator (0)	1	Indicates the presence of an ID register.

Scan register sizes

Register name	Bit size	
Instruction	3	
Bypass	1	
ID	32	
Boundary scan	x18:53	x36:72

Instruction codes

Instruction	Code	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM outputs to high-Z state. This instruction is not 1149.1-compliant.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a high-Z state.
Reserved	011	Do not use. This instruction is reserved for future use.
SAMPLE/ PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1-compliant.
Reserved	101	Do not use. This instruction is reserved for future use.
Reserved	110	Do not use. This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

165-ball BGA boundary exit order (x36)

Bit #s	Signal Name	Ball ID
1	SA0	6R
2	SA1	6P
3	SA	4P
4	SA	4R
5	SA	3R
6	SA	3P
7	LBO	1R
8	DQPd	1N
9	DQd	2M
10	DQd	2L
11	DQd	2K
12	DQd	2J
13	DQd	1M
14	DQd	1L
15	DQd	1K
16	DQd	1J
17	NC[1]	1H
18	DQc	2G
19	DQc	2F
20	DQc	2E
21	DQc	2D
22	DQc	1G
23	DQc	1F
24	DQc	1E
25	DQc	1D
26	DQPc	1C
27	SA	2B
28	SA	2A
29	CE0	3A
30	CE1	3B
31	BWd	4B
32	BWb	5A
33	BWc	4A
34	BWa	5B
35	CE2	6A
36	CLK	6B

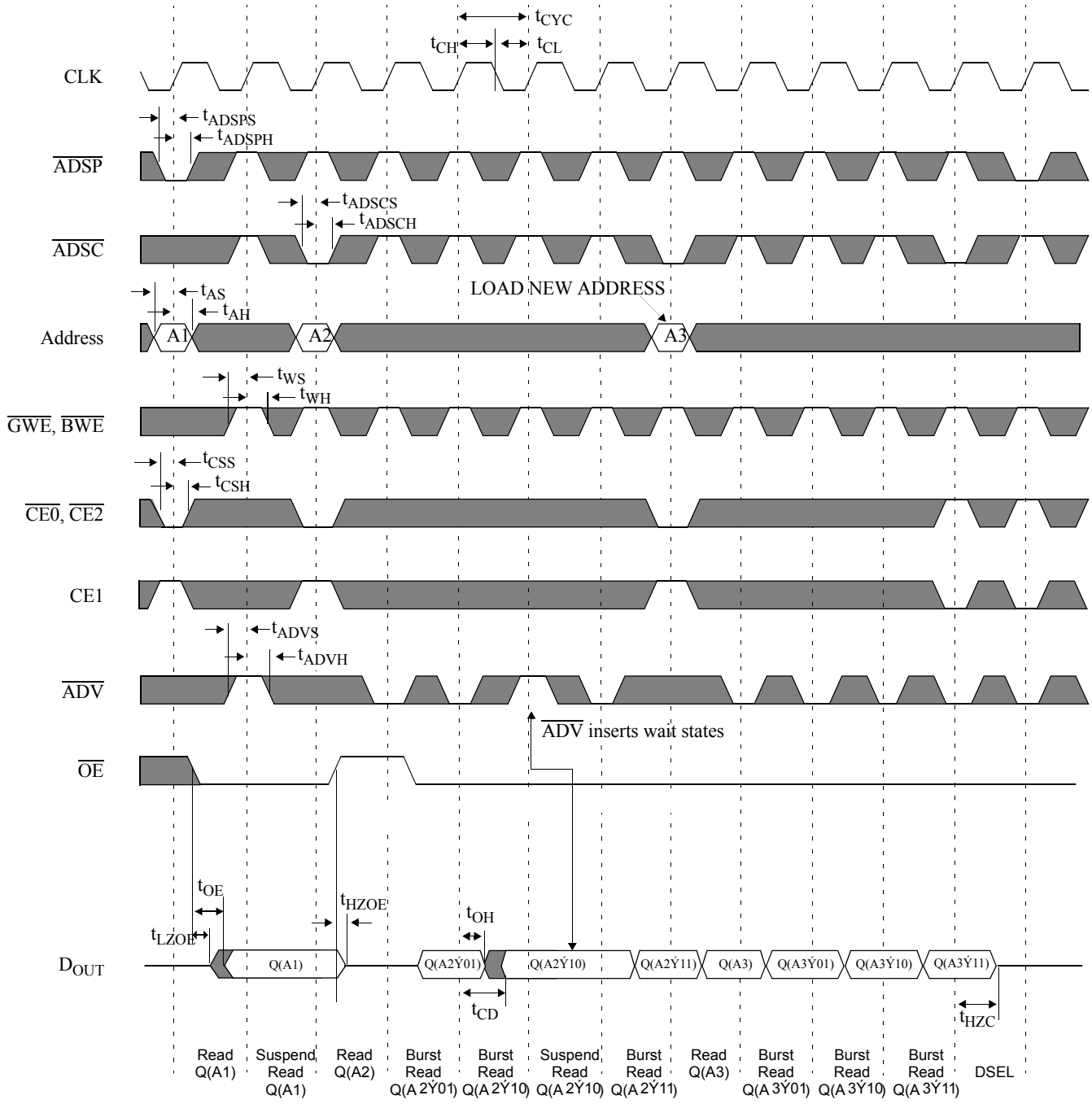
Bit #s	Signal Name	Ball ID
37	GWE	7B
38	BWE	7A
39	OE	8B
40	ADSC	8A
41	ADSP	9B
42	ADV	9A
43	SA	10B
44	SA	10A
45	DQPb	11C
46	DQb	10D
47	DQb	10E
48	DQb	10F
49	DQb	10G
50	DQb	11D
51	DQb	11E
52	DQb	11F
53	DQb	11G
54	ZZ	11H
55	DQa	10J
56	DQa	10K
57	DQa	10L
58	DQa	10M
59	DQa	11J
60	DQa	11K
61	DQa	11L
62	DQa	11M
63	DQPa	11N
64	SA	11R
65	SA	10R
66	SA	10P
67	SA	9P
68	SA	9R
69	SA	8R
70	SA	8P
71	SA	6N
72	SA	11P

1 NC is don't care

Key to switching waveforms

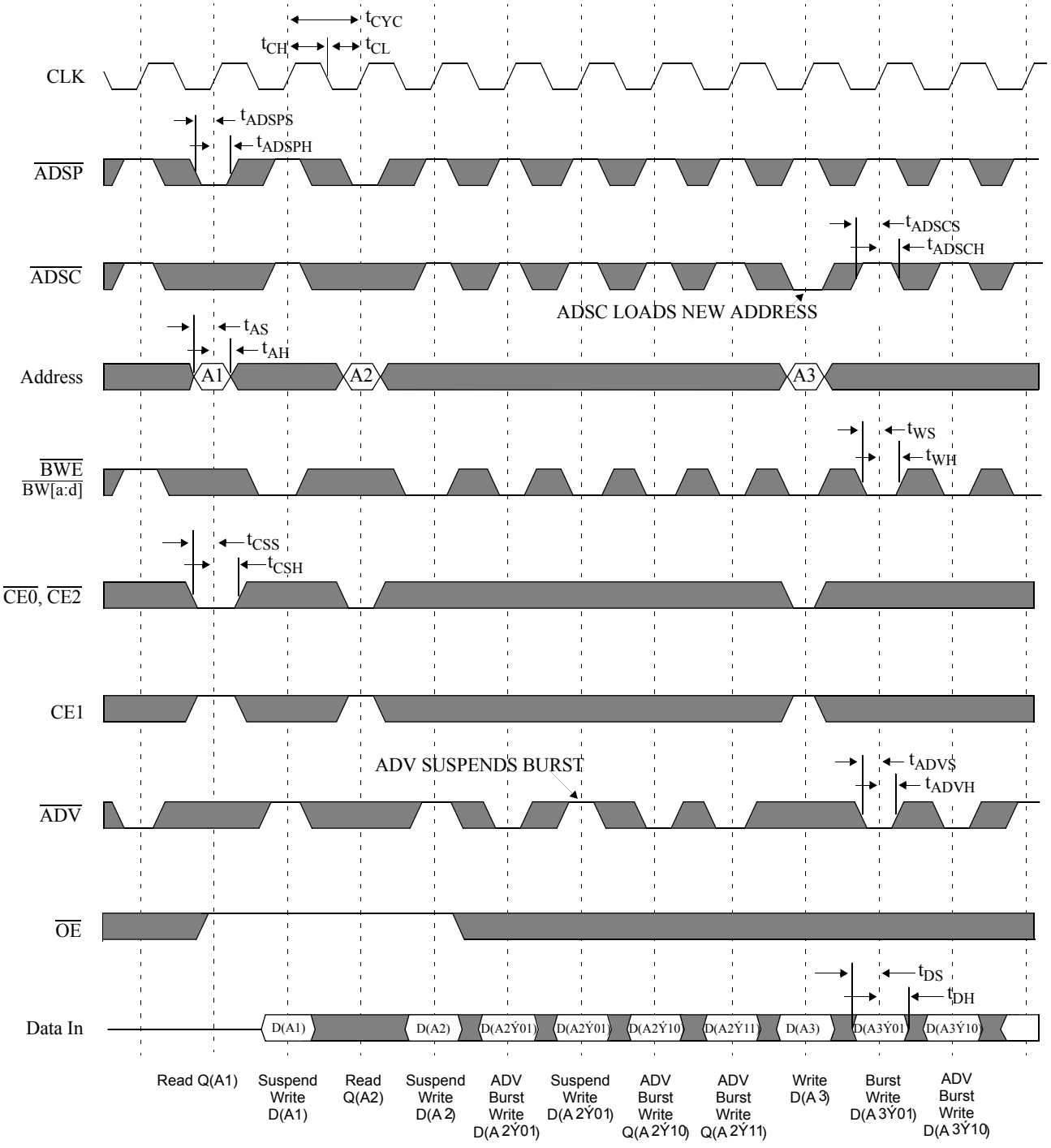
Rising input Falling input Undefined or don't care

Timing waveform of read cycle



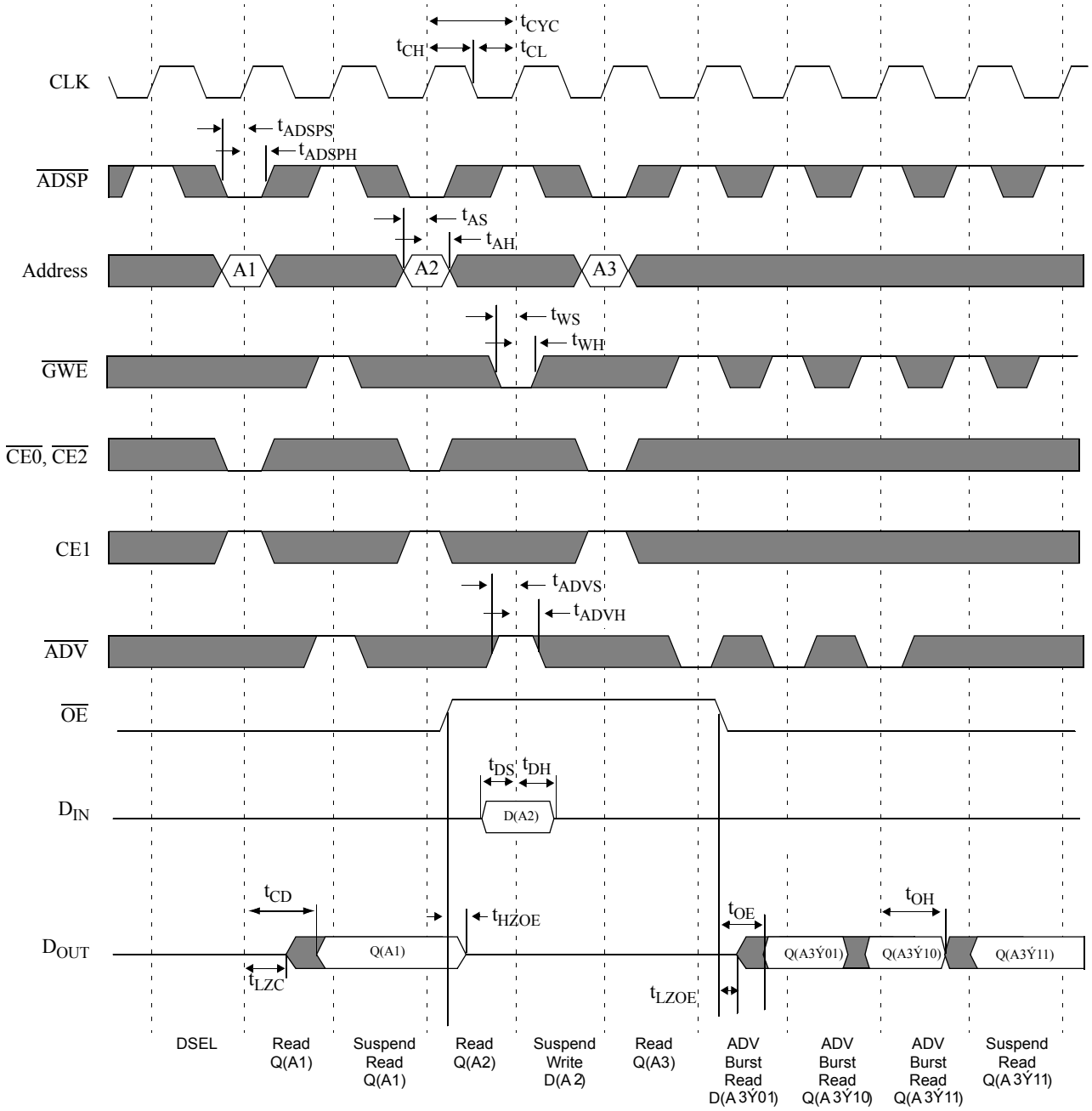
Note: Ý = XOR when $\overline{LBO}$ = high/no connect; Ý = ADD when $\overline{LBO}$ = low. $\overline{BW[a:d]}$ is don't care.

Timing waveform of write cycle



Note: Ý = XOR when $\overline{LBO}$ = high/no connect; Ý = ADD when $\overline{LBO}$ = low.

Timing waveform of read/write cycle



Note: Ý = XOR when $\overline{LBO}$ = high/no connect; Ý = ADD when $\overline{LBO}$ = low.

AC test conditions

- Output load: For t_{LZC}, t_{LZOE}, t_{HZOE}, t_{HZC}, see Figure C. For all others, see Figure B.
- Input pulse level: GND to 3V. See Figure A.
- Input rise and fall time (measured at 0.3V and 2.7V): 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

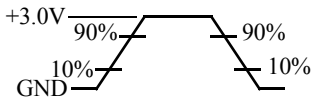


Figure A: Input waveform

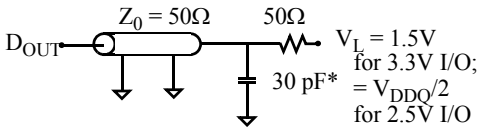


Figure B: Output load (A)

Thevenin equivalent:

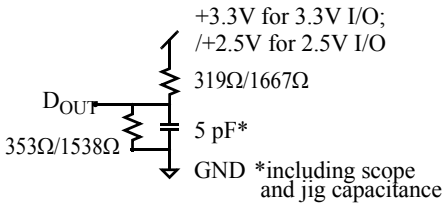


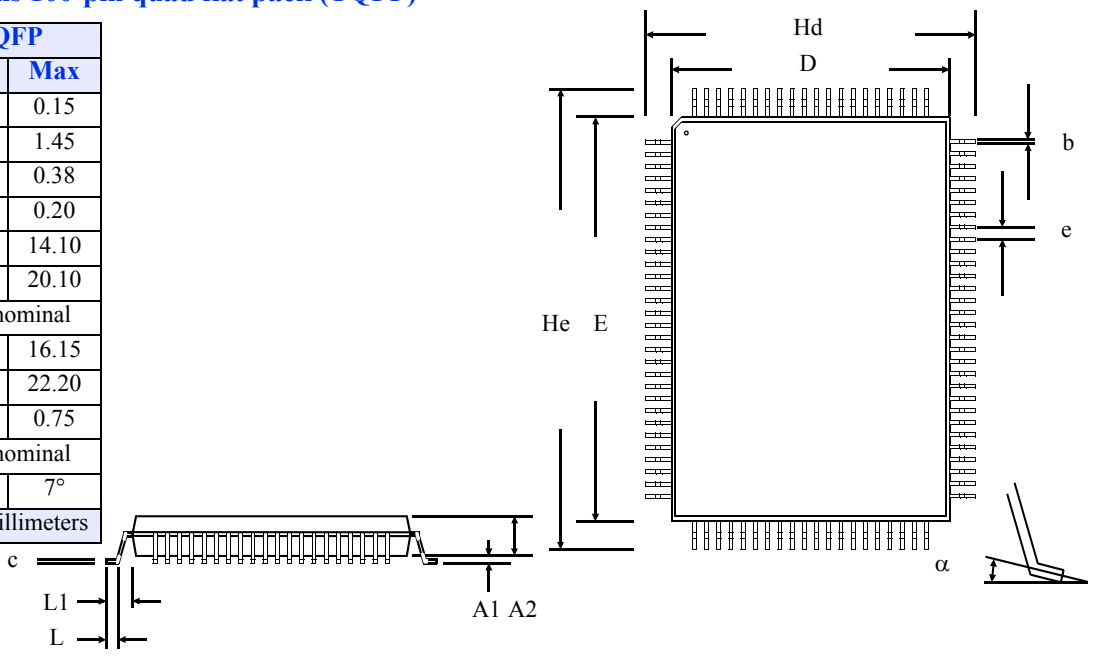
Figure C: Output load(B)

Notes

1 For test conditions, see "AC test conditions", Figures A, B, and C.
2 This parameter is measured with output load condition in Figure C.
3 This parameter is sampled but not 100% tested.
4 t_{HZOE} is less than t_{LZOE}, and t_{HZC} is less than t_{LZC} at any given temperature and voltage.
5 t_{CH} is measured as high if above VIH, and t_{CL} is measured as low if below VIL.
6 This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK. All other synchronous inputs must meet the setup and hold times for all rising edges of CLK when chip is enabled.
7 Write refers to $\overline{\text{GWE}}$, $\overline{\text{BWE}}$, and $\overline{\text{BW}}$[a:d].
8 Chip select refers to $\overline{\text{CE0}}$, CE1, and $\overline{\text{CE2}}$.

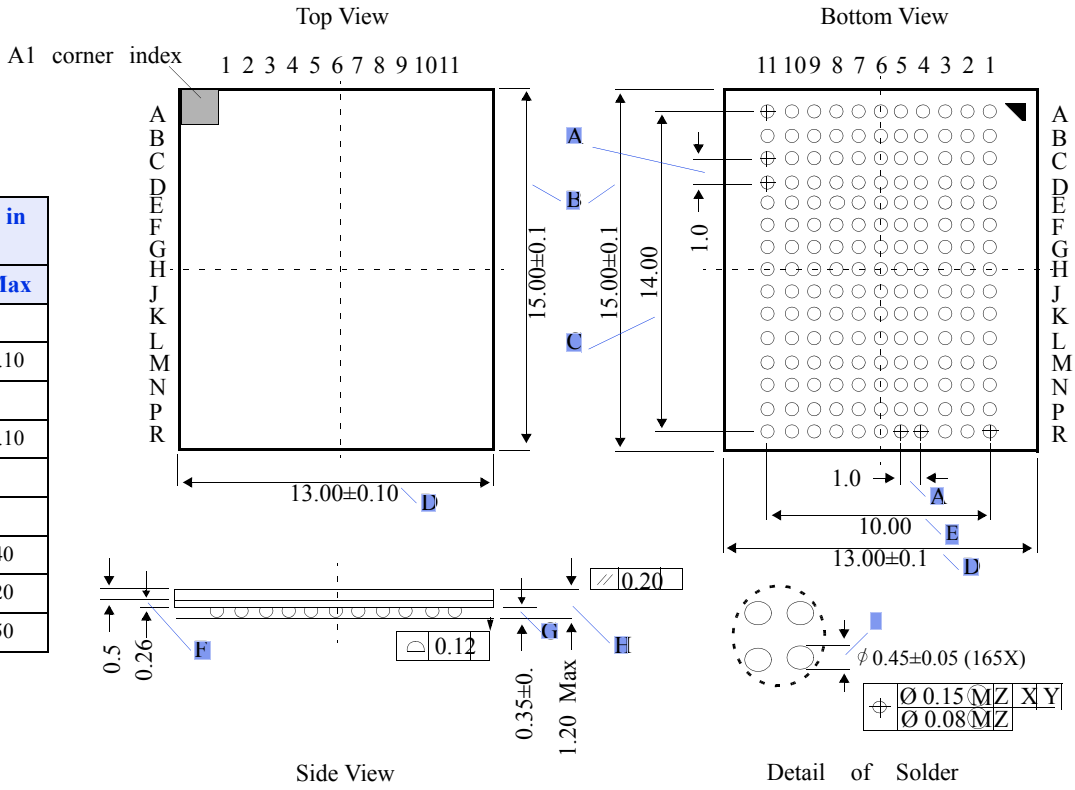
Package dimensions 100-pin quad flat pack (TQFP)

	TQFP	
	Min	Max
A1	0.05	0.15
A2	1.35	1.45
b	0.22	0.38
c	0.09	0.20
D	13.90	14.10
E	19.90	20.10
e	0.65 nominal	
Hd	15.85	16.15
He	21.80	22.20
L	0.45	0.75
L1	1.00 nominal	
α	0°	7°
Dimensions in millimeters		



165-ball BGA (ball grid array)

All measurements are in mm.			
	Min	Typ	Max
A		1.00	
B	14.90	15.00	15.10
C		14.00	
D	12.90	13.00	13.10
E		10.00	
F		0.26	
G	0.30	0.35	0.40
H			1.20
I	0.40	0.45	0.50



Ordering information

Package & Width	-85	-10
TQFP x32	AS7C33512FT32A-85TQC	AS7C33512FT32A-10TQC
	AS7C33512FT32A-85TQI	AS7C33512FT32A-10TQI
TQFP x36	AS7C33512FT36A-85TQC	AS7C33512FT36A-10TQC
	AS7C33512FT36A-85TQI	AS7C33512FT36A-10TQI
BGA x32	AS7C33512FT32A-85BC	AS7C33512FT32A-10BC
	AS7C33512FT32A-85BI	AS7C33512FT32A-10BI
BGA x36	AS7C33512FT36A-85BC	AS7C33512FT36A-10BC
	AS7C33512FT36A-85BI	AS7C33512FT36A-10BI

Note: Add suffix 'N' to the above part number for Lead Free Parts (Ex. AS7C33512FT32A-85TQCN)

Part numbering guide

AS7C	33	512	FT	32/36	A	–XX	TQ or B	C/I	X
1	2	3	4	5	6	7	8	9	10

1.Alliance Semiconductor SRAM prefix

2.Operating voltage: 33 = 3.3V

3.Organization: 512 = 512K

4.Flow-through mode

5.Organization: 32 = x 32; 36 = x 36

6.Production version: A = first production version

7.Clock speed

8.Package type: TQ = TQFP, B = BGA

9.Operating temperature: C = commercial (0° C to 70° C); I = industrial (-40° C to 85° C)

10. N = Lead free part

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Part Number: AS7C33512PFS32A-36A
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