TPS92640 / TPS92641 Synchronous Buck Controllers for Precision Dimming LED Drivers

Check for Samples: TPS92640, TPS92641

FEATURES

- **V_{IN} range from 7V to 85V**
- **Wide dimming range**
  - **500:1 Analog dimming**
  - **2500:1 Standard PWM dimming**
  - **20000:1 Shunt FET PWM dimming**
- **Adjustable LED Current Sense voltage**
- **2Ω, 1A_{peak} MOSFET gate drivers**
- **Shunt Dimming MOSFET gate driver (TPS92641)**
- **Programmable switching frequency**
- **Precision Voltage Reference 3V ±2%**
- **Input UVLO and output OVP**
- **Low Power Shutdown Mode and Thermal Shutdown**

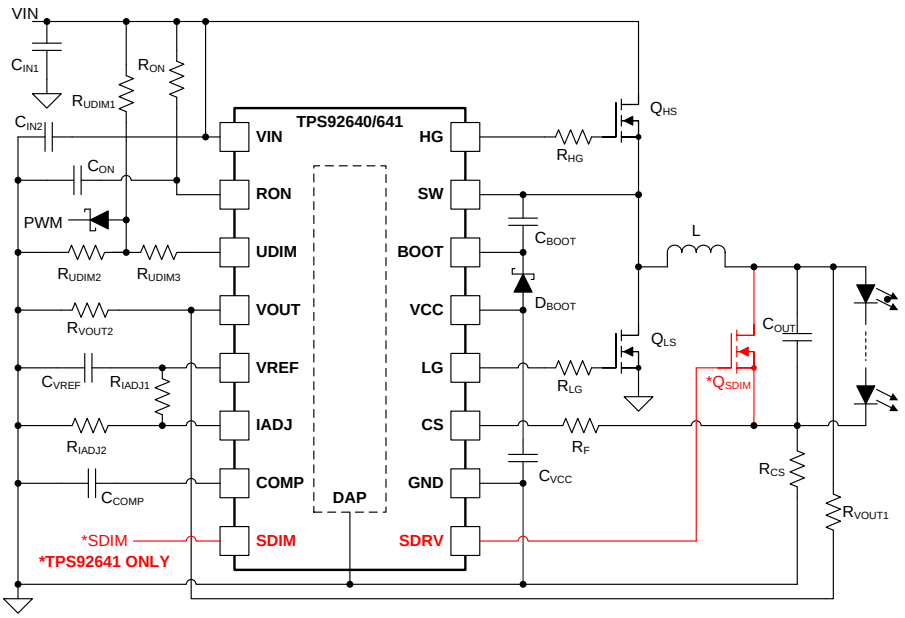
APPLICATIONS

- **LED Driver / Constant Current Regulator**
- **Architectural LED Lighting Drivers**
- **Automotive LED Drivers**
- **General LED Illumination**

DESCRIPTION

The TPS92640/41 are high voltage, synchronous NFET controllers for buck current regulators. Output current regulation is based on valley current-mode operation using a controlled on-time architecture. This control method eases the design of loop compensation whilte maintaining nearly constant switching frequency. The TPS92640/41 includes a high-voltage start-up regulator that operates over a wide input range of 7V to 85V. The PWM controller is designed for high speed capability including an oscillator frequency range up to 1.0 MHz. The deadtime between high side and low side gate driver is optimized to provide very high efficiency over a wide input operating voltage and output power range. The TPS92640/41 accepts both analog and PWM input signals resulting in exceptional dimming control range. Linear response characterisitics between input command and LED current is achieved with true zero LED current using low off-set error amplifier and proprietary PWM dimming logic. Both devices also include precision reference capable of supplying current to low power microcontroller. Protection features include cycle-by-cycle current protection, over-voltage protection and thermal shutdown. The TPS92641 includes a shunt FET dimming input and MOSFET driver for high resolution PWM dimming.

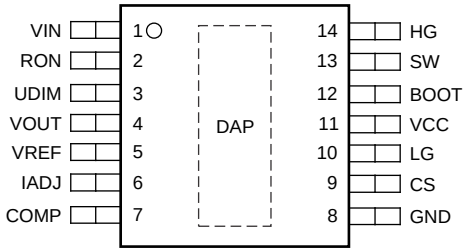
TYPICAL APPLICATION DIAGRAM



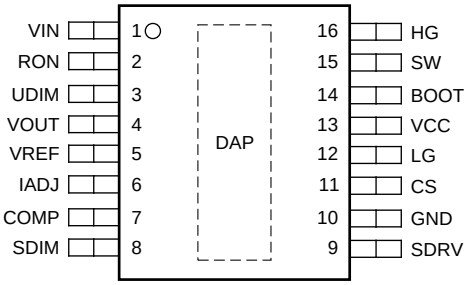
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PIN CONFIGURATION

TPS92640
PWP Package
(Top View)



TPS92641
PWP Package
(Top View)



PIN FUNCTIONS

TPS92640	TPS92641	NAME	DESCRIPTION
1	1	VIN	Connect to input voltage. Connect 1µF bypass capacitor
2	2	RON	Connect a resistor to VIN and capacitor to GND to set switching frequency.
3	3	UDIM	Connect resistor divider from VIN to set under-voltage lockout threshold.
4	4	VOUT	Connect resistor divider from V_{OUT}, scaled down feedback of V_{OUT}.
5	5	VREF	System reference voltage. Bypass with 100nF ceramic capacitor.
6	6	IADJ	Connect resistor divider from VREF to set analog dimming level. Use NTC resistor from pin to GND as resistor divider to implement thermal foldback operation.
7	7	COMP	Connect ceramic capacitor to GND to set loop compensation.
	8	SDIM	PWM dimming input for shunt FET dimming.
	9	SDRV	Connect to gate of external parallel NFET across LED load used for shunt dimming if desired.
8	10	GND	System GND. Connect to DAP.
9	11	CS	Connect to positive terminal of sense resistor at the bottom of the LED stack.
10	12	LG	Connect to gate of low-side NFET of buck regulator. Use series resistor to limit current slew-rate and mitigate EMI noise.
11	13	VCC	Bypass with 2.2µF ceramic capacitor to provide bias supply for controller.
12	14	BOOT	Connect 100nF ceramic capacitor to switch node and diode to VCC to provide boosted voltage for high-side gate drive.
13	15	SW	Connect to switch node of buck regulator.
14	16	HG	Connect to gate of high-side NFET of buck regulator. Use series resistor to limit current slew-rate and mitigate EMI noise.
		DAP	Place 6-9 vias from pad to GND plane for thermal relief

ORDERING INFORMATION

ORDER NUMBER	PACKAGE TYPE	PACKAGE DRAWING	SUPPLIED AS
TPS92640PWP	14-PIN TSSOP EXP PAD	MXA14A	94 Units in Rail
TPS92640PWPT			250 Units on Tape and Reel
TPS92640PWPR			2500 Units on Tape and Reel
TPS92641PWP	16-PIN TSSOP EXP PAD	MXA16A	92 Units in Rail
TPS92641PWPT			250 Units on Tape and Reel
TPS92641PWPR			2500 Units on Tape and Reel

ABSOLUTE MAXIMUM RATINGS(1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales/Office/Distributors for availability and specifications.

		VALUE	UNITS
V_{IN}, UDIM, SW		–0.3 to 90	V
		–1	mA
BOOT		–0.3 to 98.5	V
HG		–0.3 to 90	V
		–2.5 (Pulse < 100ns)	V
LG, SDRV, CS		–0.3 to +V_{CC}	V
		–2.5 (Pulse < 100ns)	V
		V_{CC} + 2.5 (Pulse < 100ns)	V
V_{CC}		–0.3 to 15	V
VREF, RON, COMP, VOUT, IADJ, SDIM		–0.3 to 6	V
		–200 to +200	µA
GND		–0.3 to +0.3	V
		–2.5 to +2.5 (Pulse < 100ns)	V
Continuous Power Dissipation		Internally Limited	
Maximum Junction Temperature		-40 to +125	°C
Storage Temperature Range		–65 to +150	°C
Maximum Lead Temperature (Soldering and Reflow) (2)		260	°C
ESD Rating	Human Body Model, applicable std. JESD22-A114-C	2	kV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified and **do not imply** guaranteed performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics table. All voltages are with respect to the potential at the GND pin, unless otherwise specified.
(2) Refer to TI's packaging website for more detailed information and mounting techniques.

RECOMMENDED OPERATING CONDITIONS(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	Input Voltage Range, V_{IN}	7		85	V
T_J	Junction Temperature Range	–40		125	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified and **do not imply** guaranteed performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics table. All voltages are with respect to the potential at the GND pin, unless otherwise specified.

ELECTRICAL CHARACTERISTICS(1)

Unless otherwise specified V_{IN} = 24V. Limits appearing in **bold type** face apply over the entire junction temperature range of operation, –40°C to 125°C. Specifications appearing in normal type apply for $T_A = T_J$ = 25°C. Datasheet min/max specification limits are specified by design, test or statistical analysis.

PARAMETER		CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
STARTUP REGULATOR (V_{CC}, V_{IN})						
V_{CCREG}	V_{CC} Regulation	I_{CC} = 10 mA, V_{IN} = 24V, 85V	**7.86**	8.5	**9.14**	V
I_{CCLIM}	V_{CC} Current Limit	V_{CC} = 0V	**48**	63	**78**	mA
I_Q	Quiescent Current	V_{UDIM} = 3.0V, Static V_{IN} = 7V/24V/85V		2	**3**	mA
I_{SD}	Shutdown Current	V_{UDIM} = 0V		100		µA
V_{CC-UV}	V_{CC} UVLO Threshold	V_{CC} increasing		5.04	**5.90**	V
		V_{CC} decreasing	**4.5**	4.9		
V_{CC-HYS}	V_{CC} UVLO Hysteresis			0.17		V
REFERENCE VOLTAGE (V_{REF})						
V_{REF}	Reference Voltage	No Load, V_{IN} = 7V/24V/85V	**2.97**	3.03	**3.09**	V
$I_{VREFLIM}$	Current Limit	V_{REF} = 0V	**1.3**	2.1	**2.9**	mA
ERROR AMPLIFIER (CS, COMP)						
V_{CSREF}	CS Reference Voltage	With respect to GND		V_{IADJ}/10		V
$V_{CSREF-OFF}$	Error Amp Input Offset Voltage		**–600**	0	**600**	µV
I_{COMP}	COMP Sink Current			85		µA
	COMP Source Current			110		µA
g_{M-CS}	Transconductance			500		µA/V
	Linear Input Range	See (4)		±125		mV
	Transconductance Bandwidth	-6dB unloaded response(4)		400		kHz
TIMERS / OVER VOLTAGE PROTECTION (RON, VOUT)						
$t_{OFF-MIN}$	Minimum Off-time	CS = 0V		230		ns
t_{ON-MIN}	Minimum On-time			235		ns
t_{ON}	Programmed On-time	V_{VOUT} = 2V, R_{ON} = 25 kΩ, C_{ON} = 1nF		2.08		µs
R_{RON}	RON Pull-down Resistance			35	**120**	Ω
t_{CL}	Current Limit Off-time			270		µs
t_{D-ON}	RON Thresh - HG Falling Delay			25		ns
V_{TH-OVP}	VOUT Over-Voltage Threshold	VOUT rising	**2.85**	3.05	**3.25**	V
$V_{HYS-OVP}$	VOUT Over-Voltage Hysteresis			0.13		V
GATE DRIVER (HG, LG, BOOT, SW)						
R_{SRC-LG}	LG Sourcing Resistance	LG = High		1.5	**6.0**	Ω
R_{SNK-LG}	LG Sinking Resistance	LG = Low		1	**4.5**	Ω
R_{SRC-HG}	HG Sourcing Resistance	HG = High		3.9	**6.0**	Ω
R_{SNK-HG}	HG Sinking Resistance	HG = Low		1.1	**4.5**	Ω
$V_{TH-BOOT}$	BOOT UVLO Threshold	BOOT-SW rising	**1.9**	3.4	**4.5**	V
$V_{HYS-BOOT}$	BOOT UVLO Hysteresis	BOOT-SW falling		1.8		V
T_{D-HL}	HG to LG deadtime	HG fall to LG rise		60		ns
T_{D-LH}	LG to HG deadtime	LG fall to HG rise		60		ns

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified and **do not imply** guaranteed performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics table. All voltages are with respect to the potential at the GND pin, unless otherwise specified.
(2) All limits specified at room temperature (standard typeface) and at temperature extremes (**bold typeface**). All room temperature limits are 100% production tested. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(3) Typical numbers are at 25°C and represent the most likely norm.
(4) These electrical parameters are specified by design, and are not verified by test.

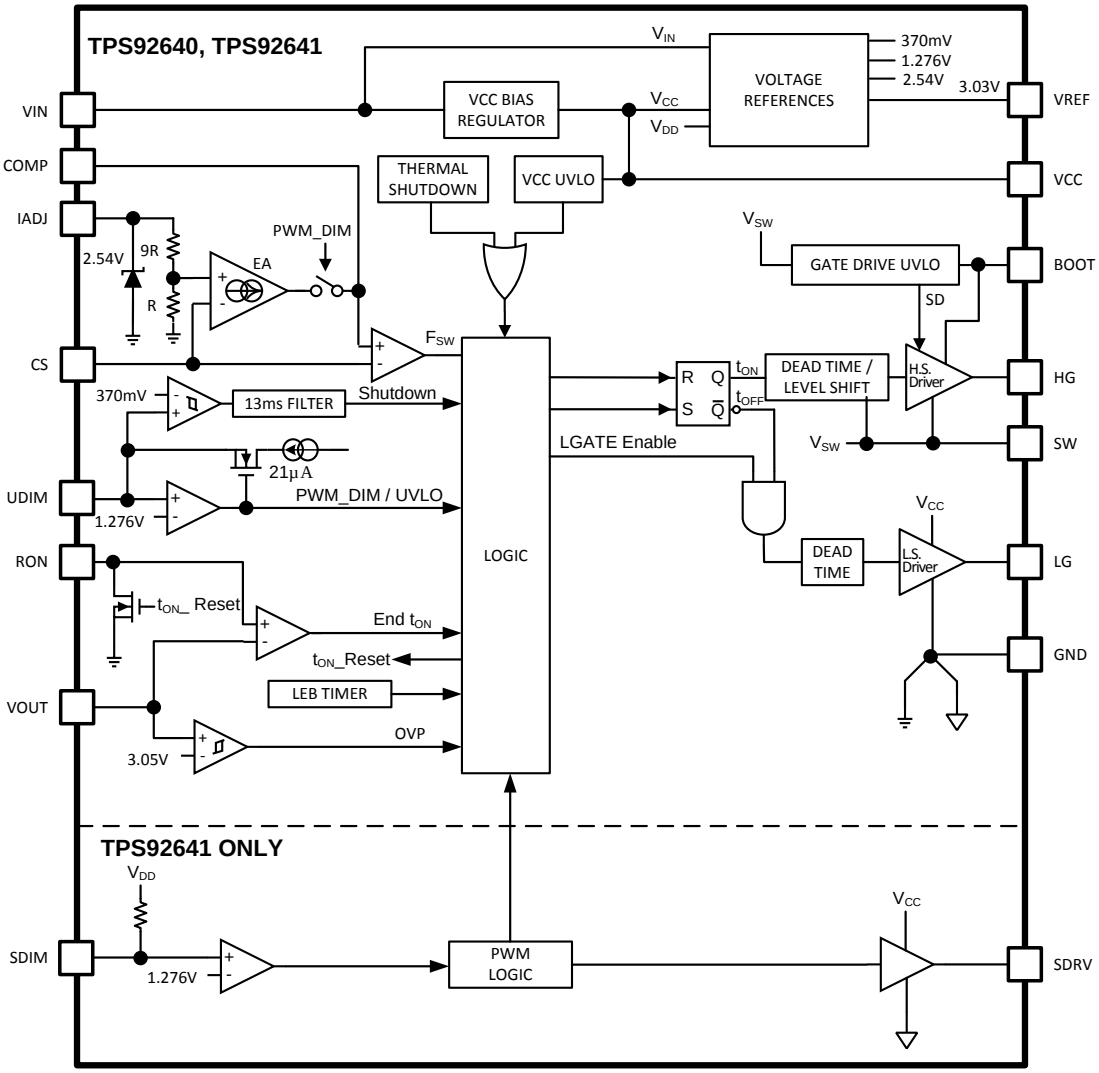
ELECTRICAL CHARACTERISTICS(1) (continued)

Unless otherwise specified V_{IN} = 24V. Limits appearing in **bold type** face apply over the entire junction temperature range of operation, –40°C to 125°C. Specifications appearing in normal type apply for $T_A = T_J$ = 25°C. Datasheet min/max specification limits are specified by design, test or statistical analysis.

PARAMETER		CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
PWM DIMMING (SDIM, SDRV) (TPS92641 only.)						
$R_{SRC-DDRV}$	SDRV Sourcing Resistance	SDRV = High		5.6	**30.0**	Ω
$t_{SDIM-RIS}$	SDIM to SDRV Rising Delay	SDIM rising		68	**100**	ns
$t_{SDIM\ -FALL}$	SDIM to SDRV Falling Delay	SDIM falling		29	**70**	ns
$V_{SDIM-RIS}$	SDIM Rising Threshold	SDIM rising		1.29	**1.74**	V
$V_{SDIM\ -FALL}$	SDIM Falling Threshold	SDIM falling	**0.5**			V
$R_{SDIM-PU}$	SDIM Pull-Up Resistance			90		kΩ
ANALOG ADJUST (IADJ)						
$V_{ADJ-MAX}$	IADJ Clamp Voltage		**2.46**	2.54	**2.62**	V
R_{ADJ}	IADJ Input Impedance			1		MΩ
UNDER-VOLTAGE / PWM (UDIM)						
$V_{TH-UDIM}$	UDIM Startup Threshold	UDIM rising	**1.210**	1.276	**1.342**	V
$I_{HYS-UDIM}$	UDIM Hysteresis Current		**12**	21	**30**	µA
$t_{UDIM-RIS}$	UDIM to HG/LG Rising Delay	UDIM rising		168	**260**	ns
$t_{UDIM-FALL}$	UDIM to HG/LG Falling Delay	UDIM falling		174	**280**	ns
$V_{UDIM-LP}$	UDIM Low Power Threshold			370		mV
$T_{UDIM-DET}$	UDIM Shutdown Detect Timer	UDIM falling	**8.5**	13		ms
THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown Threshold	See (5)		165		°C
T_{HYS}	Thermal Shutdown Hysteresis	See (5)		20		°C
THERMAL RESISTANCE						
$\theta_{JA-TPS92640}$	Junction to Ambient	14L TSSOP EXP PAD (6)		40.0		°C/W
$\theta_{JA-TPS92641}$	Junction to Ambient	16L TSSOP EXP PAD (6)		37.4		°C/W

(5) These electrical parameters are specified by design, and are not verified by test.
(6) Junction-to-ambient thermal resistance is highly board-layout dependent. In applications where high maximum power dissipation exists, namely driving a large MOSFET at high switching frequency from a high input voltage, special care must be paid to thermal dissipation issues during board design. In high-power dissipation applications, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (PD-MAX), and the junction-to ambient thermal resistance of the package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

Unless otherwise stated, –40°C ≤ T_A = T_J ≤ +125°C, V_{IN} = 24V, V_{IADJ}= 2V, I_{LED} = 1A, C_{VCC} = 2.2µF, C_{COMP} = 0.47µF

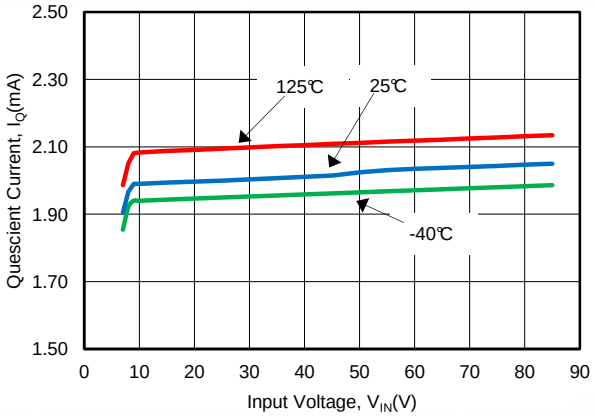


Figure 1. Quescient Current, I_Q vs Input Voltage, V_{IN}

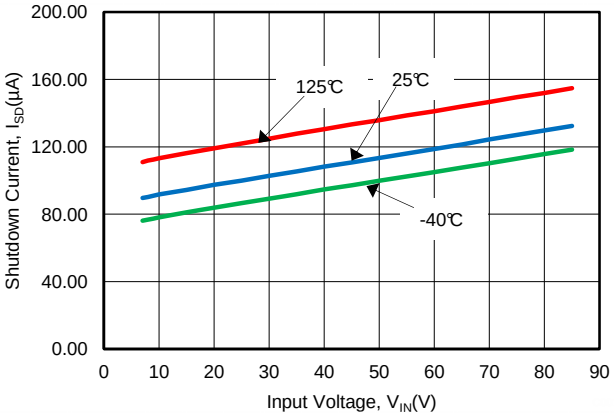


Figure 2. Shutdown Current, I_{SD}vs Input Voltage , V_{IN}

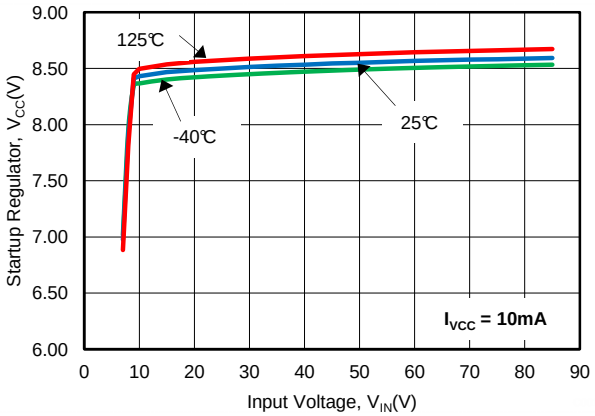


Figure 3. Startup Regulator, V_{CC} vs Input Voltage, V_{IN}

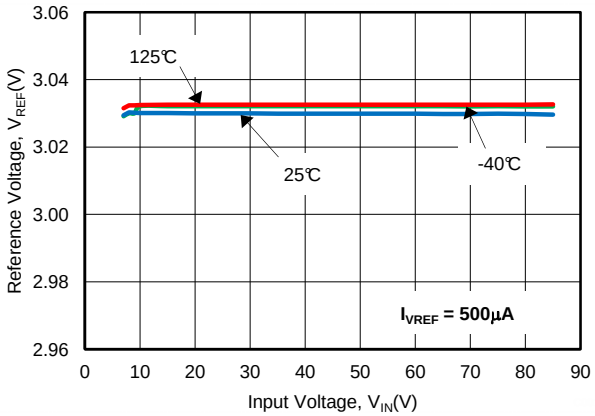


Figure 4. Reference Voltage, V_{REF} vs Input Voltage, V_{IN}

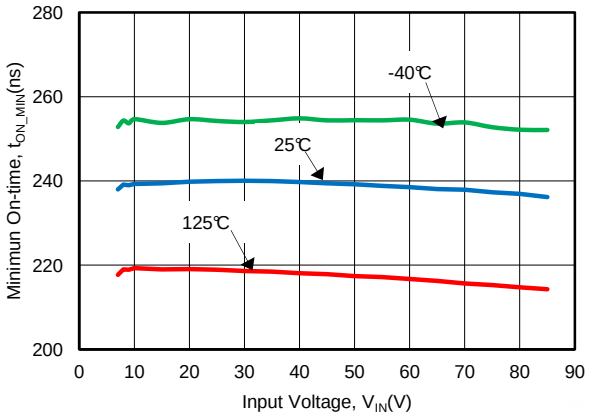


Figure 5. Minimum On-time, t_{ON_MIN} vs Input Voltage, V_{IN}

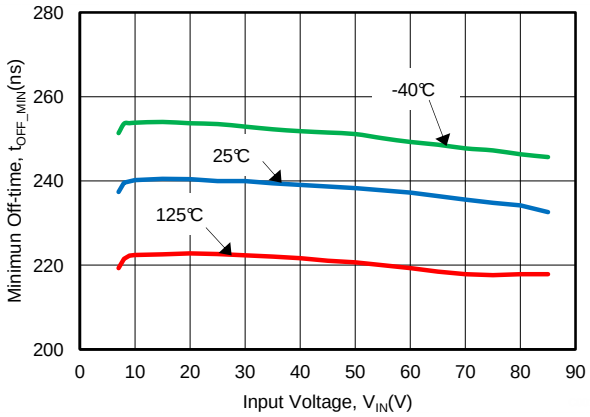


Figure 6. Minimum Off-time, t_{OFF_MIN} vs Input Voltage, V_{IN}

TYPICAL CHARACTERISTICS (continued)

Unless otherwise stated, –40°C ≤ $T_A = T_J$ ≤ +125°C, V_{IN} = 24V, V_{IADJ}= 2V, I_{LED} = 1A, C_{VCC} = 2.2µF, C_{COMP} = 0.47µF

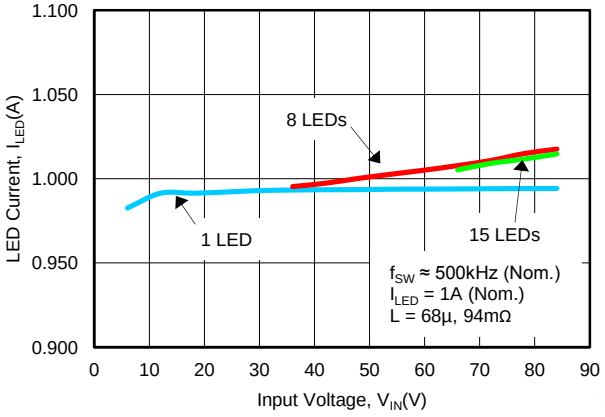


Figure 7. LED Current, I_{LED} vs Input Voltage, V_{IN}

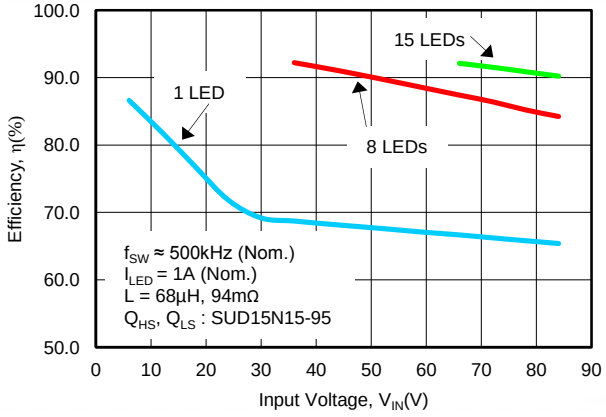


Figure 8. Conversion Efficiency, η vs Input Voltage, V_{IN}

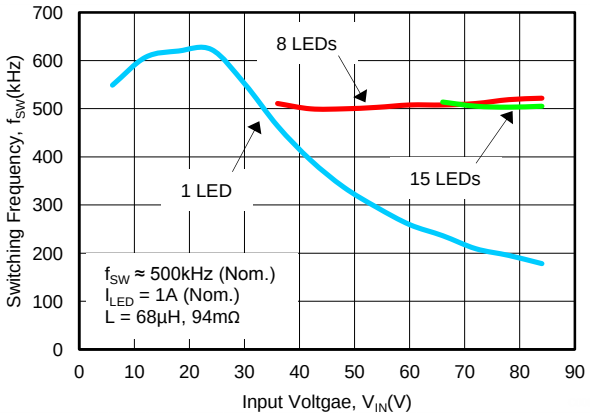


Figure 9. Converter Switching Frequency, f_{SW} vs Input Voltage, V_{IN}

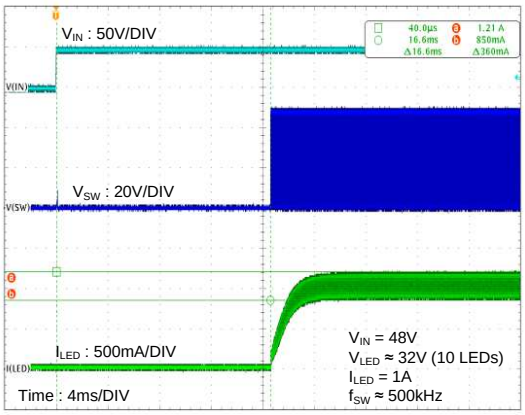


Figure 10. Waveforms of Power-up Transient

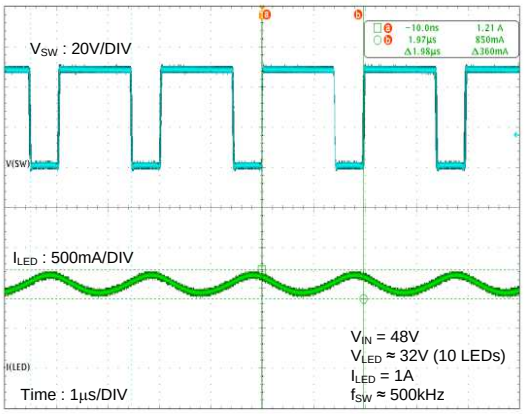


Figure 11. Waveforms of Steady-State Operation

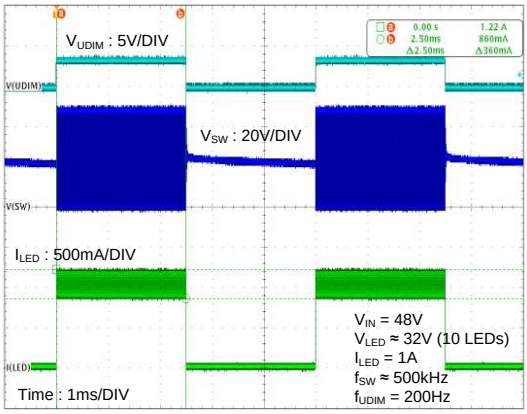


Figure 12. Waveforms of UDIM Operation (D_{DIM} = 0.5)

APPLICATION INFORMATION

TYPICAL APPLICATION DIAGRAM

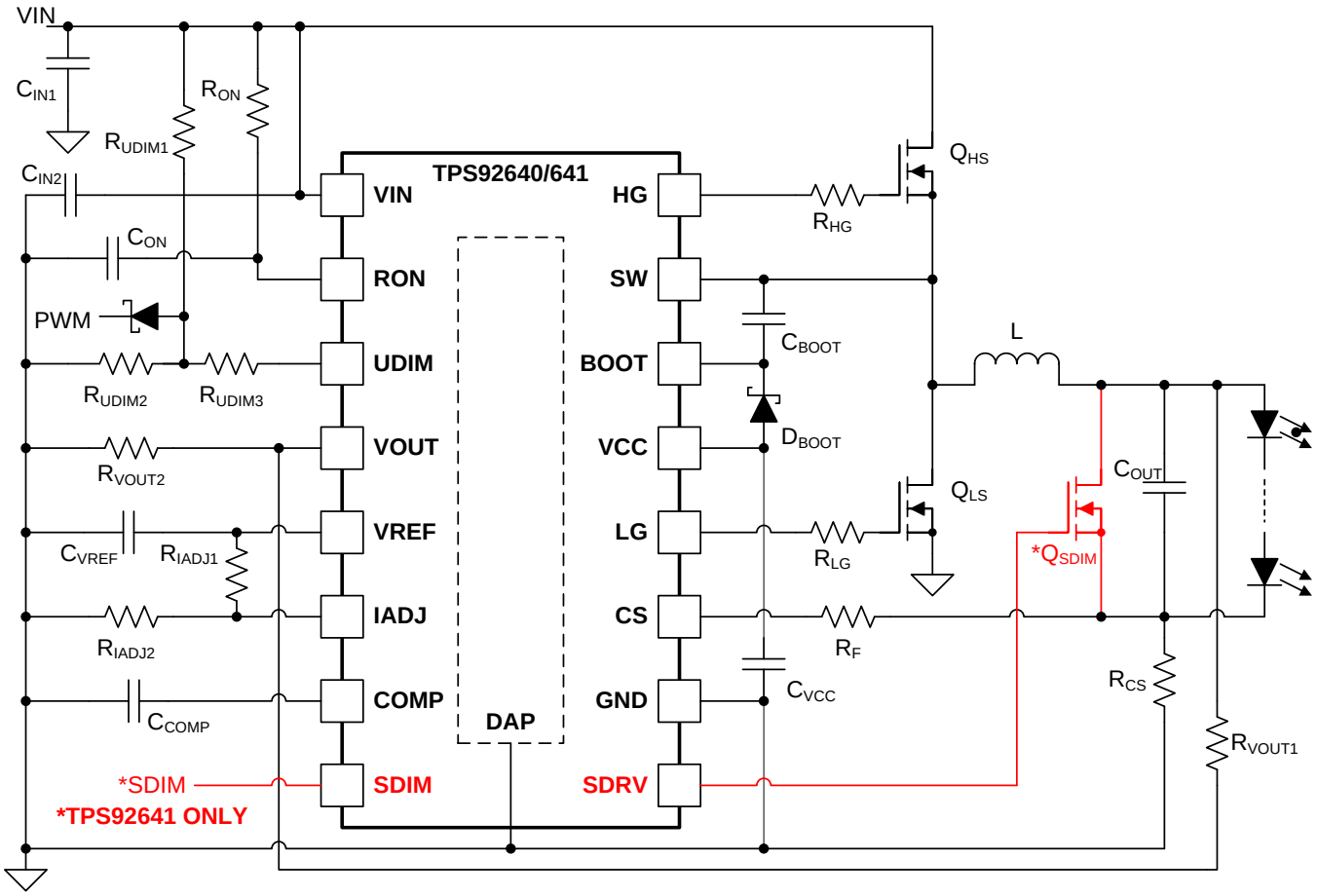


Figure 13. Synchronous Buck LED Driver

The TPS92640/41 are synchronous n-channel MOSFET (NFET) controllers for step-down (buck) current regulators which are ideal for driving LED loads.They can accept wide input voltage range allowing for greater flexibility in powering different series connected LED string combinations. The single current sense pin with low adjustable threshold voltage provides an excellent method for regulating LED current while maintaining high system efficiency. The TPS92640/41 uses valley current control with a controlled on-time architecture that allows the converter to be operated at nearly constant switching frequency without the need for slope compensation. The extremely accurate adjustable current sense threshold together with the synchronous operation provides the capability to amplitude (analog) dim the LED current with high contrast ratios. Excellent PWM dimming is attainable using the main NFETs or the external shunt FET driver (TPS92641 only). TPS92640/41 incorporate 2Ω, 1A internal gate drivers and supports constant current operation up to 5A. This simple controller contains all the features necessary to implement a high efficiency, versatile LED driver with precise dimming reponse.

CONTROLLED ON-TIME ARCHITECTURE

The control architecture is a combination of valley current control and a one-shot on-timer that varies with input and output voltage. The TPS92640/41 uses a series resistor in the LED path to sense both average LED current and valley inductor current. During the time that the high side NFET is turned on (t_{ON}), the input voltage charges up the inductor. When it is turned off (t_{OFF}) and the low side NFET is turned on, the inductor discharges. During both intervals, the current is supplied to the load keeping the LEDs forward biased. Figure 14 shows the inductor current (i_L) waveform for a buck converter operating in continuous conduction mode (CCM). As the system changes input voltage or output voltage, duty cycle D is varied indirectly by changing both t_{ON} and t_{OFF} to regulate I_L and ultimately I_{LED}. For any buck regulator, duty cycle, D, is:

$$D = \frac{T_{ON}}{T_{ON} + T_{OFF}} = \frac{V_{OUT}}{\eta \times V_{IN}}$$

$$V_{OUT} = V_{LED} + V_{CS} \quad (1)$$

where, V_{CS} is the voltage measured at the CS pin of the IC and η is the estimated or actual converter efficiency.

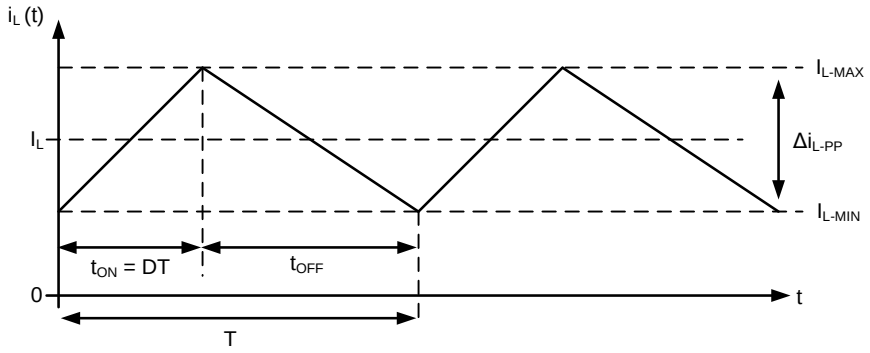


Figure 14. Ideal CCM Buck Converter Inductor Current I_L Waveform

SWITCHING FREQUENCY

The on-time is determined based on the external resistor (R_{ON}) connected between RON and VIN pins in combination with a capacitor (C_{ON}) between RON and GND pins. The input voltage and the R_{ON} resistor set the current sourced into the R_{ON} capacitor which governs the ramp speed. The ramp threshold is proportional to scaled down feedback of V_{OUT} at VOUT pin. The proportionality of V_{OUT} is set by an external resistor divider (R_{VOUT1}, R_{VOUT2}) from V_{OUT}. The switching frequency, f_{SW} can be calculated based on on-time and off-time:

$$\frac{V_{IN}}{R_{ON}} = C_{ON} \times \frac{V_{OUT} \times \frac{R_{VOUT\,2}}{(R_{VOUT\,1} + R_{VOUT\,2})}}{t_{ON}}$$

$$\frac{V_{IN}}{R_{ON}} = C_{ON} \times \frac{V_{IN} \times \frac{t_{ON}}{T} \times \frac{R_{VOUT\,2}}{(R_{VOUT\,1} + R_{VOUT\,2})}}{t_{ON}}$$

$$f_{SW} = \frac{1}{T} = \frac{(R_{VOUT\,1} + R_{VOUT\,2})}{R_{VOUT\,2}} \times \frac{1}{R_{ON} \times C_{ON}} \quad (2)$$

Even though the on-time control is quasi-hysteretic, the input and output voltage proportionality creates a nearly constant switching frequency over the entire operating range. Quasi-hysteretic control minimizes the control loop compensation necessary in many switching regulators, simplifying the design process. It also mitigates current mode instability (also known as sub-harmonic oscillation) found in standard fixed frequency current mode control when operating near or above 50% duty cycle. The inductor current sensing and averaging mechanism in the valley detection control loop provides highly accurate LED current regulation over the entire operating range and temperature.

AVERAGE LED CURRENT

Average LED current regulation is set using a sense resistor in series with the LEDs. The internal error-amplifer regulates the voltage across the sense resistor (V_{CS}) to the IADJ voltage divided by 10. The error amplifier input offset voltage has been minimized using auto-zero calibration technique as shown in . In this chopping scheme the non-inverting and inverting inputs and outputs change polarity every switching cycle to cancel the offset, providing near zero input offset voltage.

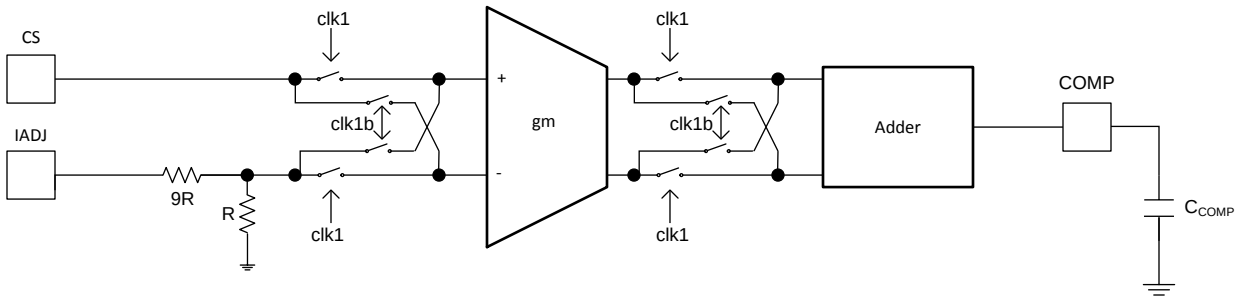


Figure 15. Working Principle of the Chopper OTA to Minimize Input Offset Voltage

IADJ can be set to any value up to 2.54V by connecting it to VREF through a resistor divider for static output current settings. IADJ can also be used to change the regulation point if connected to a controlled voltage source or potentiometer to provide analog dimming. It is also possible to configure IADJ to be used for thermal foldback functions.

$$I_{LED} = \frac{V_{CS}}{R_{CS}} \quad (3)$$

$$V_{CS} = \frac{V_{IADJ}}{10} \quad (4)$$

ANALOG DIMMING AND TRUE-ZERO OPERATION

In traditional Buck converters, discontinuous conduction mode (DCM) operation of inductor current results in loss of linearity at low dimming levels and limits the analog dimming range. When using TPS92640/41 to implement synchronous buck converter, the inductor current is forced to maintain continuous conduction mode (CCM). As a result, it is possible to maintain linearity and achieve true-zero LED current operation with respect to analog dimming command. For true zero application, an external capacitor is required across the LED string in order to provide a negative current path for the inductor current loop. Figure 16 shows the inductor current (I_L) and output voltage (V_{OUT}) waveform for a buck converter operating at true zero average current level.

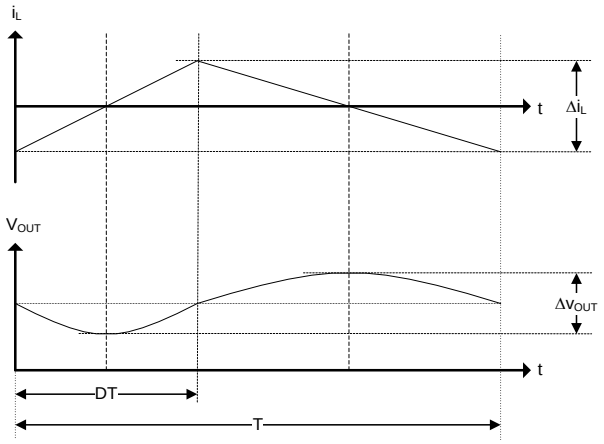


Figure 16. True Zero CCM Buck Converter Inductor Current I_L and Output Voltage V_{OUT} Waveform

In true zero application (V_{IADJ}=0V), there will be a certain amount of I_{LED} passing the LEDs even though the average inductor current is well-regulated at 0A set-point. The shaped area in Figure 17 shows the current that will pass through the LED string (i_{LED}).

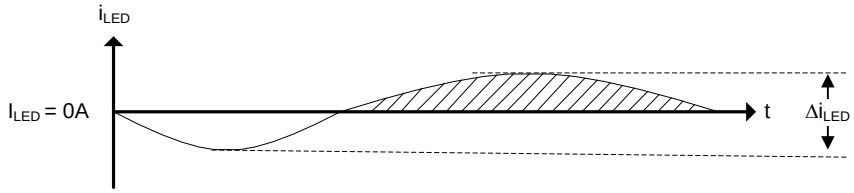


Figure 17. 54Output Current Waveform in True Zero Application with V_{IADJ} = 0V

An external resistor, R_{OFF} as shown in Figure 18 is recommended from V_{OUT} to CS to shunt the positive current ripple while maintaining the operation of error amplifier to cancel input offset voltage. The shunt current (I_{OFF}) should be at least half of the output current ripple to ensure proper operation.

$$I_{OFF} = \frac{V_{OUT}}{R_{OFF} + R_F + R_{CS}} > 0.5 \times \Delta I_{LED}$$

$$R_{OFF} < \frac{V_{OUT}}{0.5 \times \Delta I_{LED}} - (R_F + R_{CS}) \quad (5)$$

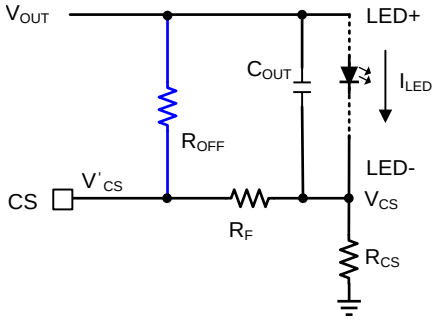


Figure 18. R_{OFF} for True Zero Application

The resistor R_{OFF} also impacts the start-up behavior of the circuit as it creates an dc shift in the voltage sensed at CS pin. To ensure proper start-up sequence and monotonic LED current behavior, the voltage V'_{CS} should exceed a threshold voltage based on the native offset of the error amplifier prior to V_{OUT} exceeding the LED forward voltage, V_{LED}. Assuming a worst case native off-set (non-chopping) of error amplifier to be less than ±10mV, the voltage V'_{CS} must be greater than this threshold to intiate switching and auto-zero operation. Therefore, R_{OFF} should be sized to also meet following condition.

$$V'_{CS} = V_{OUT} \times \left(\frac{R_F + R_{CS}}{R_{OFF} + R_F + R_{CS}} \right) > 0.01$$

$$R_{OFF} < \left[V_{OUT} \times \left(\frac{R_F + R_{CS}}{0.01} \right) - (R_F + R_{CS}) \right]$$

$$R_F >> R_{CS}$$

$$R_{OFF} < (100 \times V_{OUT}) \times R_F \quad (6)$$

To conclude, an external resistor (R_{OFF}) from V_{OUT} to CS pin is required for true zero application, where R_{OFF} should be:

$$R_{OFF} = \min\left[\frac{V_{OUT}}{0.5 \times \Delta I_{LED}} - (R_F + R_{CS}); (100 \times V_{OUT}) \times R_F\right] \quad (7)$$

UNDER-VOLTAGE LOCKOUT (UVLO)

The UDIM pin of the TPS92640/41 is a dual function input that features an accurate 1.276V threshold with programmable hysteresis. This pin functions as both the PWM dimming input of the LEDs and as an input UVLO with built-in hysteresis. When the pin voltage rises and exceeds the 1.276V threshold, 21µA (typical) of current is driven out of the UDIM pin into the resistor divider (R_{UDIM1}, R_{UDIM2}) providing programmable hysteresis. The UVLO turn-on threshold, $V_{TURN-ON}$, is defined by:

$$V_{TURN\_ON} = 1.276V \times \left(\frac{R_{UDIM1} + R_{UDIM2}}{R_{UDIM2}}\right) \quad (8)$$

Once the input voltage is above V_{TURN_ON}, the current source is active and the UVLO hysteresis is determined by:

$$V_{HYS} = 21\mu A \times (R_{UDIM1}) \quad (9)$$

When using the UDIM pin for UVLO and PWM dimming concurrently, the UVLO circuit can have an extra resistor (R_{UDIM3}) to set the hysteresis. This allows the standard resistor divider to have smaller values minimizing delays that can incur with additional external PWM dimming circuitry. In general, at least 3V of hysteresis is preferable when PWM dimming if operating near the UVLO threshold. Under these conditions, the UVLO hysteresis is defined by:

$$V_{HYS} = 21\mu A \times \left(R_{UDIM1} + \frac{R_{UDIM3} \times (R_{UDIM1} + R_{UDIM2})}{R_{UDIM2}}\right) \quad (10)$$

PWM DIMMING USING THE UDIM PIN

The UDIM pin can be driven with a PWM signal which controls the synchronous NFET operation. The brightness of the LEDs can be varied by modulating the duty cycle (D_{DIM}) of this signal using a Schottky diode with anode connected to UDIM pin, as shown in Figure 13.

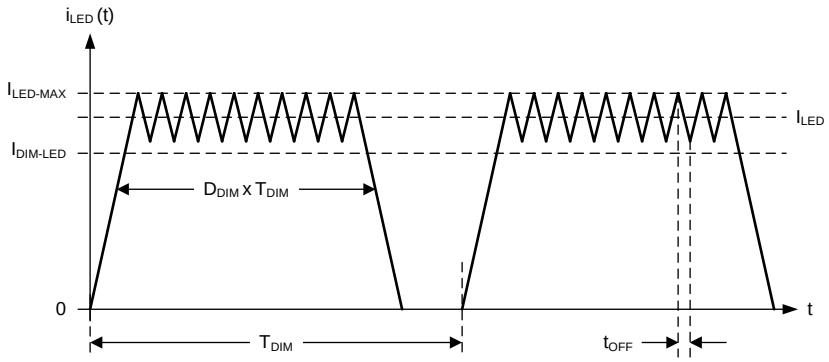


Figure 19. LED Current During UDIM Pin PWM Dimming

Figure 19 shows the LED current waveform during PWM dimming where duty cycle (D_{DIM}) is the percentage of the dimming period (T_{DIM}) that the synchronous NFETs are switching. For the remainder of T_{DIM}, the NFETs are disabled. The resulting dimmed LED current (I_{DIM_LED}) is:

$$I_{DIM\_LED} = D_{DIM} \times I_{LED} \quad (11)$$

LOW POWER SHUTDOWN USING THE UDIM PIN

The TPS92640/41 can be placed into a low power shutdown mode by grounding the UDIM pin directly (any voltage below 370mV) for more than 13ms (typical).

EXTERNAL Shunt FET PWM DIMMING

Extremly high dimming range and lineariy can be achived by using TPS92641 for Shunt FET dimming operation with SDIM and SDRV pin. When higher frequency and time resolution PWM dimming signal is applied to the SDIM pin, the SDRV pin provides an inverted signal of the same frequency and duty cycle that can be used to drive the gate of a Shunt NFET directly across the LED load. Since the output voltage will go to near zero when the Shunt NFET is turned on, the internal on-timer at the RON pin will switch to a fixed minimum on-time during the off-time of the dimming cycle. This method keeps the inductor current slewed up and the converter regulating, without the presence of extremely high switching frequencies. During the on-time of the dimming cycle, the converter will switch in its regular fashion with the programmed on-time at the RON pin. An internal resistor pulls the SDIM pin to logic high if left open. In this case, the SDRV driver will be off.

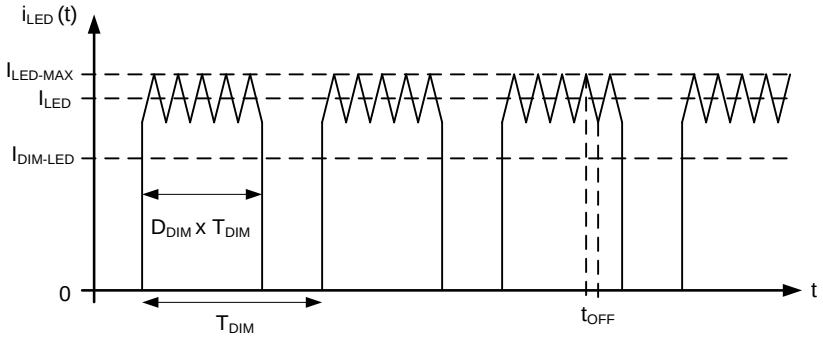


Figure 20. Ideal LED Current During Shunt FET PWM Dimming

Figure 20 shows the ideal LED current waveform during Shunt FET PWM dimming which is very similar to the internal PWM dimming described and shown previously except with much faster rise and fall of the LED current. With this method, only the speed of the parallel Shunt NFET limits the dimming frequency and dimming duty cycle.

VCC REGULATION AND START-UP

The TPS92640/41 includes a high voltage, low-dropout bias regulator. When power is applied, the regulator is enabled and sources current into an external capacitor (C_{VCC}) connected to the VCC pin. The recommended bypass capacitance for the VCC regulator is 2.2µF to 3.3µF. This capacitor should be rated for 10V or greater and an X7R dielectric ceramic is recommended. The output of the VCC regulator is monitored by an internal UVLO circuit that protects the device from attempting to operate with insufficient supply voltage and the supply current is also internally current limited. When V_{IN} is close or lower than 8.5V, the regulator will enter the by-pass mode and the VCC will closely follow V_{IN}. This linear regulator is the primary heat source generator of the device. The amount of heat generated is a function of input voltage (V_{IN}), switching frequency (F_{SW}) and the characteristics of the power MOSFET used. The thermal handling capability of the device imposes a limit on the maximum switching frequency can be used, especially when V_{IN} is higher than 48V and high current power MOSFET is used.

PRECISION REFERENCE

The device includes a precision 3V reference. This can be used in conjunction with a resistor divider to set voltage levels for the IADJ pin and other external circuitry requiring a reference. It can also be used to supply current to low power micro-controllers. The source current capability from VREF pin is internally limited 2.1mA. The recommended bypass capacitance for the VREF regulator is 0.1µF to 1µF.

CONTROL LOOP COMPENSATION

Compensating the TPS92640/41 is relatively simple for most applications. The only compensation needed is a compensation capacitor, C_{COMP} across the COMP pin and ground to place a low frequency dominant pole in the system. The pole must be placed low enough to ensure adequate phase margin at the crossover frequency. For most of the applications, C_{COMP} of 100nF to 470nF is good enough. Additionally, high quality ceramic capacitor with X7R dielectric and a 25V rated is recommended.

OVER-CURRENT PROTECTION

The TPS92640/41 has over-current protection to protect the high side NFET (HS-NFET) along with the rest of the system from over-current conditions. This peak current limit of 1.28V (with V_{IN} = 85V at room temperature) is sensed across the high side FET R_{DS-ON} (from SW to VIN). If the threshold is reached or exceeded, HS-NFET will turn off and the low side NFET (LS-NFET) will turn on for ~800ns. Then HS-NFET will turn on again, if the threshold is still reached or exceeded, both FETs are shutoff for 270µs typical. Figure 21 shows the waveforms of HG and LG under over-current protection.

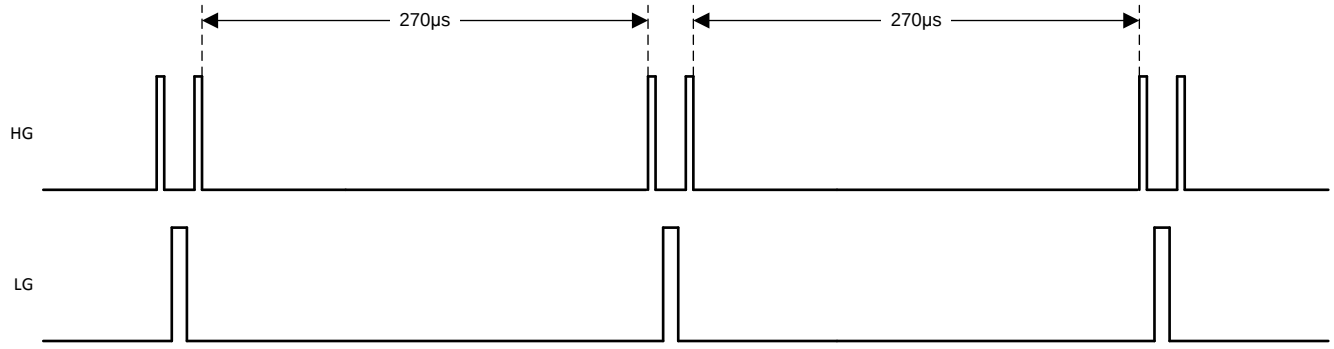


Figure 21. HG and LG Waveforms Under Over-Current Protection

OVER-VOLTAGE PROTECTION (OVP)

The TPS92640/41 has programmable over-voltage protection by using the resistor divider at the VOUT pin. The OVP limit, V_{OVP_ON}, is defined by:

$$V_{OVP\_ON} = 3.05V \times \left(\frac{R_{VOUT1} + R_{VOUT2}}{R_{VOUT2}} \right) \quad (12)$$

If the output voltage reaches V_{OVP_ON}, the HG, LG and SDRV pins are pulled low to prevent damage to the LEDs or the rest of the circuit. The $\overline{OVP}$ circuit has a fixed hysteresis of 100mV before the driver attempts to switch again.

BOOT UNDER-VOLTAGE LOCKOUT (UVLO)

The BOOT UVLO circuit is implemented to ensure proper operation of the high-side gate driver under all operating conditions. The switching operation is commenced once the BOOT voltage exceeds 3.4V above the SW pin. Comparator hysteresis of 1.8V is included to prevent false tripping due to high frequency switching noise. When the BOOT falls below the low voltage threshold (1.6V typical), the high side NFET is disabled by pulling HG pin to SW pin. The next turn-on transition of low-side NFET pulls SW pin down and charges the BOOT capacitor (C_{BOOT}) through VCC. Normal operation is commenced once BOOT capacitor (C_{BOOT}) is charged above BOOT UVLO turn-on threshold of 3.4V.

The boostrap circuit behavior impacts the circuit behavior near dropout (V_{IN}= V_{OUT}) conditions. A minimum off-time is implemented to restrict the maximum duty cycle and maintain charge on the external BOOT capacitor, C_{BOOT}. As the input voltage, V_{IN}, approachs close to the output voltage, V_{OUT}, the output current will fall with the switching frequency, as in conventional Buck regulator. This behavior ensures smooth operation in and out of dropout region while ensuring proper operation of high side gate driver and bootstrap circuit.

THERMAL SHUTDOWN

Internal thermal shutdown circuitry is provided to protect the device in the event that the maximum junction temperature is exceeded. The threshold for thermal shutdown is 165°C with a 20°C hysteresis (both values typical). During thermal shutdown the NFETs and drivers are disabled.

DESIGN CONSIDERATIONS

SWITCHING FREQUENCY

Switching frequency is selected based on the trade-offs between efficiency, solution size/cost and the range of output voltage that can be regulated. Many applications place limits on switching frequency due to EMI sensitiviy. The on-time of the TPS92640/41 can be programmed for switching frequencies ranging from the 10's of kHz to over 1MHz. This on-time varies in proportion to both V_{IN} and V_{OUT}, as described in SWITCHING FREQUENCY. However, in practice the switching frequency will shift in response to large swings in input or output voltage. The maximum switching frequency is limited only by the minimum on-time and minimum off-time requirements.

LED RIPPLE CURRENT

The LED manufacturers generally recommend values of current ripple, ΔI_{LED}, to achieve optimal optical efficiency. The peak-to-peak current ripple values typically range from ±10% to ±40% of DC current, I_{LED}. Higher LED ripple current allows the use of smaller inductors, smaller output capacitors, or no output capacitors at all. Lower ripple current requires more inductance, higher switching frequency, or additional output capacitance. Based on the LED current ripple specification and desired switching frequency, the inductor value can be calculated as follows:

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I_{LED}} \times t_{ON} \quad (13)$$

It is important to ensure that the rated inductor saturation current is greater than the worst case operating current ($I_{LED}+\Delta I_{LED}/2$) under the wide operating temperature range.

BUCK CONVERTERS WITHOUT OUTPUT CAPACITOR

A Buck regulator is ideal for regulating current because of the direct connection between the inductor and the LED load. Because the current is being regulated, not voltage, a buck current regulator is free of load current transients, and has no need of output capacitance to supply the load and maintain output voltage. This is of great benefit when driving LEDs as large electrolytic capacitors impact the lifetimes and PWM dimming performance. The output capacitor can be eliminated by using a large inductor or higher switching frequency as discussed in LED RIPPLE CURRENT

A capacitor placed in parallel with the LED or array of LEDs can be used to reduce Δi_{LED} while keeping the same average current through both the inductor and the LED array. With this topology the inductance can be lowered, making the magnetics smaller and less expensive. Alternatively, the circuit can be run at lower frequency with the same inductor value, improving the efficiency and expanding the range of output voltage that can be regulated.

Figure 22 shows the equivalent impedances presented to the $\Delta i_{L\text{-}PP}$ when an output capacitor, C_{OUT}, and its equivalent series resistance (R_{ESR}) are placed in parallel with the LED array.

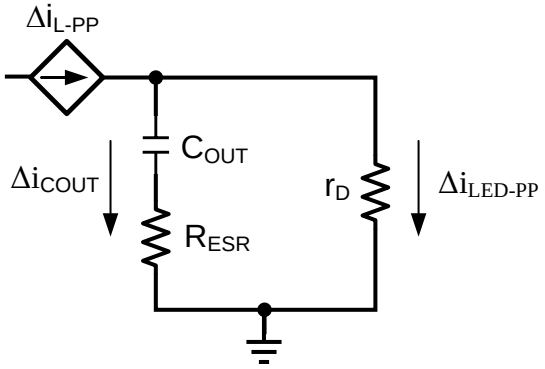


Figure 22. LED Ripple Current with C_{OUT}

To calculate the respective ripple currents, the LED array is represented as the dynamic resistance, (r_D). LED's dynamic resistance is not always specified on the manufacturer's datasheet, but it can be calculated as the inverse slope of the LED's V_{LED} vs I_{LED} curve at the operating point. However it should be reminded that this method only gives an rough estimate of r_D. Total dynamic resistance for a string of n LEDs connected in series can be calculated as the r_D of one device multiplied by n. Inductor ripple current, $\Delta i_{L\text{-}PP}$ is still calculated as before. The following equations can then be used to estimate peak-to-peak LED current ripple, $\Delta i_{LED\text{-}PP}$, when using a parallel capacitor:

$$\Delta i_{LED-PP} = \frac{\Delta i_{L-PP}}{1 + \frac{r_D}{Z_{COUT}}} \qquad Z_{COUT} = \frac{1}{2 \times \pi \times f_{SW} \times C_{OUT}} \tag{14}$$

The calculation for Z_{COUT} assumes that the shape of the inductor ripple current is approximately sinusoidal. Small values of C_{OUT} that do not significantly reduce $\Delta i_{LED\text{-}PP}$ can also be used to control EMI generated by the switching action of the TPS92640/41. EMI reduction becomes more important as the length of the connections between the LED and the rest of the circuit increase.

INPUT CAPACITOR

Input capacitor is selected using requirements for minimum capacitance and rms ripple current. The input capacitor supply pulses of current approximately equal to I_{LED} while the high-side NFET is on, and is charged up by the input voltage while the high-side NFET is off. Switching converters such as the TPS92640/41 have a negative input impedance due to the decrease in input current as input voltage increases. This inverse proportionality of input current to input voltage can cause oscillations (sometimes called 'power supply interaction') if the magnitude of the negative input impedance is greater than the input filter impedance. Minimum capacitance can be selected by comparing the input impedance to the converter's negative resistance; however this requires accurate calculation of the input voltage source inductance and resistance, quantities which can be difficult to determine. An alternative method to select the minimum input capacitance ($C_{IN\text{-}MIN}$) is to select the maximum voltage ripple ($\Delta v_{IN\text{-}MAX}$) which can be tolerated. $\Delta v_{IN\text{-}MAX}$ is equal to the change in voltage across C_{IN} during t_{ON} when it supplies the load current. A good starting point for selection of C_{IN} is to use an input voltage ripple of 2% to 10% of V_{IN}. $C_{IN\text{-}MIN}$ can be selected as follows:

$$C_{IN\_MIN} = \frac{I_{LED} \times t_{ON}}{\Delta v_{IN\_MAX}} = \frac{I_{LED} \times \left(\frac{1}{f_{SW}} - t_{OFF} \right)}{\Delta v_{IN\_MAX}} \tag{15}$$

A minimum input capacitance at least 75% greater than the $C_{IN\text{-}MIN}$ value is recommended. To determine the RMS input current rating ($I_{IN\text{-}RMS}$) the following approximation can be used:

$$I_{IN-RMS} = I_{LED} \times \sqrt{D \times (1-D)} = I_{LED} \times f_{SW} \times \sqrt{t_{ON} \times t_{OFF}} \tag{16}$$

Since this approximation assumes there is no inductor ripple current, the value should be increased by 10-30% depending on the amount of ripple that is expected. Ceramic capacitors are the best choice for the input to the TPS92640/41 due to their high ripple current rating, low ESR, low cost, and small size compared to other types. When selecting a ceramic capacitor, special attention must be paid to the operating conditions of the application. Ceramic capacitors can lose one-half or more of their capacitance at their rated DC voltage bias and also lose capacitance with extremes in temperature. Make sure to check any recommended deratings and also verify if there is any significant change in capacitance at the operating input voltage and the operating temperature.

N-CHANNEL MOSFETs (NFET)

The TPS92640/41 requires two external NFETs for the switching regulator. The FETs should have a voltage rating at least 20% higher than the maximum input voltage to ensure safe operation during the ringing of the switch node. In practice, all switching converters have some ringing at the switch node due to the diode parasitic capacitance and the lead inductance. The NFETs should also have a current rating at least 50% higher than the average transistor current. Once NFETs are chosen, the power rating is verified by calculating the power loss.

EMI AND NOISE CONSIDERATIONS

In synchronous rectifier, the high speed gate drive signals can generate significant conducted and radiated EMI. This noise can couple with high impedance nodes of the IC and result in undesirable operation. A small (4Ω - 10Ω) resistors, R_{HG} and R_{LG}, in series with the gate drive signals are recommended to slow the slew-rate of the SW node and reduce the noise signature. They also improve the robustness of the circuit by reducing the noise coupling in to sensitive nodes such as UDIM, CS, RON and IADJ.

In other to further reduce EMI signature, good PCB layout techniques must be implemented. The loop area between the synchronous NFET, inductor and output capacitor should be minimized to reduce radiated EMI due to switching action. The trace lengths of high impedance nodes (UDIM, CS, RON and IADJ) should be minimized and shielded from switching noise. The parasitic capacitance between switching node and ground node should be minimized to reduce common mode noise. Other common layout techniques such as star ground and noise suppression using local bypass capacitors should be followed to maximize noise rejection and minimize EMI within the circuit.

DESIGN PROCEDURE

1. SET OUTPUT VOLTAGE FEEDBACK RATIO

   For the desired output (V_{OUT}), R_{VOUT1} and R_{VOUT2} is calculated first with the desired feedback voltage, V_{VOUT} at ~2.5V:

$$V_{OUT} \times \frac{R_{VOUT2}}{R_{VOUT1} + R_{VOUT2}} = 2.5V$$

$$\frac{R_{VOUT2}}{R_{VOUT1} + R_{VOUT2}} = \frac{2.5}{V_{OUT}}$$

$$V_{OUT} = V_{LED} + I_{LED} \times R_{SNS} \quad (17)$$

2. SET SWITCHING FREQUENCY

   The switching frequency is set as follows:

$$f_{SW} = \frac{\frac{R_{VOUT1} + R_{VOUT2}}{R_{VOUT2}}}{R_{ON} \times C_{ON}} \quad (18)$$

3. SET AVERAGE LED CURRENT

   The average LED current (I_{LED}) is set by:

$$I_{LED} = \frac{V_{IADJ}}{10 \times R_{CS}}$$

$$V_{IADJ} = V_{REF} \times \frac{R_{IADJ2}}{R_{IADJ1} + R_{IADJ2}}$$

$$V_{REF} = 3.03V \quad (19)$$

4. SET INDUCTOR RIPPLE CURRENT

   First, the expected duty cycle, D needs to be determined:

$$D = \frac{V_{OUT}}{\eta \times V_{IN}} \qquad \eta \text{ : expected efficiency} \quad (20)$$

   With the inductor ripple current, $\Delta i_{L\text{-}PP}$ specified and the expected duty cycle, the inductance (L) can be chosen:

$$L = \frac{(V_{IN} - V_{OUT}) \times D}{\Delta i_{L-PP} \times f_{SW}} \quad (21)$$

5. SET LED RIPPLE CURRENT AND DETERMINE OUTPUT CAPACITANCE, C_{OUT}

The LED ripple current (Δi_{LED-PP}) is specified. With the target ripple current determined, the output capacitance (C_{OUT}) can be chosen as follows:

$$C_{OUT} = \frac{\Delta i_{L-PP}}{8 \times f_{SW} \times r_D \times \Delta i_{LED-PP}} \quad (22)$$

6. CHOOSE N-CHANNEL MOSFETS

The suggested minimum voltage rating, V_{T-MAX} and current rating, I_{T-MAX} are:

$$V_{T-MAX} = 1.2 \times V_{IN-MAX}$$

$$I_{T-MAX} = 1.5 \times D_{MAX} \times I_{LED} \quad (23)$$

Selecting a proper power MOSFET is critical in a power application, other than the SOA limits, the gate characteristic and the R_{DSON} can affect the system performance seriously.

Also, the peak current limit (I_{LIMIT}) is governed by:

$$I_{LIMIT} \approx \frac{1.28V}{R_{DSON}} \qquad V_{IN} = 85V, \text{ at room temperature} \quad (24)$$

Both the current limit threshold and MOSFET R_{DSON} are loosely specified and can vary a lot with temperature, input voltage and other operating conditions.

7. CHOOSE INPUT CAPACITANCE

Input capacitance is necessary to provide instantaneous current to the discontinuous portions of the circuit during the high side NFET on-time. The allowable input voltage ripple (Δv_{IN-PP}) is specified at approximately 3% Pk-Pk of V_{IN}. The minimum required capacitance (C_{IN_MIN}) to achieve this specification is:

$$C_{IN\_MIN} = \frac{I_{LED} \times D}{\Delta v_{IN-PP} \times f_{SW}} \quad (25)$$

The necessary RMS input current rating (I_{IN-RMS}) can be approximated as follows:

$$I_{IN-RMS} = I_{LED} \times \sqrt{D \times (1-D)} \quad (26)$$

8. SET THE TURN-ON VOLTAGE AND UNDER-VOLTAGE LOCKOUT HYSTERESIS

With the desired turn-on threshold voltage (V_{TURN_ON}) stated, the resistor divider network composing with R_{UDIM1} and R_{UDIM2} can be calculated with the equation in below.

$$V_{TURN\_ON} = 1.276V \times \left(\frac{R_{UDIM1} + R_{UDIM2}}{R_{UDIM2}} \right)$$

$$R_{UDIM2} = \frac{1.276V \times R_{UDIM1}}{V_{TURN\_ON} - 1.276V} \quad (27)$$

Then R_{UDIM3} is optional and recommended for PWM. The R_{UDIM3} can be calculated based on to provide the desired under-voltage lockout hysteresis (V_{HYS}).

TYPICAL APPLICATION CIRCUITS

TPS92640 - Precision Analog Dimming Application

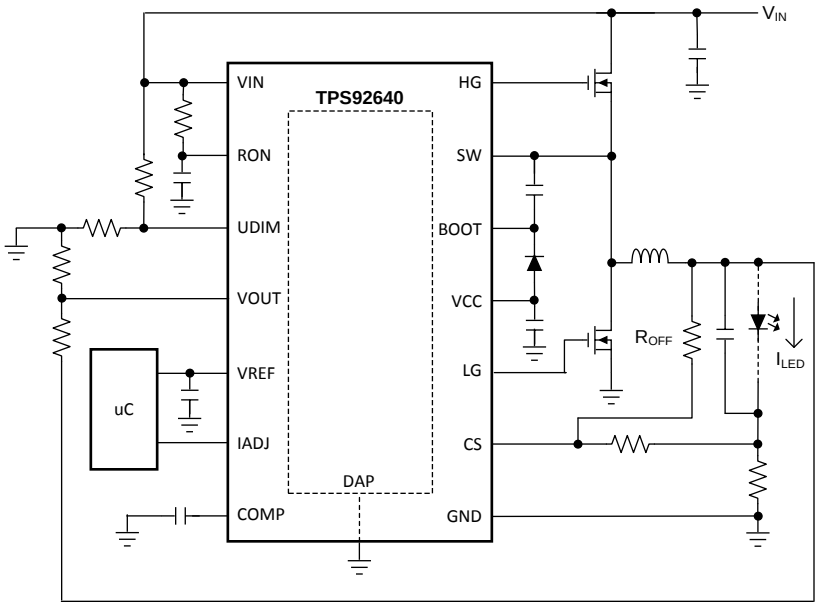


Figure 23. Percision analog dimming circuit using an external micro-controller and TPS92640.

TPS92640 – PWM Dimming Application with Thermal Fold-back

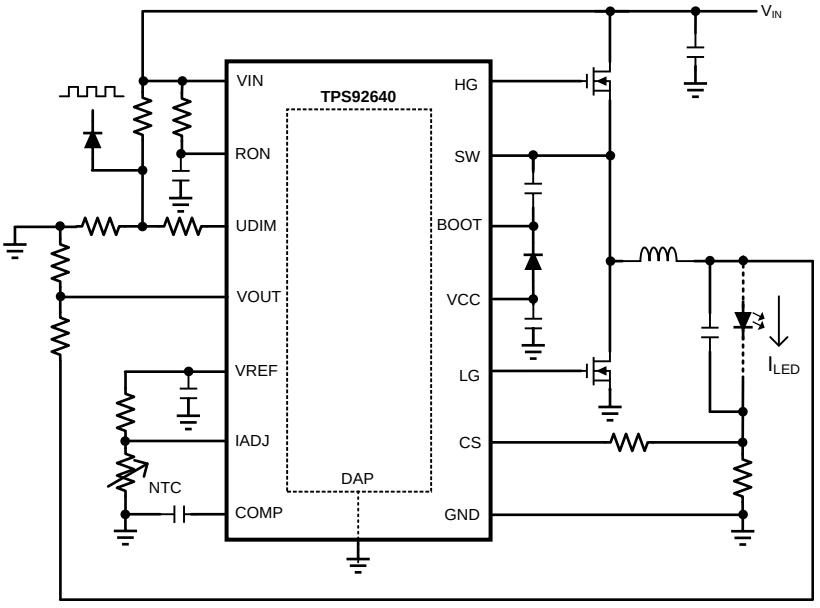


Figure 24. PWM dimming using UDIM pin.

TPS92641 – Shunt FET PWM Dimming Application

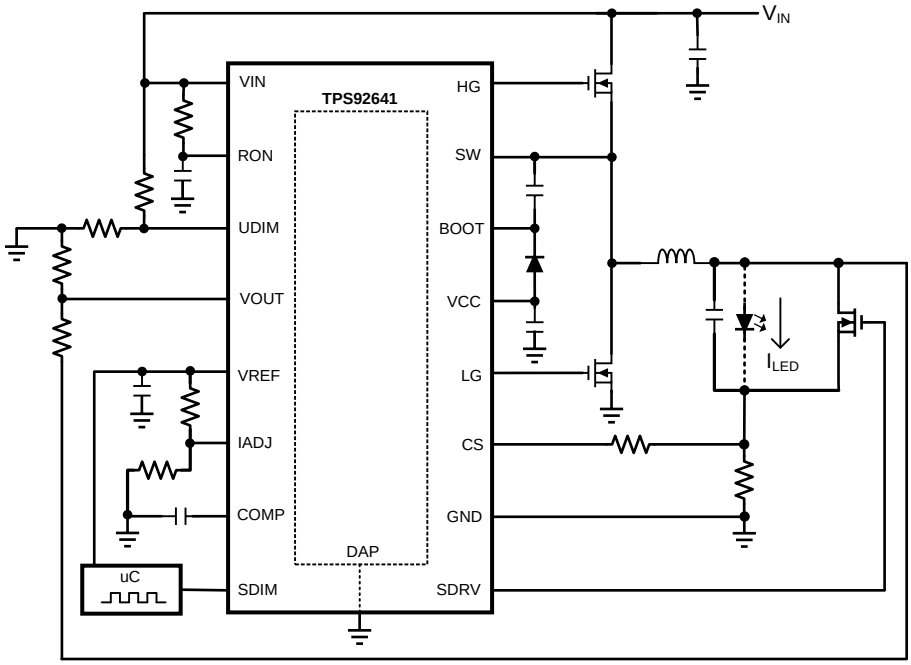


Figure 25. Shunt FET dimming circuit using TPS92641.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92640PWP/NOPB	ACTIVE	HTSSOP	PWP	14	94	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	TP92640 PWP	Samples
TPS92640PWPR/NOPB	ACTIVE	HTSSOP	PWP	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	TP92640 PWP	Samples
TPS92640PWPT/NOPB	ACTIVE	HTSSOP	PWP	14	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	TP92640 PWP	Samples
TPS92641PWP/NOPB	ACTIVE	HTSSOP	PWP	16	92	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	TP92641 PWP	Samples
TPS92641PWPR/NOPB	ACTIVE	HTSSOP	PWP	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	TP92641 PWP	Samples
TPS92641PWPT/NOPB	ACTIVE	HTSSOP	PWP	16	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	TP92641 PWP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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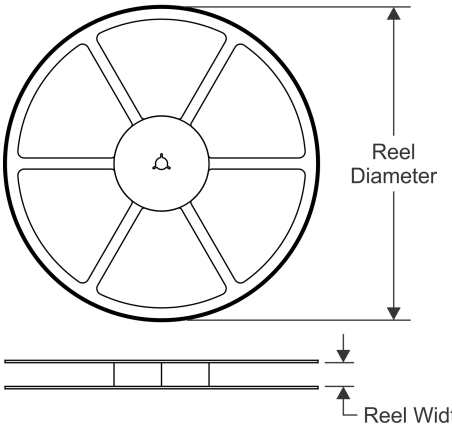
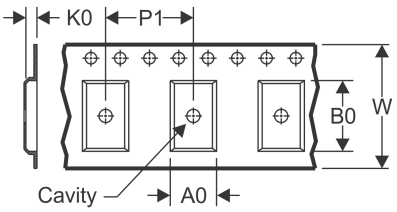
TAPE AND REEL INFORMATION

REEL DIMENSIONS

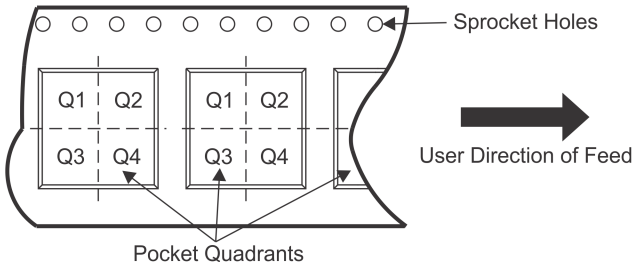


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

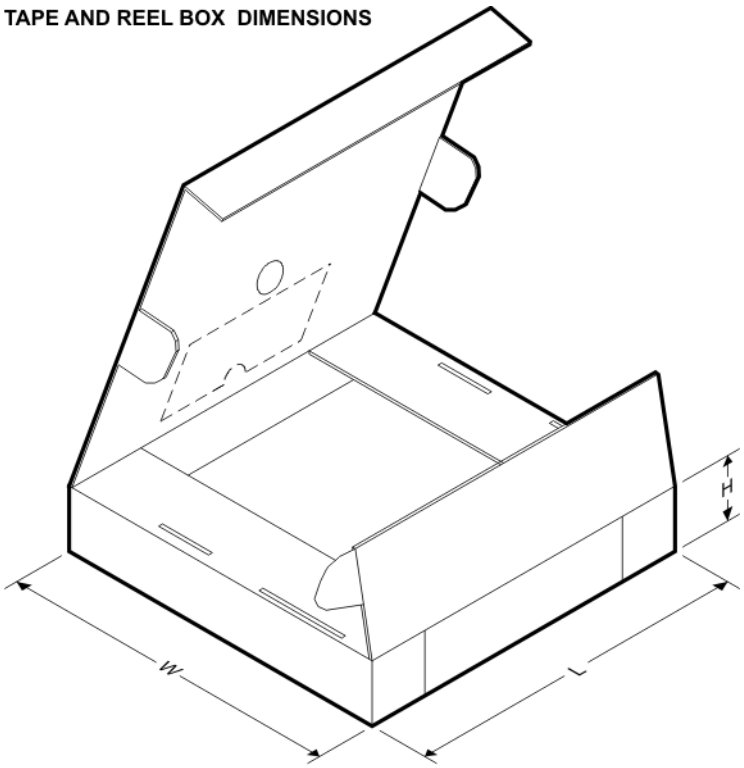
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92640PWPR/NOPB	HTSSOP	PWP	14	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
TPS92640PWPT/NOPB	HTSSOP	PWP	14	250	178.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
TPS92641PWPR/NOPB	HTSSOP	PWP	16	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
TPS92641PWPT/NOPB	HTSSOP	PWP	16	250	178.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1

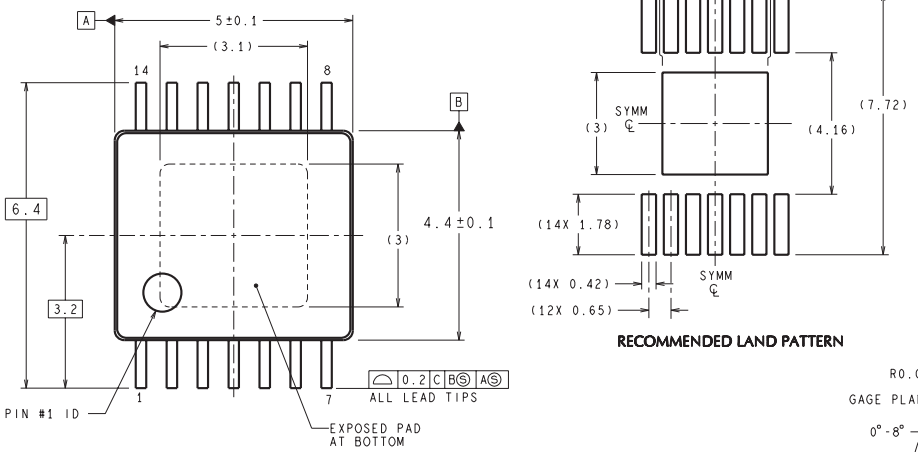
TAPE AND REEL BOX DIMENSIONS



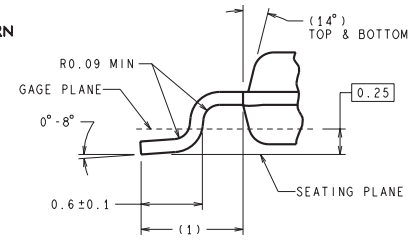
*All dimensions are nominal

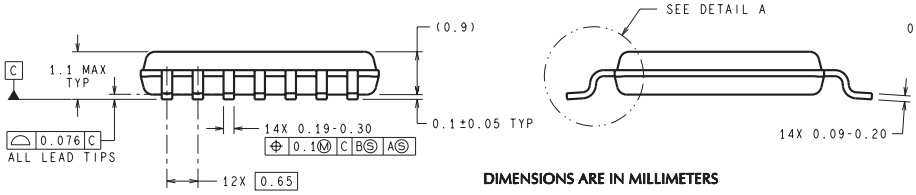
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92640PWPR/NOPB	HTSSOP	PWP	14	2500	367.0	367.0	35.0
TPS92640PWPT/NOPB	HTSSOP	PWP	14	250	203.0	190.0	41.0
TPS92641PWPR/NOPB	HTSSOP	PWP	16	2500	367.0	367.0	35.0
TPS92641PWPT/NOPB	HTSSOP	PWP	16	250	203.0	190.0	41.0

PWP0014A



RECOMMENDED LAND PATTERN





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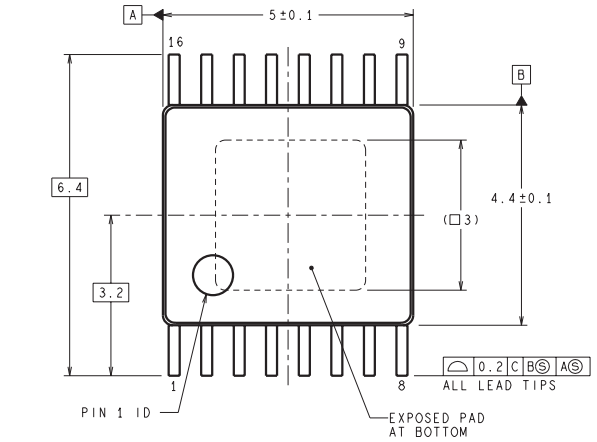
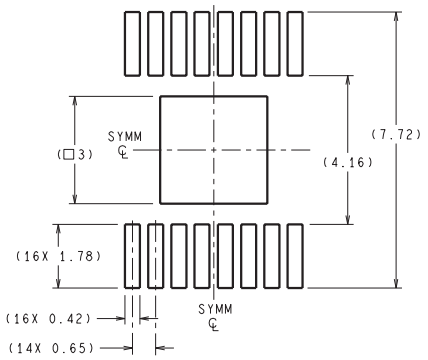
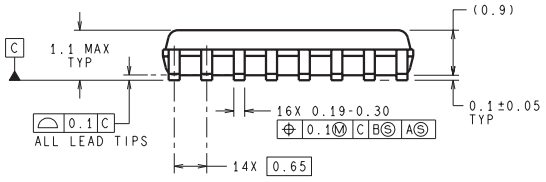
MXA14A (Rev A)

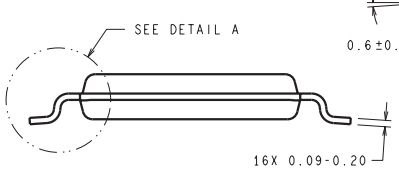
PWP0016A

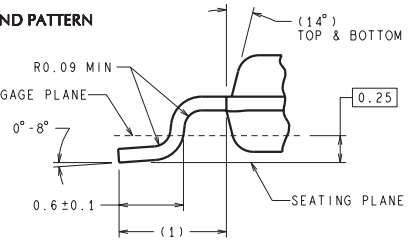




RECOMMENDED LAND PATTERN







DETAIL A
TYPICAL

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