

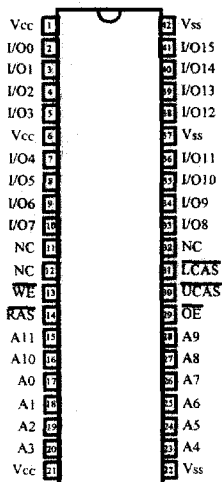


Description

The GM71C(S)16163C/CL is the new generation dynamic RAM organized 1,048,576 x 16 bit. GM71C(S)16163C/CL has realized higher density, higher performance and various functions by utilizing advanced CMOS process technology. The GM71C(S)16163C/CL offers Extended Data out(EDO) Mode as a high speed access mode. Multiplexed address inputs permit the GM71C(S)16163C/CL to be packaged in standard 400 mil 42pin plastic SOJ, and standard 400mil 44(50)pin plastic TSOP II. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

Pin Configuration

42 SOJ



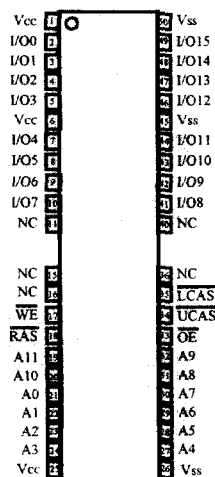
Features

- 1,048,576 Words x 16 Bit Organization
- Extended Data Out Mode Capability
- Single Power Supply (5V ± 10%)
- Fast Access Time & Cycle Time (Unit: ns)

	t _{TRAC}	t _{CAC}	t _{RC}	t _{HPC}
GM71C(S)16163C/CL-5	50	13	84	20
GM71C(S)16163C/CL-6	60	15	104	25
GM71C(S)16163C/CL-7	70	18	124	30
GM71C(S)16163C/CL-8	80	20	144	35

- Low Power
 Active : 605/550/495/400mW (MAX)
 Standby : 11mW (MAX)
 0.83mW (L-series : MAX)
- $\overline{\text{RAS}}$ Only Refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh, Hidden Refresh Capability
- All inputs and outputs TTL Compatible
- 4096 Refresh Cycles/64ms
- 4096 Refresh Cycles/128ms (L-series)
- Self Refresh Operation (L-version)
- Battery Back Up Operation (L-series)
- 2 CAS byte Control

44(50) TSOP II



(Top View)

Pin Description

Pin	Function	Pin	Function
A0-A11	Address Inputs	\overline{WE}	Write Enable
A0-A11	Refresh Address Inputs	\overline{OE}	Output Enable
I/O0-I/O15	Data-In/Out	V _{cc}	Power (+5V)
\overline{RAS}	Row Address Strobe	V _{ss}	Ground
\overline{CAS}	Column Address Strobe	NC	No Connection

Ordering Information

Type No.	Access Time	Package
GM71C(S)16163CJ/CLJ -5 GM71C(S)16163CJ/CLJ -6 GM71C(S)16163CJ/CLJ -7 GM71C(S)16163CJ/CLJ -8	50ns 60ns 70ns 80ns	400 Mil 42 Pin Plastic SOJ
GM71C(S)16163CT/CLT -5 GM71C(S)16163CT/CLT -6 GM71C(S)16163CT/CLT -7 GM71C(S)16163CT/CLT -8	50ns 60ns 70ns 80ns	400 Mil 44(50) Pin Plastic TSOP II (Normal Type)

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T _A	Ambient Temperature under Bias	0 ~ +70	°C
T _{STG}	Storage Temperature	-55 ~ +125	°C
V _T	Voltage on any Pin Relative to V _{ss}	-1.0 ~ +7.0V	V
V _{CC}	Supply voltage Relative to V _{ss}	-1.0 ~ +7.0V	V
I _{OUT}	Short Circuit Output Current	50	mA
P _T	Power Dissipation	1.0	W

Recommended DC Operating Conditions (T_A = 0 ~ +70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.4	-	6.0	V
V _{IL}	Input Low Voltage	-1.0	-	0.8	V

*Note: All voltage referred to V_{ss}.

Truth Table

$\overline{\text{RAS}}$	$\overline{\text{LCAS}}$	$\overline{\text{UCAS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Output	Operation		Notes
H	D	D	D	D	Open	Standby		1,3
L	L	H	H	L	Valid	Lower byte	Read cycle	1,3
L	H	L	H	L	Valid	Upper byte		
L	L	L	H	L	Valid	Word		
L	L	H	L	D	Open	Lower byte	Early write cycle	1,2,3
L	H	L	L	D	Open	Upper byte		
L	L	L	L	D	Open	Word		
L	L	H	L	H	Undefined	Lower byte	Delayed Write cycle	1,2,3
L	H	L	L	H	Undefined	Upper byte		
L	L	L	L	H	Undefined	Word		
L	L	H	H to L	L to H	Valid	Lower byte	Read-modify-write cycle	1,3
L	H	L	H to L	L to H	Valid	Upper byte		
L	L	L	H to L	L to H	Valid	Word		
H to L	H	L	D	D	Open	Word	CBR Refresh or Self Refresh (L-series)	1,3
H to L	L	H	D	D	Open	Word		
H to L	L	L	D	D	Open	Word		
L	H	H	D	D	Open	Word	LAS-only Refresh cycle	1,3
L	L	L	H	H	Open	Read cycle (Output disabled)		1,3

Notes: 1. H: High (inactive) L: Low(active) D: H or L

2. $t_{wcs} \geq 0ns$ Early write cycle

$t_{wcs} < 0ns$ Delayed write cycle

3. Mode is determined by the OR function of the $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$. (Mode is set by earliest of $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ active edge and reset by the latest of $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ inactive edges.) However write OPERATION and output HIZ control are done independently by each $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$.
ex. if $\overline{\text{RAS}} = \text{H to L}$, $\overline{\text{UCAS}} = \text{H}$, $\overline{\text{LCAS}} = \text{L}$, then CAS-before-RAS refresh cycle is selected.

DC Electrical Characteristics ($V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_A = 0 \sim 70^\circ C$)

Symbol	Parameter	Min	Max	Unit	Note	
V_{OH}	Output Level Output "H" Level Voltage ($I_{OUT} = -2mA$)	2.0	V_{CC}	V		
V_{OL}	Output Level Output "L" Level Voltage ($I_{OUT} = 2mA$)	0	0.4	V		
I_{CC1}	Operating Current Average Power Supply Operating Current (RAS, CAS Cycling: $t_{RC} = t_{RC \min}$)	50ns	-	110	mA	1, 2
		60ns	-	100		
		70ns	-	90		
		80ns	-	80		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current (RAS, CAS = V_{IH} , DOUT = High-Z)	-	2	mA		
I_{CC3}	RAS Only Refresh Current Average Power Supply Current RAS Only Refresh Mode ($t_{RC} = t_{RC \min}$)	50ns	-	110	mA	2
		60ns	-	100		
		70ns	-	90		
		80ns	-	80		
I_{CC4}	EDO Page Mode Current Average Power Supply Current EDO Page Mode ($t_{RPC} = t_{RPC \min}$)	50ns	-	105	mA	1, 3
		60ns	-	95		
		70ns	-	85		
		80ns	-	75		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current (RAS, CAS > $V_{CC} - 0.2V$, DOUT = High-Z)	-	1	mA		
		-	150	uA	5	
I_{CC6}	CAS-before-RAS Refresh Current ($t_{RC} = t_{RC \min}$)	50ns	-	110	mA	
		60ns	-	100		
		70ns	-	90		
		80ns	-	80		
I_{CC7}	Standby Current $\overline{RAS} = V_{IH}$ $\overline{CAS} = V_{IL}$ DOUT = Enable	-	5	mA	1	
I_{CC8}	Battery Back Up Operating Current(Standby with CBR Ref.) (CBR refresh, $t_{RC} = 31.3\mu s$, $t_{RAS} \leq 0.3\mu s$, DOUT=High-Z, CMOS interface)	-	500	uA	4,5	
I_{CC9}	Self-Refresh Mode Current ($\overline{RAS}, \overline{CAS} \leq 0.2V$, DOUT=High-Z, CMOS interface)	-	300	uA	5	
I_{IU}	Input Leakage Current Any Input ($0V \leq V_{IN} \leq 6V$)	-10	10	uA		
I_{IO}	Output Leakage Current (DOUT is Disabled, $0V \leq V_{OUT} \leq 6V$)	-10	10	uA		

Note: 1. I_{CC} depends on output load condition when the device is selected. $I_{CC}(\max)$ is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.
3. Address can be changed once or less while $\overline{CAS} = V_{IH}$.
4. $\overline{CAS} = L$ ($\leq 0.2V$) while $\overline{RAS} = L$ ($\leq 0.2V$).
5. L - Series.

Capacitance ($V_{CC} = 5V \pm 10\%$, $T_A = 25^\circ C$)

Symbol	Parameter	Min	Max	Unit	Note
C _{I1}	Input Capacitance (Address)	-	5	pF	1
C _{I2}	Input Capacitance (Clocks)	-	7	pF	1
C _{I/O}	Output Capacitance (Data-In/Out)	-	7	pF	1, 2

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $CAS = V_{IH}$ to disable D_{OUT}.

AC Characteristics ($V_{CC} = 5V \pm 10\%$, $T_A = 0 \sim +70^\circ C$, $V_{SS} = 0V$) Note 1, 2, 18, 19, 20

Test Conditions

Input rise and fall times : 2 ns

Output load : 1TTL gate + C_L (100 pF)

Input timing reference levels : 0.8V, 2.4V

(Including scope and jig)

Output timing reference levels : 0.8V, 2.0V

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GM71C(S)16163 C/CL-5		GM71C(S)16163 C/CL-6		GM71C(S)16163 C/CL-7		GM71C(S)16163 C/CL-8		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t _{RC}	Random Read or Write Cycle Time	84	-	104	-	124	-	144	-	ns	
t _{RP}	RAS Precharge Time	30	-	40	-	50	-	60	-	ns	
t _{CP}	CAS Precharge Time	7	-	10	-	13	-	15	-	ns	
t _{RAS}	RAS Pulse Width	50	10,000	60	10,000	70	10,000	80	10,000	ns	
t _{CAS}	CAS Pulse Width	7	10,000	10	10,000	13	10,000	15	10,000	ns	
t _{ASR}	Row Address Set up Time	0	-	0	-	0	-	0	-	ns	
t _{RAH}	Row Address Hold Time	7	-	10	-	10	-	10	-	ns	
t _{ASC}	Column Address Set-up Time	0	-	0	-	0	-	0	-	ns	21
t _{CAH}	Column Address Hold Time	7	-	10	-	13	-	15	-	ns	21
t _{RCd}	RAS to CAS Delay Time	11	37	14	45	14	52	20	60	ns	3
t _{RAD}	RAS to Column Address Delay Time	9	25	12	30	12	35	15	40	ns	4
t _{RSH}	RAS Hold Time	10	-	13	-	13	-	18	-	ns	
t _{CSH}	CAS Hold Time	35	-	40	-	45	-	50	-	ns	23
t _{CRP}	CAS to RAS Precharge Time	5	-	5	-	5	-	5	-	ns	22
t _{OED}	OE to D _{IN} Delay Time	13	-	15	-	18	-	20	-	ns	5
t _{DZO}	OE Delay Time from D _{IN}	0	-	0	-	0	-	0	-	ns	6
t _{DZC}	CAS Delay Time from D _{IN}	0	-	0	-	0	-	0	-	ns	6
t _T	Transition Time (Rise and Fall)	2	50	2	50	2	50	2	50	ns	7

Read Cycle

Symbol	Parameter	GM71C(S)16163 C/CL-5		GM71C(S)16163 C/CL-6		GM71C(S)16163 C/CL-7		GM71C(S)16163 C/CL-8		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t _{RAC}	Access Time from $\overline{\text{RAS}}$	-	50	-	60	-	70	-	80	ns	8,9
t _{CAC}	Access Time from $\overline{\text{CAS}}$	-	13	-	15	-	18	-	20	ns	9,10,17
t _{AA}	Access Time from Address	-	25	-	30	-	35	-	40	ns	9,11,17
t _{OE}	Access Time from $\overline{\text{OE}}$	-	13	-	15	-	18	-	20	ns	9
t _{RCS}	Read Command Setup Time	0	-	0	-	0	-	0	-	ns	21
t _{RCH}	Read Command Hold Time to $\overline{\text{CAS}}$	0	-	0	-	0	-	0	-	ns	12,22
t _{RRH}	Read Command Hold Time to $\overline{\text{RAS}}$	5	-	5	-	5	-	5	-	ns	12
t _{RAL}	Column Address to $\overline{\text{RAS}}$ Lead Time	25	-	30	-	35	-	40	-	ns	
t _{CAL}	Column Address to $\overline{\text{CAS}}$ Lead Time	15	-	18	-	23	-	28	-	ns	
t _{CLZ}	$\overline{\text{CAS}}$ to Output in Low-Z	0	-	0	-	0	-	0	-	ns	
t _{OH}	Output Data Hold Time	3	-	3	-	3	-	3	-	ns	27
t _{OHO}	Output Data Hold Time from $\overline{\text{OE}}$	3	-	3	-	3	-	3	-	ns	
t _{OFF}	Output Buffer Turn-off Time	-	13	-	15	-	15	-	15	ns	13,27
t _{OEZ}	Output Buffer Turn-off Time to $\overline{\text{OE}}$	-	13	-	15	-	15	-	15	ns	13
t _{CDD}	$\overline{\text{CAS}}$ to D_{IN} Delay Time	13	-	15	-	18	-	20	-	ns	5
t _{RCHR}	Read Command Hold Time from $\overline{\text{RAS}}$	50	-	60	-	70	-	80	-	ns	
t _{OHR}	Output Data hold Time from $\overline{\text{RAS}}$	3	-	3	-	3	-	3	-	ns	27
t _{OFR}	Output Buffer turn off to $\overline{\text{RAS}}$	-	13	-	15	-	15	-	15	ns	27
t _{WEZ}	Output Buffer turn off to $\overline{\text{WE}}$	-	13	-	15	-	15	-	15	ns	
t _{WED}	$\overline{\text{WE}}$ to D_{IN} Delay Time	13	-	15	-	18	-	20	-	ns	
t _{ROD}	$\overline{\text{RAS}}$ to D_{IN} Delay Time	13	-	15	-	18	-	20	-	ns	

Write Cycle

Symol	Parameter	GM71C(S)16163 C/CL-5		GM71C(S)16163 C/CL-6		GM71C(S)16163 C/CL-7		GM71C(S)16163 C/CL-8		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t _{WCS}	Write Command Setup Time	0	-	0	-	0	-	0	-	ns	14,21
t _{WCH}	Write Command Hold Time	7	-	10	-	13	-	15	-	ns	21
t _{WP}	Write Command Pulse Width	7	-	10	-	10	-	10	-	ns	
t _{RWL}	Write Command to $\overline{\text{RAS}}$ Lead Time	7	-	10	-	13	-	15	-	ns	
t _{CWL}	Write Command to $\overline{\text{CAS}}$ Lead Time	7	-	10	-	13	-	15	-	ns	23
t _{DS}	Data-in Setup Time	0	-	0	-	0	-	0	-	ns	15,23
t _{DH}	Data-in Hold Time	7	-	10	-	13	-	15	-	ns	15,23

Read-Modify-Write Cycle

Symbol	Parameter	GM71C(S)16163 C/CL-5		GM71C(S)16163 C/CL-6		GM71C(S)16163 C/CL-7		GM71C(S)16163 C/CL-8		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t _{RWC}	Read-Modify-Write Cycle Time	111	-	136	-	161	-	176	-	ns	
t _{RWD}	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	67	-	79	-	92	-	105	-	ns	14
t _{CWD}	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	30	-	34	-	40	-	44	-	ns	14
t _{AWD}	Column Address to $\overline{\text{WE}}$ Delay Time	42	-	49	-	57	-	64	-	ns	14
t _{OEH}	$\overline{\text{OE}}$ Hold Time from $\overline{\text{WE}}$	13	-	15	-	18	-	20	-	ns	

Refresh Cycle

Symbol	Parameter	GM71C(S)16163 C/CL-5		GM71C(S)16163 C/CL-6		GM71C(S)16163 C/CL-7		GM71C(S)16163 C/CL-8		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t _{CSR}	$\overline{\text{CAS}}$ Setup Time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)	5	-	5	-	5	-	5	-	ns	21
t _{CHR}	$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)	7	-	10	-	10	-	10	-	ns	22
t _{WRP}	$\overline{\text{WE}}$ Setup Time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)	0	-	0	-	0	-	0	-	ns	
t _{WRH}	$\overline{\text{WE}}$ Hold Time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)	10	-	10	-	10	-	10	-	ns	
t _{RPC}	$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Hold Time	5	-	5	-	5	-	5	-	ns	21

EDO Page Mode Cycle

Symbol	Parameter	GM71C(S)16163 C/CL-5		GM71C(S)16163 C/CL-4		GM71C(S)16163 C/CL-7		GM71C(S)16163 C/CL-8		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
tHPC	EDO Page Mode Cycle Time	20	-	25	-	30	-	35	-	ns	25
tRASP	EDO Page Mode RAS Pulse Width	-	100,000	-	100,000	-	100,000	-	100,000	ns	16
tACP	Access Time from $\overline{\text{CAS}}$ Precharge	-	30	-	35	-	40	-	45	ns	9,17,22
tRHCP	RAS Hold Time from CAS Precharge	30	-	35	-	40	-	45	-	ns	
tDOH	Output data Hold Time from $\overline{\text{CAS}}$ low	3	-	3	-	3	-	3	-	ns	9
tCOL	CAS Hold Time referred OE	7	-	10	-	13	-	15	-	ns	
tCOP	$\overline{\text{CAS}}$ to OE Setup Time	5	-	5	-	5	-	5	-	ns	
tRCHP	Read command Hold Time from CAS Precharge	30	-	35	-	40	-	45	-	ns	

EDO Page Mode Read-Modify-Write Cycle

Symbol	Parameter	GM71C(S)16163 C/CL-5		GM71C(S)16163 C/CL-6		GM71C(S)16163 C/CL-7		GM71C(S)16163 C/CL-8		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
tHPRWC	EDO Page Mode Read-Modify-Write Cycle Time	57	-	68	-	79	-	88	-	ns	
tCPW	$\overline{\text{WE}}$ Delay Time from CAS Precharge	45	-	54	-	62	-	69	-	ns	14,22

Refresh

Symbol	Parameter	GM71C(S)1616 C/CL-5		GM71C(S)1616 C/CL-6		GM71C(S)1616 C/CL-7		GM71C(S)1616 C/CL-8		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
tREF	Refresh period	-	64	-	64	-	64	-	64	ms	4096 cycles
tREF	Refresh period (L-Series)	-	128	-	128	-	128	-	128	ms	4096 cycles

Self Refresh Mode (L-version)

Symbol	Parameter	GM71C(S)16163 C/CL-5		GM71C(S)16163 C/CL-6		GM71C(S)16163 C/CL-7		GM71C(S)16163 C/CL-8		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t _{RASS}	RAS Pulse Width(Self-Refresh)	100	-	100	-	100	-	100	-	us	29
t _{RPS}	RAS Precharge Time(Self-Refresh)	90	-	110	-	130	-	150	-	ns	
t _{CHS}	CAS Hold Time(Self-Refresh)	-50	-	-50	-	-50	-	-50	-	ns	

Notes:

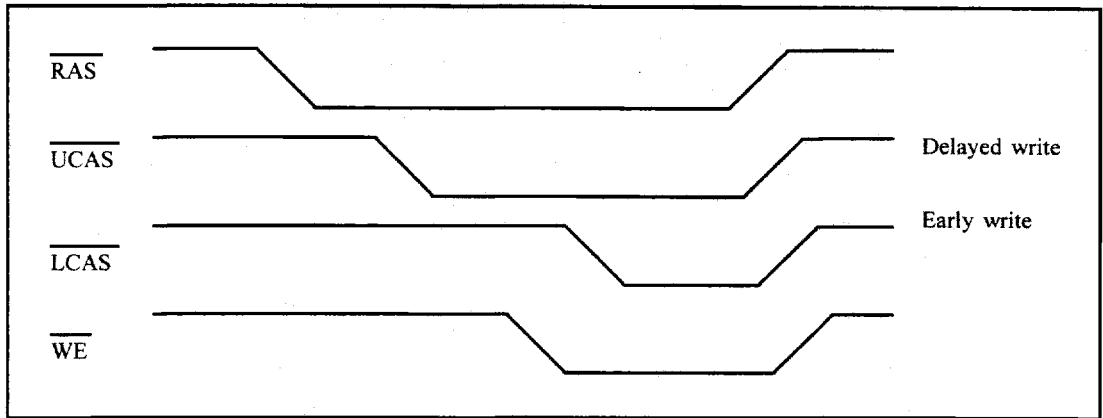
1. AC measurements assume $t_T = 5ns$.
2. An initial pause of 200us is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing RAS-only refresh or CAS-before-RAS refresh). If the internal refresh counter is used, a minimum of eight CAS-before-RAS refresh cycles are required.
3. Operation with the $t_{RCD}(max)$ limit insures that $t_{RAC}(max)$ can be met, $t_{RCD}(max)$ is specified as a reference point only; if $t_{RCD} \geq t_{RAD}(max) + t_{AA}(max) - t_{CAC}(max)$, then access time is controlled exclusively by t_{CAC} .
4. Operation with the $t_{RAD}(max)$ limit insures that $t_{RAC}(max)$ can be met, $t_{RAD}(max)$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, then access time is controlled exclusively by t_{AA} .
5. Either t_{OED} or t_{CDD} must be satisfied.
6. Either t_{DZO} or t_{DZC} must be satisfied.
7. $V_{IH}(min)$ and $V_{IL}(max)$ are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{IH}(min)$ and $V_{IL}(max)$.
8. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
9. Measured with a load circuit equivalent to 1 TTL load and 100pF.
10. Assumes that $t_{RCD} \geq t_{RCD}(max)$ and $t_{RCD} + t_{CAC}(max) \geq t_{RAD} + t_{AA}(max)$.
11. Assumes that $t_{RAD} \geq t_{RAD}(max)$ and $t_{RCD} + t_{CAC}(max) \leq t_{RAD} + t_{AA}(max)$.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
13. $t_{OFF}(max)$ and $t_{OEZ}(max)$ define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPW} are not restrictive operationing parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}(min)$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle ; if $t_{RWD} \geq t_{RWD}(min)$, $t_{CWD} \geq t_{CWD}(min)$, and $t_{AWD} \geq t_{AWD}(min)$, or $t_{CWD} \geq t_{CWD}(min)$, $t_{AWD} \geq t_{AWD}(min)$ and $t_{CPW} \geq t_{CPW}(min)$, the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of data out (at access time) is indeterminate.

15. These parameters are referred to \overline{UCAS} and \overline{LCAS} leading edge in early write cycles and to WE leading edge in delayed write or read-modify-write cycles.
16. t_{RASP} defines \overline{RAS} pulse width in EDO page mode cycles.
17. Access time is determined by the longest among t_{AA} , t_{CAC} , and t_{ACP} .
18. In delayed write or read-modify-write cycles, \overline{OE} must disable output buffer prior to applying data to the device. After \overline{RAS} is reset, if $t_{OEHL} \geq t_{CWL}$, the I/O pin will remain open circuit (high impedance); if $t_{OEHL} < t_{CWL}$, invalid data will be out at each I/O.
19. When both \overline{UCAS} and \overline{LCAS} go low at the same time, all 16-bit data are written into the device. \overline{UCAS} and \overline{LCAS} cannot be staggered within the same write/read cycles.
20. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
21. t_{ASC} , t_{CAH} , t_{RCS} , t_{WCS} , t_{WCH} , t_{CSR} and t_{RPC} are determined by the earlier falling edge of \overline{UCAS} or \overline{LCAS} .
22. t_{CRP} , t_{CHR} , t_{RCH} , t_{ACP} and t_{CPW} are determined by the later rising edge of \overline{UCAS} or \overline{LCAS} .
23. t_{CWL} , t_{DH} , t_{DS} and t_{CSH} should be satisfied by both \overline{UCAS} and \overline{LCAS} .
24. t_{CP} is determined by that time the both \overline{UCAS} and \overline{LCAS} are high.
25. When output buffers are enabled once, sustain the low impedance state until valid data is obtained.
When output buffer is turned on and off within a very short time, generally it causes large V_{CC}/V_{SS} line noise, which causes to degrade $V_{IH \text{ min}}/V_{IL \text{ max}}$ level.
26. Please do not use t_{RASS} timing, $10\mu s \leq t_{RASS} \leq 100\mu s$. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{RASS} \geq 100\mu s$, then \overline{RAS} precharge time should use t_{RPS} instead of t_{RP} .
27. If you use distributed CBR refresh within 15.6us interval in normal read/write cycle, CBR refresh should be executed within 15.6us immediately after exiting from and before entering into self refresh mode.
28. If you use \overline{RAS} only refresh or CBR burst refresh mode in normal read/write cycle, 4096 or 1024 cycles of distributed CBR refresh with 15.6us interval should be executed within 64 or 16ms immediately after exiting from and before entering into the self refresh mode.
29. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.
30. XXXX H or L (H: $V_{IH(\text{min})} \leq V_{IN} \leq V_{IH(\text{max})}$, L: $V_{IL(\text{min})} \leq V_{IN} \leq V_{IL(\text{max})}$)

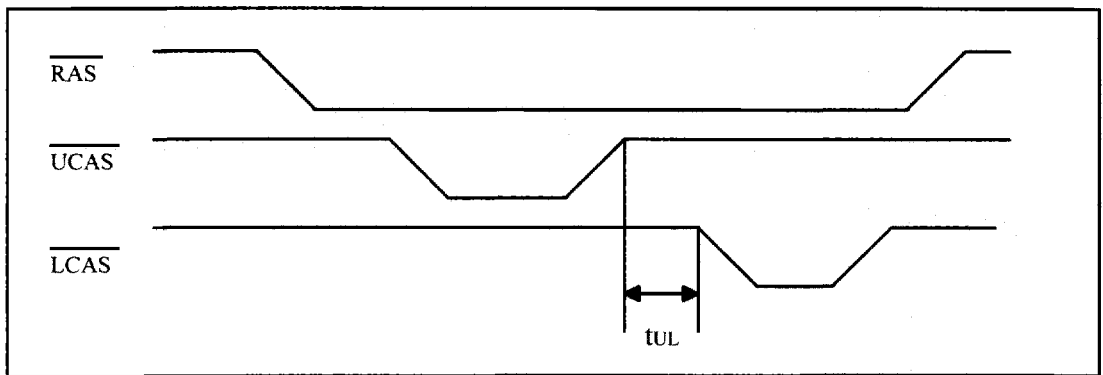
Notes concerning 2CAS control

Please do not separate the $\overline{\text{UCAS}}$ / $\overline{\text{LCAS}}$ operation timing intentionally. However skew between $\overline{\text{UCAS}}$ / $\overline{\text{LCAS}}$ are allowed under the following conditions.

1. Each of the $\overline{\text{UCAS}}$ / $\overline{\text{LCAS}}$ should satisfy the timing specifications individually.
2. Different operation mode for upper/lower byte is not allowed; such as following.



3. Closely separated upper/lower byte control is not allowed. However when the condition ($t_{cp} < t_{UL}$) is satisfied, EDO page mode can be performed.

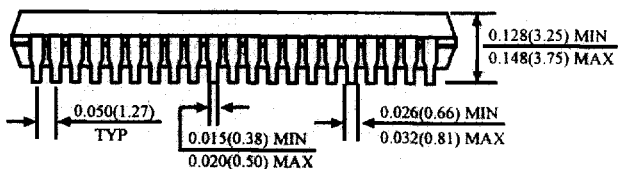
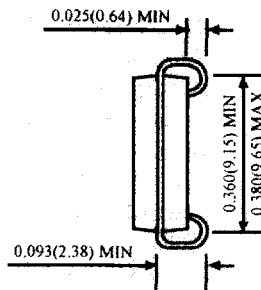
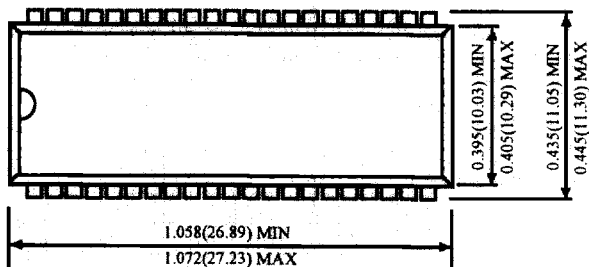


4. Byte control operation by remaining $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ high is guaranteed.

Package Dimensions

Unit : Inches (mm)

42 SOJ



44(50) TSOP (TYPE II)

