

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4043B

MSI

Quadruple R/S latch with 3-state outputs

Product specification
File under Integrated Circuits, IC04

January 1995

Quadruple R/S latch with 3-state outputs

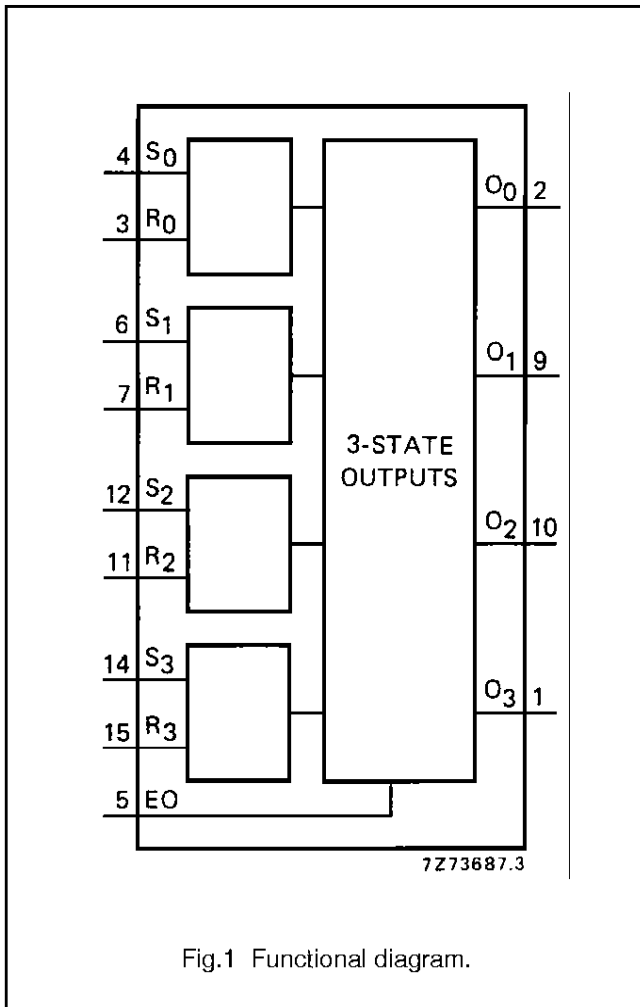
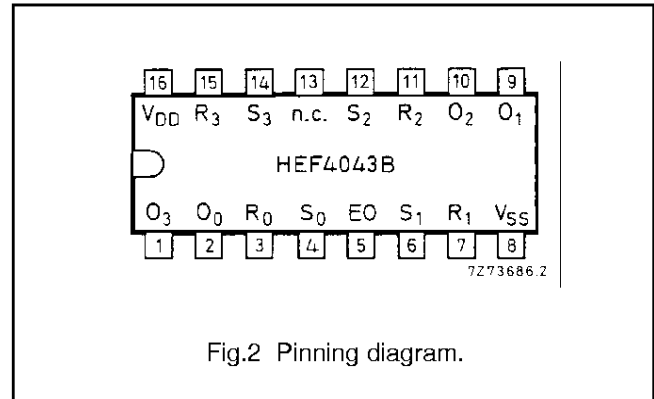
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DESCRIPTION

The HEF4043B is a quadruple R/S latch with 3-state outputs with a common output enable input (EO). Each latch has an active HIGH set input (S₀ to S₃), an active HIGH reset input (R₀ to R₃) and an active HIGH 3-state output (O₀ to O₃).

When EO is HIGH, the state of the latch output (O_n) can be determined from the function table below. When EO is LOW, the latch outputs are in the high impedance OFF-state. EO does not affect the state of the latch.

The high impedance off-state feature allows common busing of the outputs.



- HEF4043BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4043BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4043BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

PINNING

- EO common output enable input
- S₀ to S₃ set inputs (active HIGH)
- R₀ to R₃ reset inputs (active HIGH)
- O₀ to O₃ 3-state buffered latch outputs

FUNCTION TABLE

INPUTS			OUTPUT O _n
EO	S _n	R _n	
L	X	X	Z
H	L	H	L
H	H	X	H
H	L	L	latched

Notes

1. H = HIGH state (the more positive voltage)
- L = LOW state (the less positive voltage)
- X = state immaterial
- Z = high impedance state

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

Quadruple R/S latch with 3-state outputs

HEF4043B
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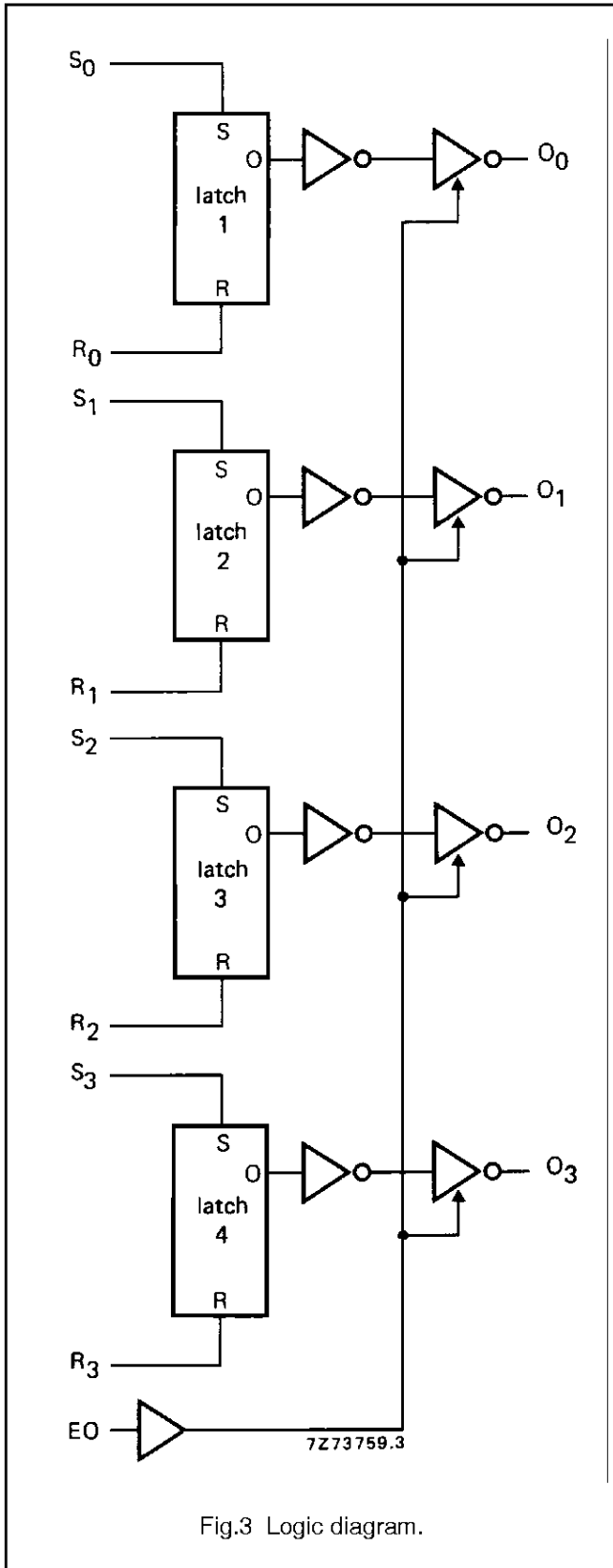


Fig.3 Logic diagram.

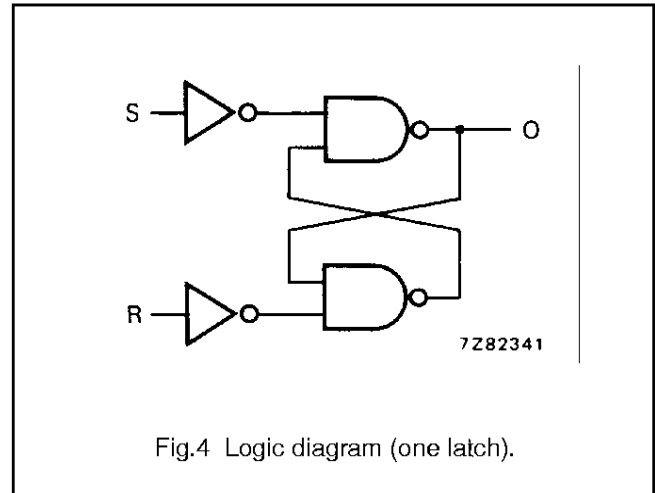


Fig.4 Logic diagram (one latch).

Quadruple R/S latch with 3-state outputs

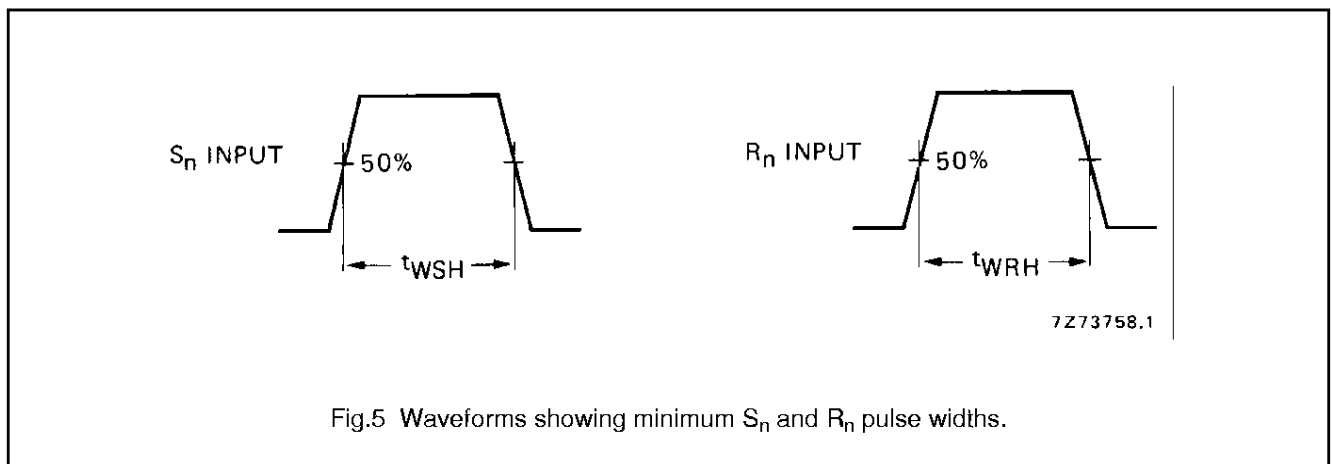
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	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA			
Propagation delays $R_n \rightarrow O_n$ HIGH to LOW	5	t_{PHL}		90	180	ns	$63\text{ ns} + (0,55\text{ ns/pF}) C_L$		
	10			35	70	ns		$24\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15			25	50	ns		$17\text{ ns} + (0,16\text{ ns/pF}) C_L$	
	$S_n \rightarrow O_n$ LOW to HIGH	5	t_{PLH}		65	135	ns	$38\text{ ns} + (0,55\text{ ns/pF}) C_L$	
		10			25	50	ns		$14\text{ ns} + (0,23\text{ ns/pF}) C_L$
		15			15	35	ns		$7\text{ ns} + (0,16\text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	t_{THL}		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$		
	10			30	60	ns		$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15			20	40	ns		$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	
	LOW to HIGH	5	t_{TLH}		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$	
		10			30	60	ns		$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
		15			20	40	ns		$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
3-state propagation delays Output disable times $EO \rightarrow O_n$ HIGH	5	t_{PHZ}		45	90	ns	see also waveforms Fig.5		
	10			20	35	ns			
	15			10	25	ns			
	LOW	5	t_{PLZ}		50	100		ns	
		10			20	40		ns	
		15			10	25		ns	
Output enable times $EO \rightarrow O_n$ HIGH	5	t_{PZH}		25	50	ns			
	10			15	30	ns			
	15			10	25	ns			
	LOW	5	t_{PZL}		40	80	ns		
		10			20	45	ns		
		15			15	35	ns		
Minimum S_n pulse width; HIGH	5	t_{WSH}	30	15		ns			
	10			20	10	ns			
	15			16	8	ns			
Minimum R_n pulse width; HIGH	5	t_{WRH}	30	15		ns			
	10			20	10	ns			
	15			16	8	ns			

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	V _{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5 10 15	1100 f _i + ∑(f _o C _L) × V _{DD} ² 4400 f _i + ∑(f _o C _L) × V _{DD} ² 11 400 f _i + ∑(f _o C _L) × V _{DD} ²	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) ∑(f _o C _L) = sum of outputs V _{DD} = supply voltage (V)



APPLICATION INFORMATION

An example of application for the HEF4043B is:

- Four-bit storage with output enable