

# DATA SHEET

## **PCA9556** Octal SMBus Registered Interface

Product specification

1998 Dec 18

## Octal SMBus Registered Interface

## PCA9556

## FEATURES

- SMBus compliance with fixed 3.3V voltage levels
- Operating power supply voltage range of 3.0V – 3.6V
- Active high polarity inverter register
- Write protect register
- Active low reset pin
- Low leakage current on power-down
- Noise filter on SCL/SDA inputs
- No glitch on power-up
- Internal power-on reset
- 8 I/O pins which default to 8 inputs
- High impedance open drain on I/O

## DESCRIPTION

The PCA9556 is a silicon CMOS circuit which provides parallel input/output expansion for SMBus applications. The PCA9556 consists of an 8-bit input port register, 8-bit output port register, and an SMBus interface. It has low current consumption and a high impedance open drain output pin, I/O0.

The SMBus system master can reset the PCA9556 in the event of a timeout by asserting a LOW on the reset input. The SMBus system master can also invert the PCA9556 inputs by writing to their active HIGH polarity inversion bits. Finally, the SMBus system master can enable the PCA9556's I/Os as either inputs or outputs by writing to their I/O configuration bits.

The power-on reset sets the registers to their default values and initializes the SMBus state machine. The RESET pin causes the same reset/initialization to occur without depowering the part.

## PIN CONFIGURATION

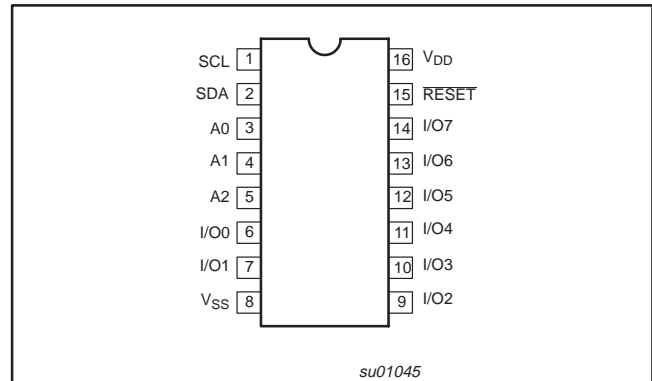


Figure 1. Pin configuration

## PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	SCL	Serial clock line
2	SDA	Serial data line
3	A0	Address input 0
4	A1	Address input 1
5	A2	Address input 2
6	I/O0	I/O0 (open drain)
7	I/O1	I/O1
8	V <sub>SS</sub>	Supply GROUND
9	I/O2	I/O2
10	I/O3	I/O3
11	I/O4	I/O4
12	I/O5	I/O5
13	I/O6	I/O6
14	I/O7	I/O7
15	RESET	External reset (active LOW)
16	V <sub>DD</sub>	Supply voltage

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	DRAWING NUMBER
16-Pin Plastic TSSOP16 Type I	0°C to +70°C	PCA9556 PW	SOT403-1

# Octal SMBus Registered Interface

# PCA9556

## BLOCK DIAGRAM

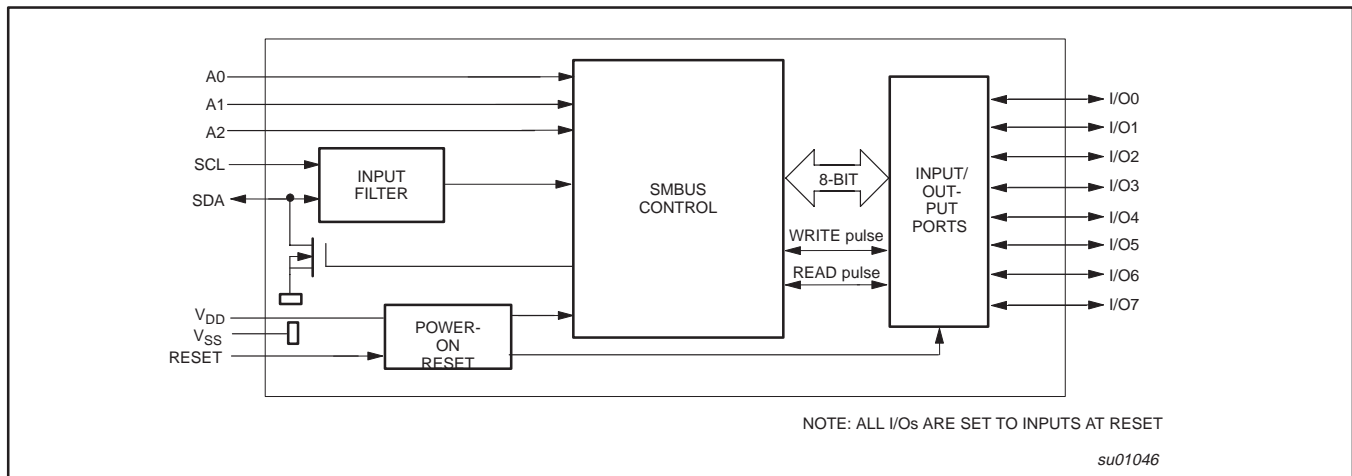


Figure 2. Block diagram

## REGISTERS

### Command Byte

Command	Protocol	Function
0	Read byte	Input port register
1	Read/write byte	Output port register
2	Read/write byte	Polarity inversion register
3	Read/write byte	I/O configuration register

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

### Register 0 – Input Port Register

I7	I6	I5	I4	I3	I2	I1	I0
----	----	----	----	----	----	----	----

This register is an input-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by register 3. Writes to this register have no effect.

### Register 1 – Output Port Register

bit	O7	O6	O5	O4	O3	O2	O1	O0
default	0	0	0	0	0	0	0	0

This register is an output-only port. It reflects the outgoing logic levels of the pins defined as outputs by register 3. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, NOT the actual pin value.

### Register 2 – Polarity Inversion Register

bit	N7	N6	N5	N4	N3	N2	N1	N0
default	1	1	1	1	0	0	0	0

This register enables polarity inversion of pins defined as inputs by register 3. If a bit in this register is set (written with '1'), the corresponding port pin's polarity is inverted. If a bit in this register is cleared (written with a '0'), the corresponding port pin's original polarity is retained.

### Register 3 – Input/Output Configuration Register

bit	C7	C6	C5	C4	C3	C2	C1	C0
default	1	1	1	1	1	1	1	1

This register configures the directions of the I/O pins. If a bit in this register is set (written with '1'), the corresponding port pin is enabled as an input with high impedance output driver. If a bit in this register is cleared (written with '0'), the corresponding port pin is enabled as an output.

## RESET

### Power-on Reset

When power is applied to  $V_{DD}$ , an internal power-on reset holds the PCA9556 in a reset state until  $V_{DD}$  has reached  $V_{POR}$ . At that point, the reset condition is released and the PCA9556 registers and SMBus state machine will initialize to their default states.

### External Reset

A reset can be accomplished by holding the  $\overline{RESET}$  pin low for a minimum of  $T_{W}$ . The PCA9556 registers and SMBus state machine will be held in their default state until the  $\overline{RESET}$  input is once again high. This input contains an internal pull-up, therefore, it may be left open if not used.

# Octal SMBus Registered Interface

# PCA9556

## SIMPLIFIED SCHEMATIC OF I/O0

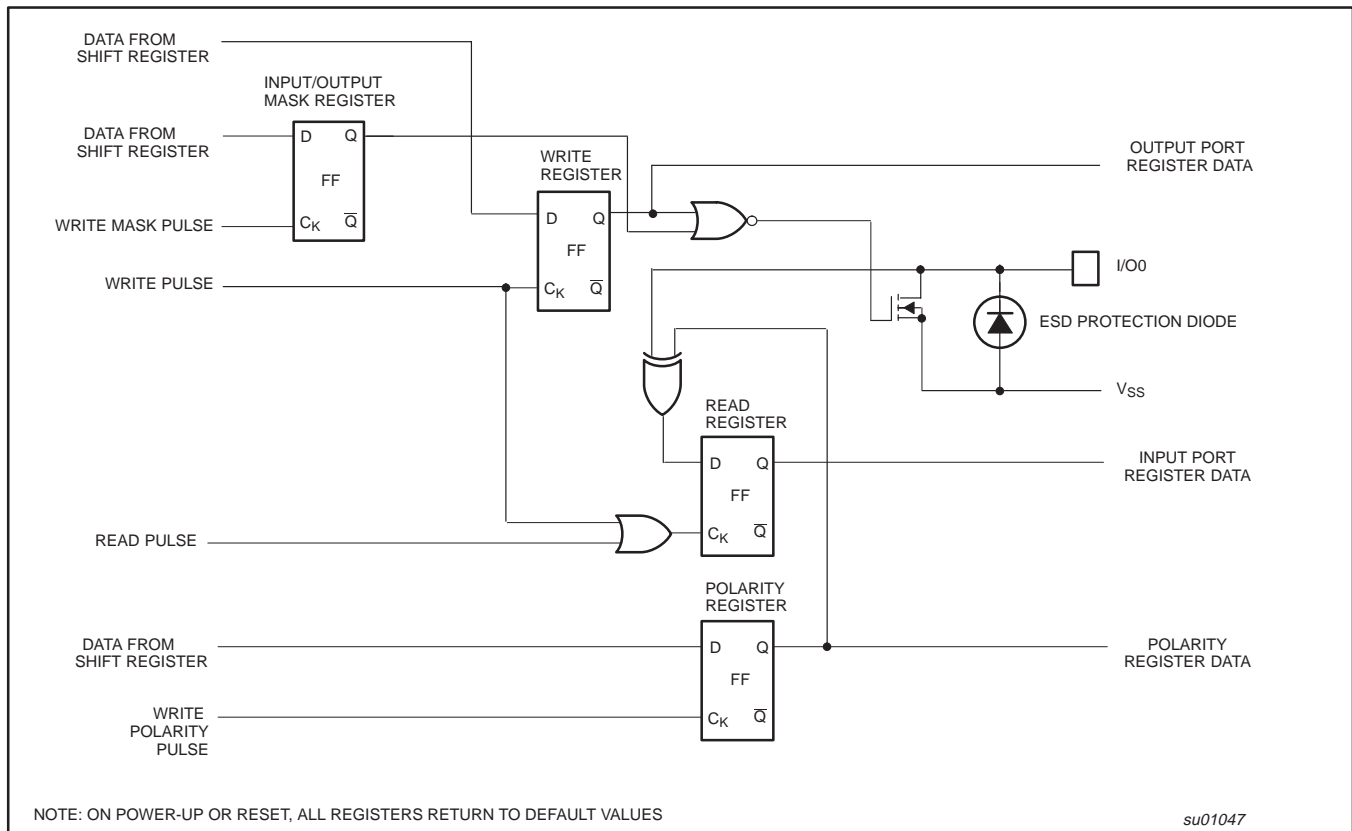


Figure 3. Simplified schematic of I/O0

# Octal SMBus Registered Interface

# PCA9556

## SIMPLIFIED SCHEMATIC OF I/O1 TO I/O7

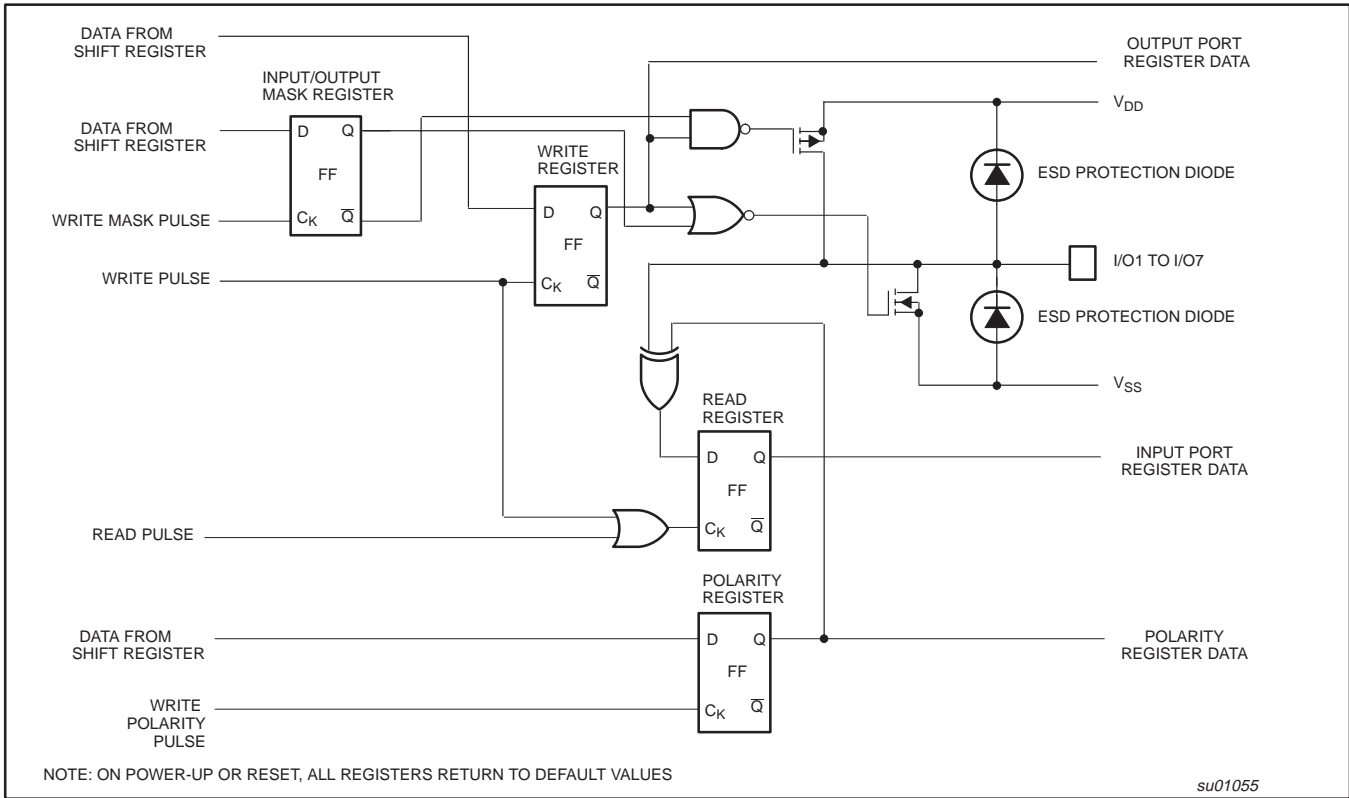


Figure 4. Simplified schematic of I/O1 to I/O7

# Octal SMBus Registered Interface

# PCA9556

## SMBus Address

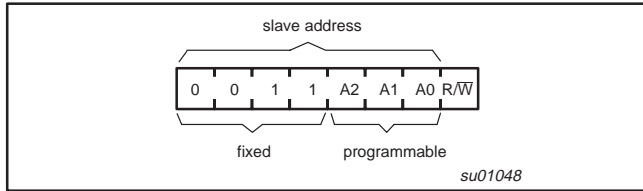


Figure 5. PCA9556 address

## SMBus Transactions

Data is transmitted to the PCA9556 registers using Write Byte transfers (see Figures 6 and 7). Data is read from the PCA9556 registers using Read and Receive Byte transfers (see Figures 8 and 9).

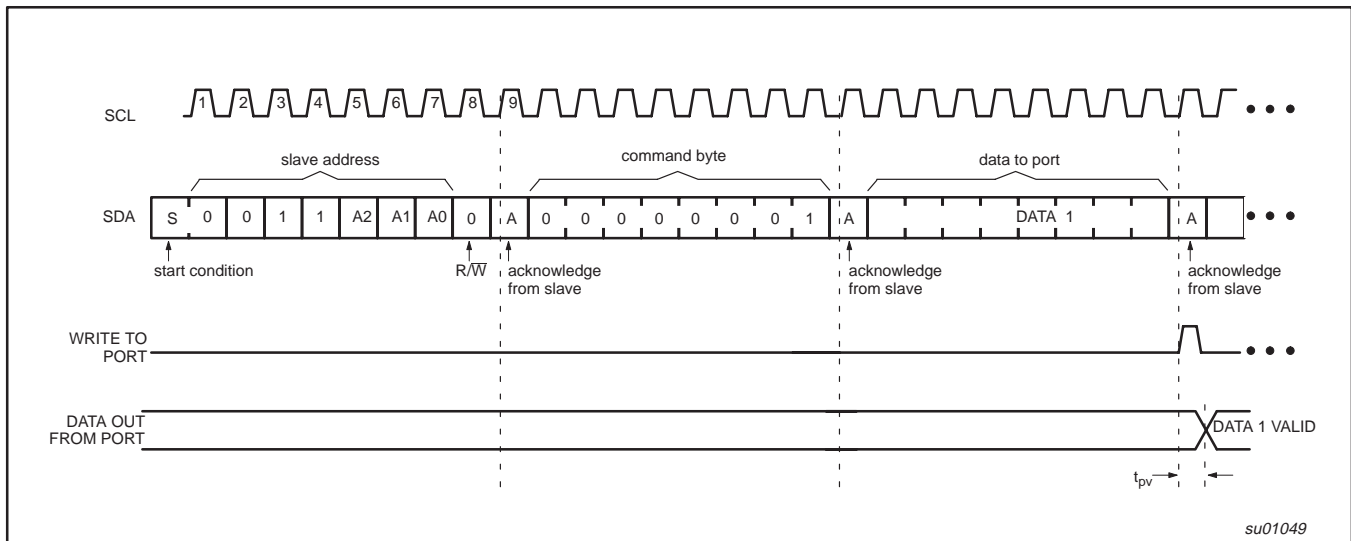


Figure 6. WRITE to output port register via Write Byte Protocol

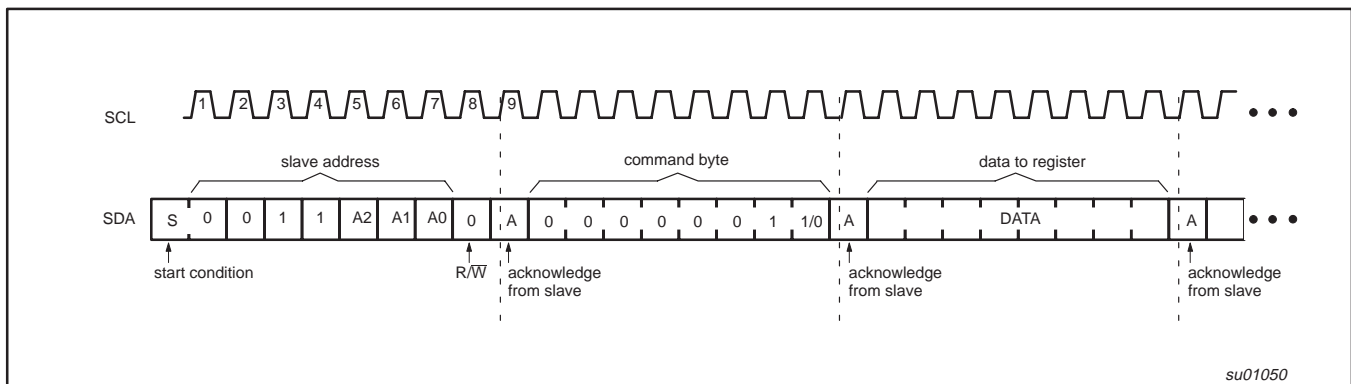
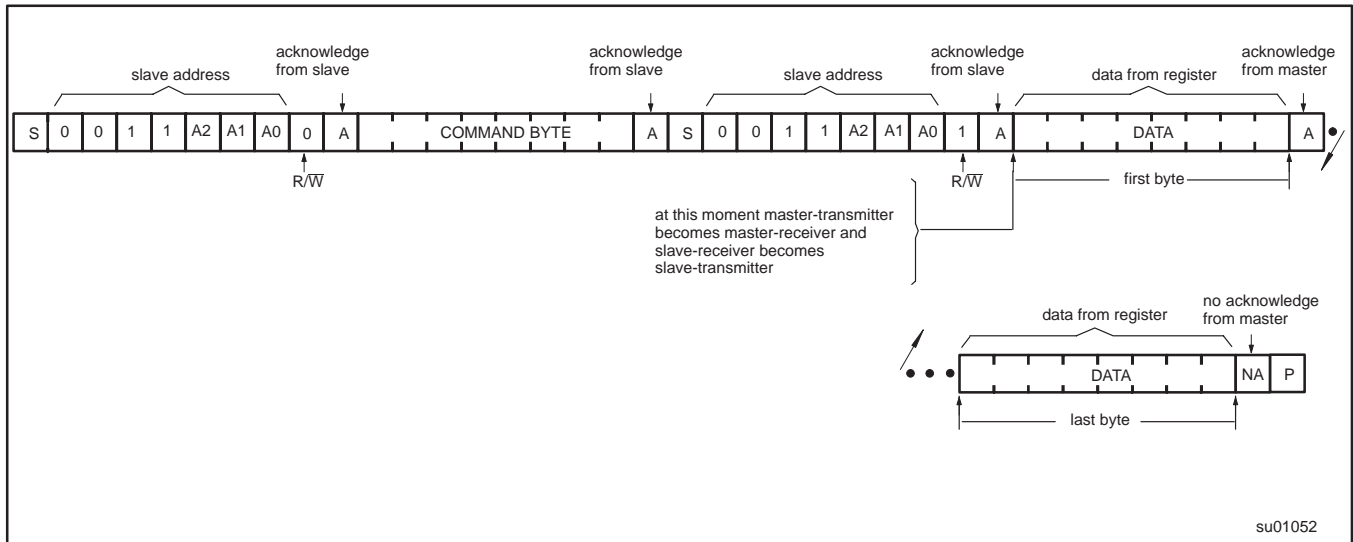


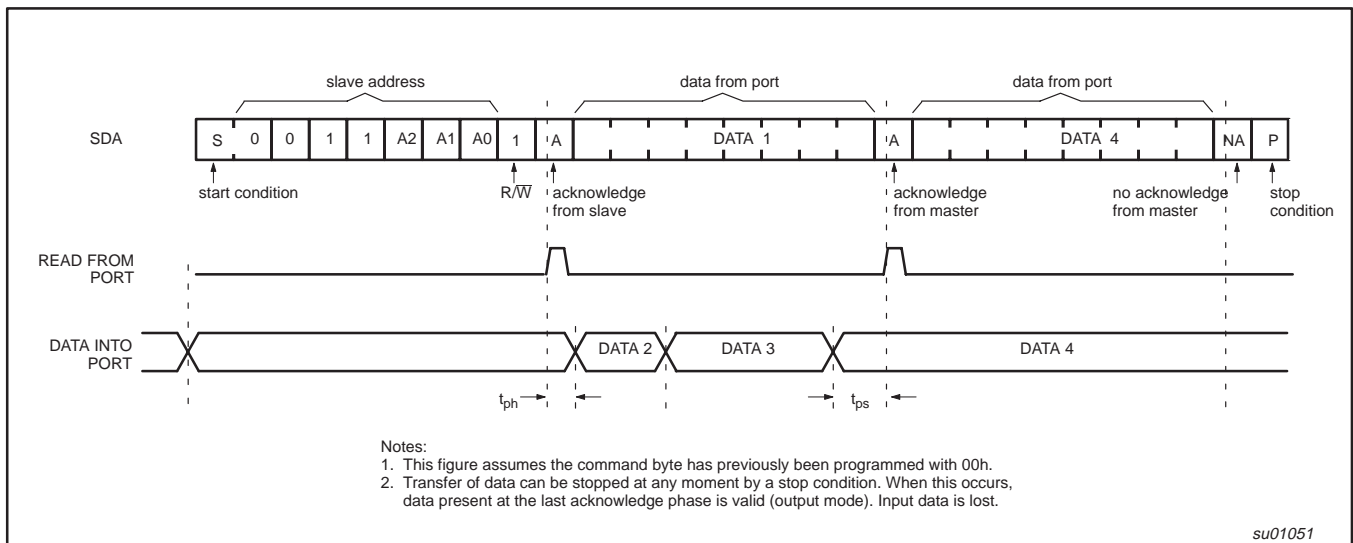
Figure 7. WRITE to I/O configuration or polarity inversion registers via Write Byte Protocol

# Octal SMBus Registered Interface

# PCA9556



**Figure 8. READ from register via Read byte protocol**



**Figure 9. READ input port register via Receive byte protocol**

## Octal SMBus Registered Interface

## PCA9556

**ABSOLUTE MAXIMUM RATINGS**

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
$V_{DD}$	Supply voltage		-0.5	+4.6	V
$V_I$	Input voltage		$V_{SS} - 0.5$	$V_{DD} + 0.5$	V
$I_I$	DC input current		-	$\pm 20$	mA
$V_{I/O}$	DC voltage on an I/O as an input other than I/O0		$V_{SS} - 0.5$	$V_{DD} + 0.5$	V
$V_{I/O0}$	DC voltage on I/O0 as an input		$V_{SS} - 0.5$	4.6	V
$I_{I/O0}$	DC input current on I/O0		-	+400	$\mu$ A
			-	-20	mA
$I_{I/O}$	DC output current on an I/O		-	$\pm 20$	mA
$I_{DD}$	Supply current		-		mA
$I_{SS}$	Supply current		-		mA
$P_{tot}$	Total power dissipation		-		mW
$P_O$	Power dissipation per output		-		mW
$T_{stg}$	Storage temperature range		-65	+150	$^{\circ}$ C
$T_{amb}$	Operating ambient temperature		0	+70	$^{\circ}$ C

**HANDLING**

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC24 under "Handling MOS devices".

**DC CHARACTERISTICS** $V_{DD} = 3.0$  to  $3.6$  V;  $V_{SS} = 0$  V;  $T_{amb} = 0$  to  $+70$   $^{\circ}$ C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
<b>Supplies</b>						
$V_{DD}$	Supply voltage		3.0		3.6	V
$I_{DD}$	Supply current	Operating mode; $V_{DD} = 3.3$ V; no load; $V_I = V_{DD}$ or $V_{SS}$ ; $f_{SCL} = 100$ kHz		300	425	$\mu$ A
$I_{stb}$	Standby current	Standby mode; $V_{DD} = 3.3$ V no load; $V_I = V_{DD}$ or $V_{SS}$		25	50	$\mu$ A
$V_{POR}$	Power-on reset voltage	$V_{DD} = 3.3$ V no load; $V_I = V_{DD}$ or $V_{SS}$ ; note 1		1.3	2.4	V
<b>input SCL; input/output SDA</b>						
$V_{IL}$	LOW level input voltage		-0.5		0.8	V
$V_{IH}$	HIGH level input voltage		2.1		$V_{DD} + 0.5$	V
$I_{OL}$	LOW level output current	$V_{OL} = 0.4$ V	3		-	mA
$I_L$	Leakage current	$V_I = V_{DD} = V_{SS}$	-1		+1	$\mu$ A
$C_I$	Input capacitance	$V_I = V_{SS}$	-		10	pF
<b>I/Os</b>						
$V_{IL}$	LOW level input voltage		-0.5	-	0.8	V
$V_{IH}$	HIGH level input voltage		2.0	-	$V_{DD} + 0.5$	V
$I_{IHL(max)}$	Maximum allowed input current through protection diode (I/O1 – I/O7)	$V_I \geq V_{DD}$ or $V_I \leq V_{SS}$	-	-	$\pm 400$	$\mu$ A
$I_{OL}$	LOW level output current	$V_{OL} = 0.55$ V; $V_{DD} = 3.3$ V	8	10	-	mA
$I_{OH}$	HIGH level output current except I/O0	$V_{OH} = 2.4$ V; $V_{DD} = 3.3$ V	4	-	-	mA
	HIGH level output current on I/O0	$V_{DD} = 3.6$ V; $V_{OH} = 4.6$ V $V_{DD} = 0$ V; $V_{OH} = 3.3$ V		-	1	$\mu$ A
$I_L$	Input leakage current	$V_{DD} = 3.6$ V; $V_I = 0$ or $V_{DD}$	-1		1	$\mu$ A
$C_I$	Input capacitance		-	-	10	pF
$C_O$	Output capacitance		-	-	10	pF
<b>Select Inputs A0, A1, A2, and RESET</b>						
$V_{IL}$	LOW level input voltage		-0.5		0.8	V
$V_{IH}$	HIGH level input voltage		2.0		$V_{DD} + 0.5$	V
$I_{LI}$	Input leakage current		-1		1	$\mu$ A

**NOTE:**

1. The power-on reset circuit resets the SMBus logic with  $V_{DD} < V_{POR}$  and sets all I/Os to their default values



# Octal SMBus Registered Interface

# PCA9556

## AC SPECIFICATIONS

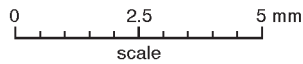
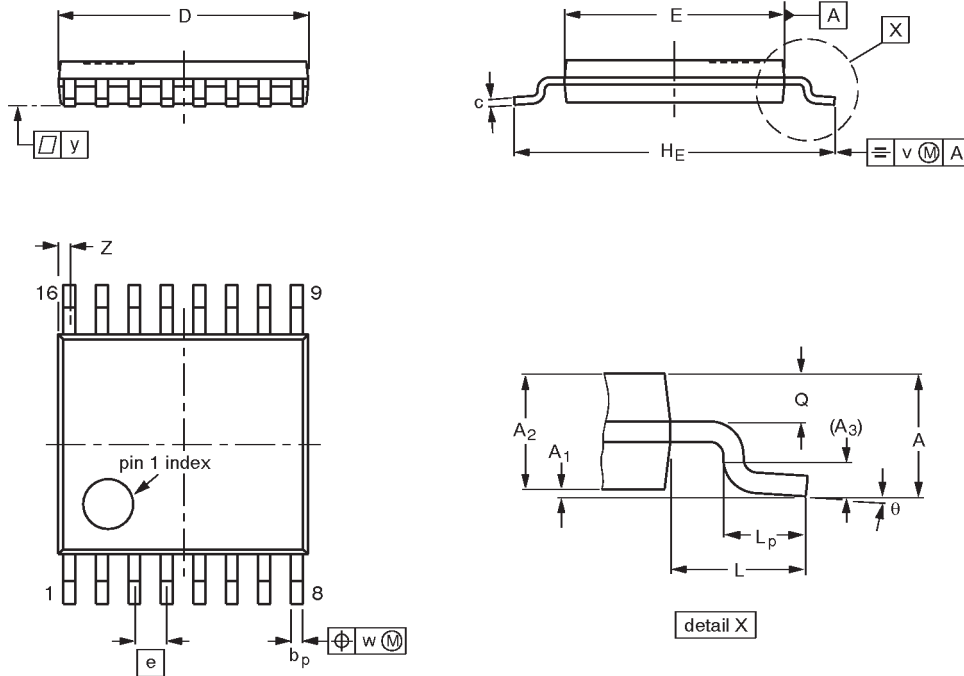
SYMBOL	PARAMETER	LIMITS		UNITS
		MIN	MAX	
F <sub>SBM</sub>	SMB operating frequency	10	100	KHz
T <sub>BUF</sub>	Bus free time between stop and start conditions	4.7		μs
T <sub>HO:STA</sub>	Hold time after (repeated) start condition	4.0		μs
T <sub>SU:STA</sub>	Repeated start condition setup time	4.7		μs
T <sub>HO:DAT</sub>	Data hold time	300		ns
T <sub>SU:DAT</sub>	Data setup time	250		ns
T <sub>LOW</sub>	Clock LOW period	4.7		μs
T <sub>HIGH</sub>	Clock HIGH period	4.0		μs
T <sub>F</sub>	Clock/Data fall time		300	ns
T <sub>R</sub>	Clock/Data rise time		1000	ns
<b>Port Timing</b>				
T <sub>PV</sub>	Output data valid		4	μs
T <sub>PS</sub>	Input data setup time	0		μs
T <sub>PH</sub>	Input data hold time	4		μs
<b>Reset</b>				
T <sub>W</sub>	Reset pulse width	2		ns

# Octal SMBus Registered Interface

# PCA9556

**TSSOP16:** plastic thin shrink small outline package; 16 leads; body width 4.4 mm

**SOT403-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				94-07-12 95-04-04

---

# Octal SMBus Registered Interface

PCA9556

---

## NOTES

## Octal SMBus Registered Interface

PCA9556



Purchase of Philips I<sup>2</sup>C components conveys a license under the Philips' I<sup>2</sup>C patent to use the components in the I<sup>2</sup>C system provided the system conforms to the I<sup>2</sup>C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

## Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information** — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

## Disclaimers

**Life support** — These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

**Right to make changes** — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Philips Semiconductors  
811 East Arques Avenue  
P.O. Box 3409  
Sunnyvale, California 94088-3409  
Telephone 800-234-7381

© Copyright Philips Electronics North America Corporation 1999  
All rights reserved. Printed in U.S.A.

Date of release: 04-99

Document order number:

9397 750 04974

*Let's make things better.*

Go to Philips Semiconductors' home

Select & Go...

Catalog & Datasheets

#### Catalog by Function

- Discrete semiconductors
- Audio
- Clocks and Watches
- Data communications
- Microcontrollers
- Peripherals
- Standard analog
- Video
- Wired communications
- Wireless communications

#### Catalog by System

- Automotive
- Consumer Multimedia Systems
- Communications
- PC/PC-peripherals

#### Cross reference

#### Models

#### Packages

#### Application notes

#### Selection guides

#### Other technical documentation

#### End of Life information

#### Datahandbook system

#### Relevant Links

- About catalog tree
- About search
- About this site
- Subscribe to eNews
- Catalog & Datasheets
- Search
- [PCA9556](#)
- [PCA9556](#)

## PCA9556; Octal SMBus Registered Interface

- [Description](#)
- [Features](#)
- [Datasheet](#)
- [Products, packages, availability and ordering](#)
- [Find similar products](#)

### Description

The PCA9556 is a silicon CMOS circuit which provides parallel input/output expansion applications. The PCA9556 consists of an 8-bit input port register, 8-bit output port interface. It has low current consumption and a high impedance open drain output port.

The SMBus system master can reset the PCA9556 in the event of a timeout by asserting reset input. The SMBus system master can also invert the PCA9556 inputs by writing polarity inversion bits. Finally, the SMBus system master can enable the PCA9556's outputs by writing to their I/O configuration bits.

The power-on reset sets the registers to their default values and initializes the SMB RESET pin causes the same reset/initialization to occur without depowering the part.

### Features

- SMBus compliance with fixed 3.3V voltage levels
- Operating power supply voltage range of 3.0V - 3.6V
- Active high polarity inverter register
- Write protect register
- Active low reset pin
- Low leakage current on power-down
- Noise filter on SCL/SDA inputs
- No glitch on power-up
- Internal power-on reset
- 8 I/O pins which default to 8 inputs
- High impedance open drain on I/O

### Datasheet

<u>Type nr.</u>	<u>Title</u>	<u>Publication release date</u>	<u>Datasheet status</u>	<u>Page count</u>
PCA9556	Octal SMBus Registered Interface	18-Dec-98	Product Specification	12

### Products, packages, availability and ordering

<u>Partnumber</u>	<u>North American Partnumber</u>	<u>Order code (12nc)</u>	<u>marking/packing</u>	<u>package</u>	<u>device s</u>
PCA9556PW	PCA9556PW	9352 628 99112	Standard Marking * Tube	<a href="#">SOT403</a>	Full pro
	PCA9556PW- T	9352 628 99118	Standard Marking * Reel Pack, SMD, 13"	<a href="#">SOT403</a>	Full pro

### Find similar products:

[PCA9556](#) links to the similar products page containing an overview of product function or related to the part number(s) as listed on this page. The similar products from the same catalog tree(s) , relevant selection guides and products from the sar