National Semiconductor

December 1995

NM93C56/C56A
2,048-Bit Serial Interface, Standard Voltage CMOS EEPROM (MICROWIRE™ Synchronous Bus)

General Description

The NM93C56/C56A is 2,048 bits of CMOS non-volatile, electrically erasable memory organized in either 128 16-bit registers (NM93C56), or user organized as either 128 16-bit registers or 256 8-bit registers (NM93C56A). The user organization is determined by the status of the ORG input. The memory device is fabricated using National Semiconductor's floating gate CMOS process for high reliability, high endurance and low power consumption. The NM93C56/C56A is available in an 8-pin SO package for space considerations.

The EEPROM is MICROWIRE compatible for simple interfacing to a wide variety of microcontrollers and microprocessors. There are 7 instructions that operate the NM93C56/C56A: Read, Erase/Write Enable, Erase, Write, Erase/Write Disable, Write All, and Erase All.

The NM93C56A defaults to the 128 x 16 configuration if the ORG pin (Pin 6) is left floating, as it is internally pulled up to V_CC.

Features

- 4.5V to 5.5V operation in all modes
- Typical active current of 400 μA; typical standby current of 25 μA
- Self-timed programming cycle
- Device status indication during programming mode
- No erase required before write
- Reliable CMOS floating gate technology
- MICROWIRE compatible serial I/O
- 40 years data retention
- Endurance: 10^6 data changes
- Packages available: 8-Pin TSSOP, 8-pin SO, 8-pin DIP

Block Diagram
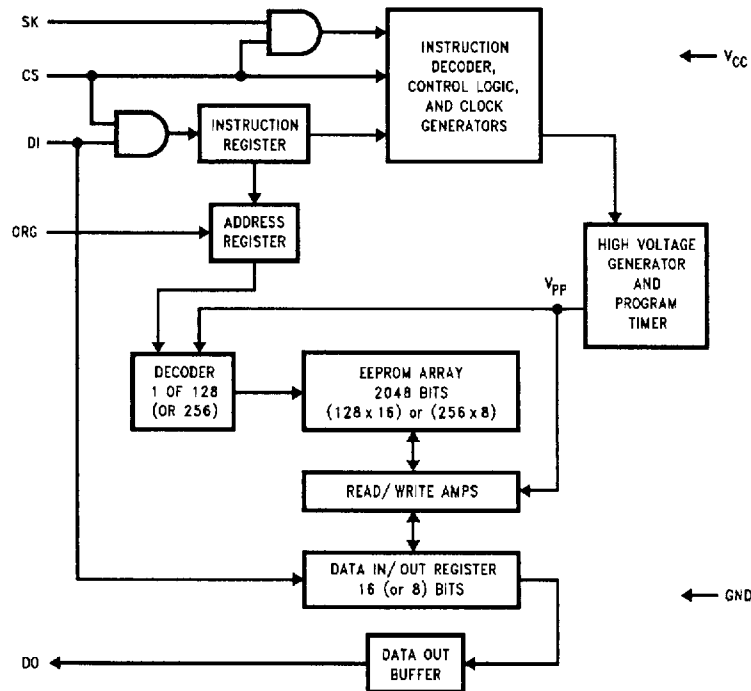
TRI-STATE® is a registered trademark of National Semiconductor Corporation.
MICROWIRE™ is a trademark of National Semiconductor Corporation.

TL/D/12509–1

Connection Diagrams

Dual-In-Line Package (N)
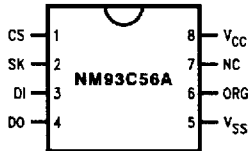**8-Pin SO Package (M8)**
and 8-Pin TSSOP Package (MTC08)

```
       ┌───┬───┐
CS ──│1  ∪   8│── V_CC
SK ──│2      7│── NC
DI ──│3 NM93C56 6│── NC
DO ──│4      5│── V_SS
       └───────┘
```

TL/D/12509-2

Top View

See NS Package Number
N08E, M08A and MTC08

Dual-In-Line Package (N)
8-Pin SO Package (M8)
and 8-Pin TSSOP Package (MTC08)

```
       ┌───┬───┐
CS ──│1  ∪   8│── V_CC
SK ──│2      7│── NC
DI ──│3 NM93C56A 6│── ORG
DO ──│4      5│── V_SS
       └───────┘
```

TL/D/12509-3

Top View

See NS Package Number
N08E, M08A and MTC08

Pin Names

Pin	Description
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{SS}	Ground
ORG	Memory Organization Select (On the NM93C56A)
NC	No Connect
V_{CC}	Positive Power Supply

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number
NM93C56N
NM93C56M8
NM93C56MT8

Commercial Temp. Range (0°C to +70°C)

Order Number
NM93C56AN
NM93C56AM8
NM93C56AMT8

Extended Temp. Range (−40°C to +85°C)

Order Number
NM93C56EN
NM93C56EM8
NM93C56EMT8

Extended Temp. Range (−40°C to +85°C)

Order Number
NM93C56AEN
NM93C56AEM8
NM93C56AEMT8

Military Temp. Range (−55°C to +125°C)

Order Number
NM93C56MN
NM93C56MM8
NM93C56MMT8

Military Temp. Range (−55°C to +125°C)

Order Number
NM93C56AMN
NM93C56AMM8
NM93C56AMMT8

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	$-65°C$ to $+150°C$
All Input or Output Voltages with Respect to Ground	$V_{CC} +1$ to $-0.3V$
Lead Temperature (Soldering, 10 seconds)	$+300°C$
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature

NM93C56/C56A	$0°C$ to $+70°C$
NM93C56E/C56AE	$-40°C$ to $+85°C$
NM93C56M/C56AM	$-55°C$ to $+125°C$
Power Supply (V_{CC}) Range	4.5V to 5.5V

DC and AC Electrical Characteristics $4.5V \leq V_{CC} \leq 5.5V$

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CCA}	Operating Current	NM93C56/C56A NM93C56E/C56AE NM93C56M/C56AM	$CS = V_{IH}$ SK = 1 MHz SK = 1 MHz SK = 0.5 MHz		1	mA
I_{CCS}	Standby Current		$CS = 0V$ ORG $= V_{CC}$ or NC		50	μA
I_{IL}	Input Leakage		$V_{IN} = 0V$ to V_{CC} (Note 2)	-1	1	μA
I_{ILO}	Input Leakage ORG Pin		ORG Tied to V_{CC} ORG Tied to V_{SS} (Note 3)	-1 -2.5	1 2.5	μA
I_{OL}	Output Leakage		$V_{IN} = 0V$ to V_{CC}	-1	1	μA
V_{IL}	Input Low Voltage			-0.1	0.8	V
V_{IH}	Input High Voltage			2	$V_{CC} +1$	V
V_{OL1}	Output Low Voltage		$I_{OL} = 2.1$ mA		0.4	V
V_{OH1}	Output High Voltage		$I_{OH} = -400$ μA	2.4		V
V_{OL2}	Output Low Voltage		$I_{OL} = 10$ μA		0.2	V
V_{OH2}	Output High Voltage		$I_{OL} = -10$ μA	$V_{CC} - 0.2$		V
f_{SK}	SK Clock Frequency	NM93C56/C56A NM93C56E/C56AE NM93C56M/C56AM	(Note 4)	0 0 0	1 1 0.5	MHz
t_{SKH}	SK High Time	NM93C56/C56A NM93C56E/C56AE NM93C56M/C56AM		250 300 500		ns
t_{SKL}	SK Low Time			250		ns
t_{CS}	Minimum CS Low Time	NM93C56/C56A NM93C56E/C56AE NM93C56M/C56AM	(Note 5)	250 250 500		ns
t_{CSS}	CS Set-Up Time	NM93C56/C56A NM93C56E/C56AE NM93C56M/C56AM		50 50 100		ns

DC and AC Electrical Characteristics 4.5V ≤ V_{CC} ≤ 5.5V (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{DH}	DO Hold Time			70		ns
t_{DIS}	DI Set-Up Time	NM93C56/C56A NM93C56E/C56AE NM93C56M/C56AM		100 200 200		ns
t_{CSH}	CS Hold Time			0		ns
t_{DIH}	DI Hold Time			20		ns
t_{PD1}	Output Delay to "1"	NM93C56/C56A NM93C56E/C56AE NM93C56M/C56AM			500 500 1000	ns
t_{PD0}	Output Delay to "0"	NM93C56/C56A NM93C56E/C56AE NM93C56M/C56AM			500 500 1000	ns
t_{SV}	CS to Status Valid	NM93C56/C56A NM93C56E/C56AE NM93C56M/C56AM			500 500 1000	ns
t_{DF}	CS to DO in TRI-STATE®	NM93C56/C56A NM93C56E/C56AE NM93C56M/C56AM			100 100 200	ns
t_{WP}	Write Cycle Time				10	ms

Capacitance
T_A = +25°C, f = 1 MHz (Note 6)

Symbol	Test	Max	Units
C_{OUT}	Output Capacitance	5	pF
C_{IN}	Input Capacitance	5	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2.0V

Note 1: Stress ratings above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical leakage values are in the 20 nA range.

Note 3: The ORG pin may draw >1 μA when in the x8 mode due to an internal pull-up transistor.

Note 4: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKL} limits must be observed. Therefore, it is not allowable to set $1/t_{SK}$ = $t_{SKH(minimum)}$ + $t_{SKL(minimum)}$ for shorter SK cycle time operation.

Note 5: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle. (This is shown in the opcode diagrams in the following pages.)

Note 6: This parameter is periodically sampled and not 100% tested.

Interface Pin Description

Chip Select (CS):

Chip Select performs several functions. It is used to differentiate between various devices on the same MICROWIRE bus. The rising edge resets the internal circuitry of the device, a function necessary prior to initiating a new cycle. Chip Select (as shown on Block Diagram) also gates the Data Input (DI) and Serial Clock (SK) Input, to disable these functions. In the case of these EEPROMs, Chip Select cannot be tied HIGH even if it is the only device on the bus.

Chip Select must be held HIGH continuously during the course of clocking in the start bit, op-code address, and data-in or data-out. Otherwise the internal circuits will reset and the cycle will have to be started again with a new start bit.

Chip Select initiates the internal programming cycle. The falling edge of Chip Select will start the internal asynchronous programming cycle after a programming op-code has been entered (Erase, Write, Erase All, or Write All). In conjunction with Chip Select, Data-Out (DO) will indicate when programming is complete. If the internal programming is incomplete, then Data-Out pin will be LOW. Then when the internal programming is complete, the Data-Out pin will be HIGH (see Timing Diagrams).

Serial Clock (SK):

The Serial Clock input is used to clock all start bits, op-codes, data, addresses, and data bits into or out of the EEPROMs. The clock's rising edge controls the input and output of bits. The falling edge has no effect on the device. The Serial Clock is not necessary for the asynchronous Ready/Busy polling function.

The Serial Clock is in a "Don't Care" at any time Chip Select is LOW. It is also in a "Don't Care" state prior to clocking in a start bit, or during Ready/Busy polling. During either of these last two conditions, Data-In (DI) must be held at a LOW level, otherwise a new start bit will be interpreted.

Data-In (DI):

The Data-In pin receives the start bit, address, and input data synchronously. Each bit is clocked in on the rising edge of SK. DI is gated by Chip Select to provide a high degree of noise immunity. Data-In is routed to both the instruction shift register and the data shift register. After the start bit is clocked into the last bit of the instruction register, the clock is switched to the data register to receive input data. To avoid false reading of a start bit, it is safer to keep the Data-In pin at LOW level when not in use.

Data-Out (DO):

The Data-Out pin sends Read data onto the MICROWIRE bus and it is clocked out on the rising edge of the Serial Clock. During the Read cycle, the DO output begins to drive actively after the last address bit (A0) is clocked in.

Data-Out also carries the device's status during the asynchronous programming cycle. The Data-Out pin drives LOW while the device is still in its internal programming cycle. After the EEPROM has completed this internal programming, Data-Out will drive HIGH. This is accomplished while Chip Select is held HIGH.

Finally, if Chip Select is pulsed LOW to HIGH, Data-Out pin will again produce a pulse HIGH. Thus indicating the completion of the programming cycle.

To clear the Ready/Busy polling, it is necessary to raise Chip Select and clock in another start bit. Once the start bit is clocked in, Data-Out will return to the HIGH impedance state. It is not necessary to continue with a cycle after this start bit has been clocked in, although it is permissible to start a new cycle with this start bit. This clearing of Ready/Busy status may be necessary if a bidirectional data bus is used (Data-In tied to Data-Out) as the Data-Out output will interfere with the new data being presented on the Data-In pin. This connecting of the two Data pins is used for three-wire interface schemes.

Organization (ORG):

The Organization input (ORG) is available only on the NM93C46A device and it is used to control the internal organization of the memory. The two selectable organizations are 16-bit words and 8-bit words. By connecting the ORG pin to V_{CC}, 16-bit words are selected. In contrast, by connecting the ORG pin to GND, 8-bit words are selected. If the ORG pin is left floating, then default setting is the 16-bit word. When in the 8-bit mode, one additional address bit is required in the instruction sequence since the depth of the memory is doubled.

Instruction Set for NM93C56/C56A

The NM93C56/C56A has 7 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. The next 2 bits carry the op code, the next 7 (or 8) bits carry the address for selection of 1 of 128 16-bit registers or 1 of 256 8-bit registers, depending on memory array organization.

1024 by 16-Bit Organization (NM93C56 or NM93C56A when ORG = V$_{CC}$ or NC)

Instruction	SB	Op Code 2 Bits	Address 7 Bits	Data 16 Bits	Comments
READ	1	10	A6–A0		Read data stored in selected registers.
EWEN	1	00	11XXXXX		Enables programming modes.
EWDS	1	00	00XXXXX		Disables all programming modes.
ERASE	1	11	A6–A0		Erase selected register.
WRITE	1	01	A6–A0	D15–D0	Writes data pattern D15–D0 into selected registers.
ERAL	1	00	10XXXXX		Erases all registers.
WRAL	1	00	01XXXXX	D15–D0	Writes data pattern D15–D0 into all registers.

2048 by 8-Bit Organization (NM93C56A when ORG = GND)

Instruction	SB	Op Code 2 Bits	Address 8 Bits	Data 8 Bits	Comments
READ	1	10	A7–A0		Read data stored in selected registers.
EWEN	1	00	11XXXXXX		Enables programming modes.
EWDS	1	00	00XXXXXX		Disables all programming modes.
ERASE	1	11	A7–A0		Erase selected register.
WRITE	1	01	A7–A0	D7–D0	Writes data pattern D7–D0 into selected registers.
ERAL	1	00	10XXXXXX		Erases all registers.
WRAL	1	00	01XXXXXX	D7–D0	Writes data pattern D7–D0 into all registers.

Functional Description

Device	ORG Pin Logic	Memory	
		Configuration	# of Address Bits
NM93C56	X	128 x 16	7 Bits
NM93C56A	0	256 x 8	8 Bits
	1	128 x 16	7 Bits

The following instructions are common to both the NM93C56 and NM93C56A devices.

Programming

In all programming modes the READY/BUSY status of the device can be determined by polling the DO pin. After clocking in the last bit of the instruction sequence and with the CS held "high", the DO pin will exit the high impedance state and indicate the READY/BUSY status of the device. DO = logical "0" indicates that programming is still in progress and no other instruction can be executed. DO = logical "1" indicates that the device is READY for another instruction. If CS is forced "low" the DO pin will return to the high impedance state. After the programming cycle has been completed and DO = logical "1", the DO pin can be reset back to the high impedance state by clocking a logical "1" into the DI pin. (This is also performed with the start bit on all op codes, thus clocking an instruction has the same effect.)

Read (READ)

The READ instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a serial-out shift register. A dummy bit (logical 0) precedes the serial data output string. Output data changes are initiated by a low to high transition of SK after the last address bit (A0) is clocked in.

Erase/Write Enable (EWEN)

When V$_{CC}$ is applied to the part, it "powers up" in the Erase/Write Disable (EWDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V$_{CC}$ is removed from the part.

Functional Description (Continued)

Erase/Write Disable (EWDS)

To protect against accidental data overwrites, the Erase/Write Disable (EWDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

Erase (ERASE)

The ERASE instruction will program all bits in the specified register to the logical "1" state. The self-timed programming cycle is initiated on the rising edge of the SK clock as the last address bit (A0) is clocked in. At this point CS, SK and DI become don't care states. After starting an Erase cycle the DO pin indicates the READY/BUSY status of the chip if CS is held "high". DO = logical "0" indicates that programming is still in progress. DO = logical "1" indicates that the register, at the address specified in the instruction, has been erased.

Write (WRITE)

The WRITE instruction is followed by 16 bits of data (or 8 bits of data when using the NM93C56A in the x8 organi-zation) to be written into the specified address. The self-timed programming cycle is initiated on the rising edge of the SK clock as the last data bit (D0) is clocked in. At this point, CS, SK and DI become don't care states. No separate ERASE cycle is required before a WRITE instruction.

As in the ERASE instruction, after starting a WRITE cycle, the DO pin indicates the READY/BUSY status of the chip if CS is held "high". DO = logical "0" indicates that programming is still in progress. DO = logical "1" indicates that the register, at the address specified in the instruction, has been written and that the part is ready for another instruction.

Erase All (ERAL)

The ERAL instruction will simultaneously program all registers in the memory array to the logical "1" state.

Write All (WRAL)

The WRAL instruction will simultaneously program all registers with the data pattern specified in the instruction.

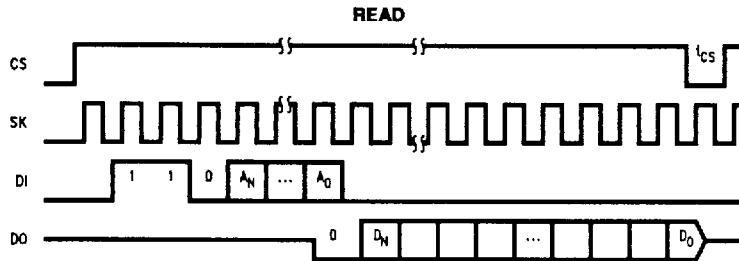## Timing Diagrams for both the NM93C56 and NM93C56A

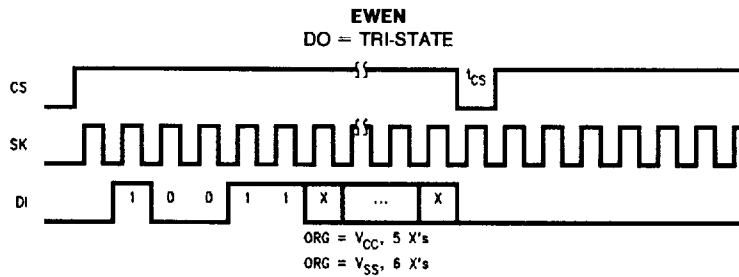### Synchronous Data Timing
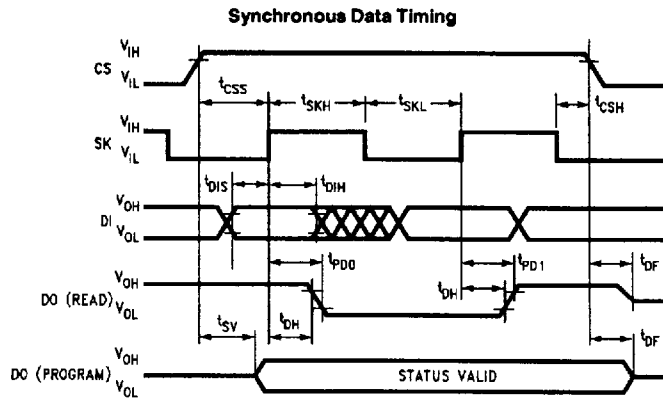
TL/D/12509–4

Timing Diagrams for both the NM93C56 and NM93C56A (Continued)

Organization of Address and Data Fields for the NM93C56A

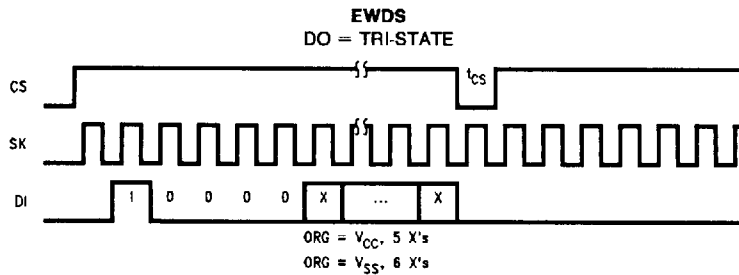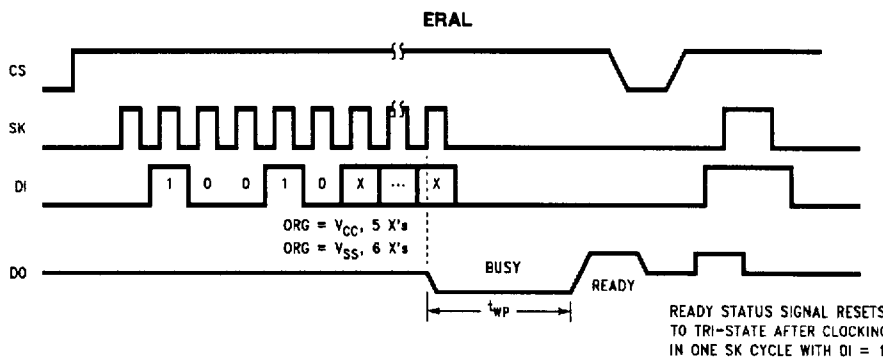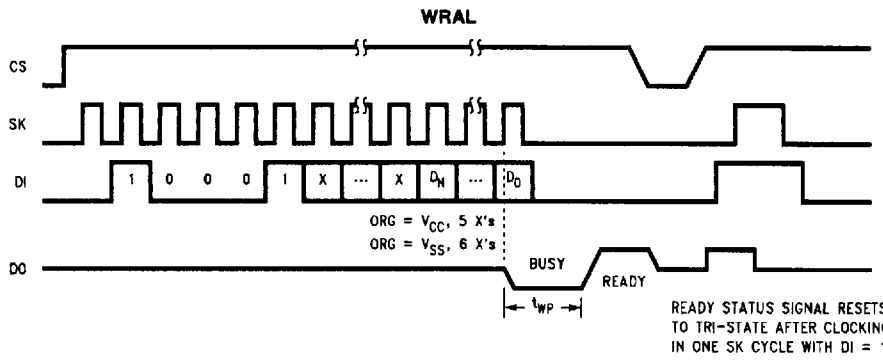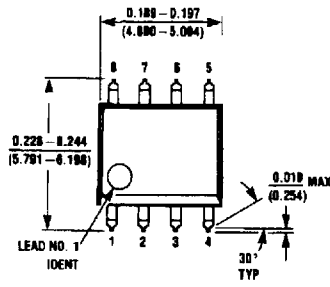| ORG Pin	Organization	A_N	D_N
V_{CC} or NC	128 x 16	A6	D15
V_{SS}	256 x 8	A7	D7

READ

TL/D/12509-5

EWEN
DO = TRI-STATE

ORG = V_{CC}, 5 X's
ORG = V_{SS}, 6 X's

TL/D/12509-6

EWDS
DO = TRI-STATE

ORG = V_{CC}, 5 X's
ORG = V_{SS}, 6 X's

TL/D/12509-7

ERASE

BUSY
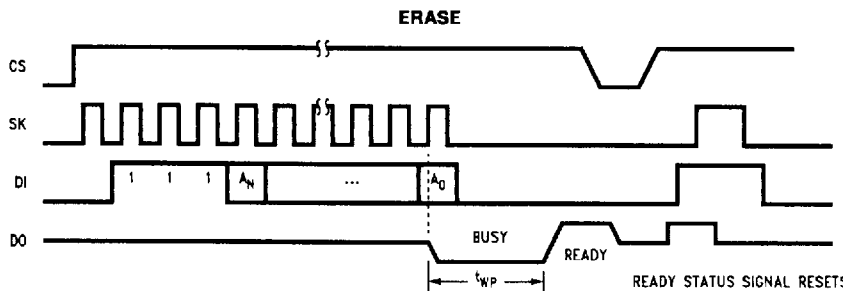
READY

READY STATUS SIGNAL RESETS
TO TRI-STATE AFTER CLOCKING
IN ONE SK CYCLE WITH DI = 1

TL/D/12509-8

Timing Diagrams for both the NM93C56 and NM93C56A (Continued)

WRITE

READY STATUS SIGNAL RESETS
TO TRI-STATE AFTER CLOCKING
IN ONE SK CYCLE WITH DI = 1

TL/D/12509-9

ERAL

ORG = V_{CC}, 5 X's
ORG = V_{SS}, 6 X's

READY STATUS SIGNAL RESETS
TO TRI-STATE AFTER CLOCKING
IN ONE SK CYCLE WITH DI = 1

TL/D/12509-10

WRAL

ORG = V_{CC}, 5 X's
ORG = V_{SS}, 6 X's

READY STATUS SIGNAL RESETS
TO TRI-STATE AFTER CLOCKING
IN ONE SK CYCLE WITH DI = 1

TL/D/12509-11

9

Physical Dimensions inches (millimeters)

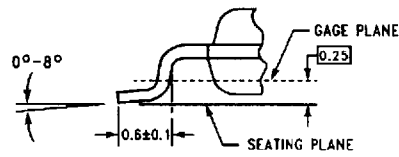0.189 − 0.197
(4.800 − 5.004)

8 7 6 5

0.228 − 0.244
(5.791 − 6.198)

0.010 MAX
(0.254)

LEAD NO. 1
IDENT

1 2 3 4

30°
TYP

0.150 − 0.157
(3.810 − 3.988)

0.010 − 0.020
(0.254 − 0.508) × 45°

6° MAX TYP
ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.008 − 0.010
(0.203 − 0.254)
TYP ALL LEADS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.053 − 0.069
(1.346 − 1.753)

0.004 − 0.010
(0.102 − 0.254)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008 TYP
(0.203)

0.014 − 0.020 TYP
(0.356 − 0.508)
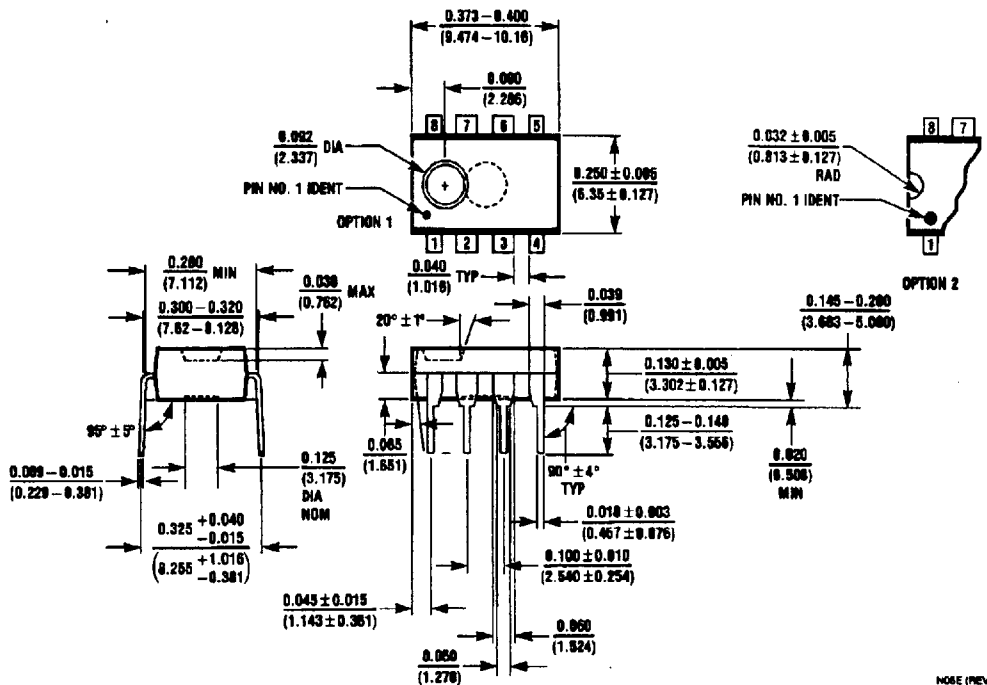
M08A (REV H)

Molded Small Outline Package (M8)
Order Number NM93C56M8 or NM93C56AM8
NS Package Number M08A

6501126 0073299 481

Physical Dimensions millimeters (Continued)

3.0±0.1
-A-

6.4

3.2

4.4±0.1
-B-

0.2 C B A
ALL LEAD TIPS

PIN #1 IDENT.

7.72 TYP

4.16 TYP

(1.78 TYP)

0.42 TYP

0.65 TYP

LAND PATTERN RECOMMENDATION

1.1 MAX TYP

0.1 C
ALL LEAD TIPS

(0.9)

-C-

0.10±0.05 TYP

0.65 TYP

0.19-0.30 TYP

0.13 M A B S C S
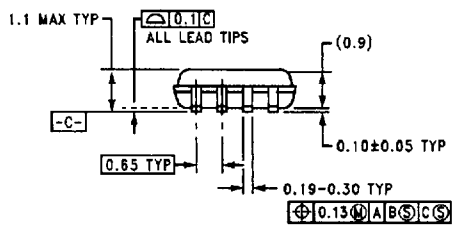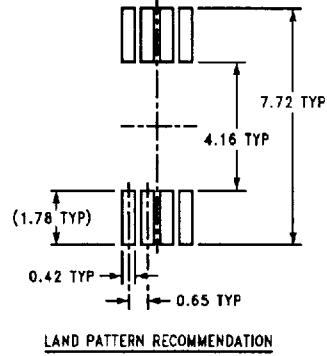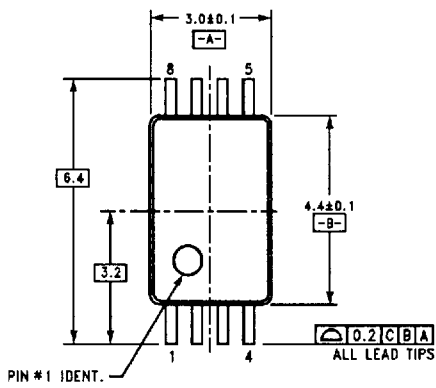
DIMENSIONS ARE IN MILLIMETERS

SEE DETAIL A

0.09-0.20 TYP

GAGE PLANE

0.25

0°-8°

0.6±0.1

SEATING PLANE
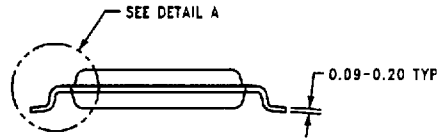
DETAIL A
TYPICAL, SCALE: 40X

MTC08 (REV A)

Molded Small Outline Package (MTC08)
Order Number NM93C56M8 or NM93C56AM8
NS Package Number MTC08

6501126 0073300 T23

Physical Dimensions inches (millimeters) (Continued)

Molded Dual-In-Line Package (N)
Order Number NM93C56N or NM93C56AN
NS Package Number N08E

LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

6501126 0073301 96T