Features

256Kx16 bit CMOS Static
Random Access Memory

- Access Times: 20, 25 and 35ns
- Data Retention Function (LPA version)
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

44 lead JEDEC Approved Revolutionary Pinout

- Ceramic Flatpack No. 323
- Ceramic SOJ No. 322

Single +5V (±10%) Supply Operation

256Kx16 Static RAM
CMOS, Monolithic

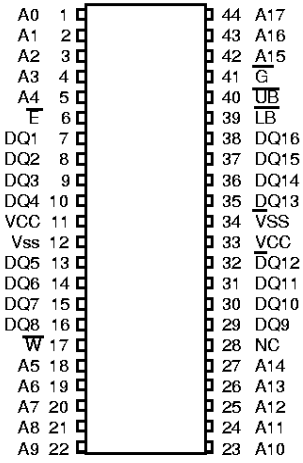
The EDI816256CA is a 4 megabit Monolithic CMOS Static RAM.

The EDI816256CA uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device allows upper and lower byte access by use of the data byte control pins (LB/ UB/).

The devices are available in a fully hermetic 44 lead ceramic SOJ and a 44 lead Ceramic Flatpack. The Ceramic SOJ is pin for pin compatible with the commercially available plastic SOJ. This allows the user the luxury of designing a board that can be used for both the commercial and military market.

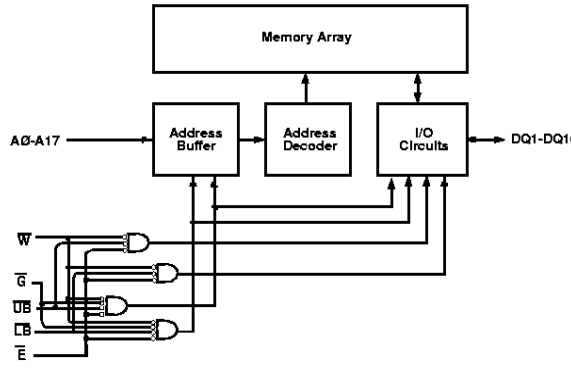
A Low Power version with Data Retention (EDI816256LPA) is also available for battery backed applications. Military product is available compliant to Appendix A of MIL-PRF-38535.

Pin Configurations and Block Diagram



Pin Names

AØ-A17	Address Inputs
E	Chip Enable
W	Write Enable
G	Output Enable
DQ1-DQ16	Common Data Input/Output
LB (DQ1-DQ8)	Lower-Byte Control
UB (DQ9-DQ16)	Upper-Byte Control
VCC	Power (+5V±10%)
VSS	Ground



Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Military	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Power Dissipation	1.5 Watts
Output Current.	20 mA
Junction Temperature, TJ	175°C

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CI	12	pF
Data Lines	CD/Q	14	pF

These parameters are sampled, not 100% tested.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	VCC+0.5	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

(note: For TEHQZ,TGHQZ and TWLQZ, See Figure 2)

Figure 1

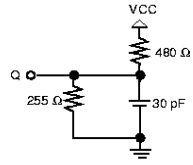
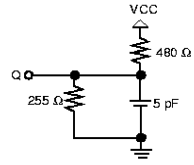


Figure 2



DC Electrical Characteristics

Parameter	Sym	Conditions		Min	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, I/O = 0mA, Min Cycle		-	300	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ ≥ VIH, VIN ≤ VIL VIN ≥ VIH		-	60	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$ ≥ VCC-0.2V	CA	--	25	mA
		VIN ≥ VCC-0.2V or VIN ≤ 0.2V	LPA	--	10	mA
Input Leakage Current	ILI	VIN = 0V to VCC		-10	10	µA
Output Leakage Current	ILO	V I/O = 0V to VCC		-10	10	µA
Output High Voltage	VOH	IOH = -4mA		2.4	–	V
Output Low Voltage	VOL	IOL = 8mA		--	0.4	V

Truth Table

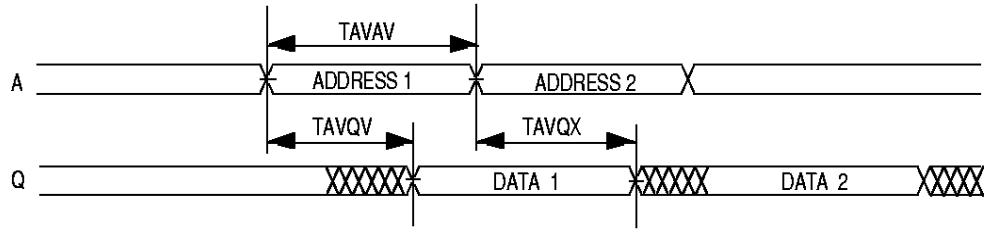
$\overline{E}$	$\overline{W}$	$\overline{G}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						DQ1-DQ8	DQ9-DQ16	
H	X	X	X	X	Not Selected	High Z	High Z	ICC2, ICC3
L	H	H	X	X	Output Disable			
L	X	X	H	H				
L	H	L	L	H	Read	Dout	High Z	ICC1
			H	L		High Z	Dout	
			L	L		Dout	Dout	
L	L	X	L	H	Write	Din	High Z	ICC1
			H	L		High Z	Din	
			L	L		Din	Din	

AC Characteristics Read Cycle

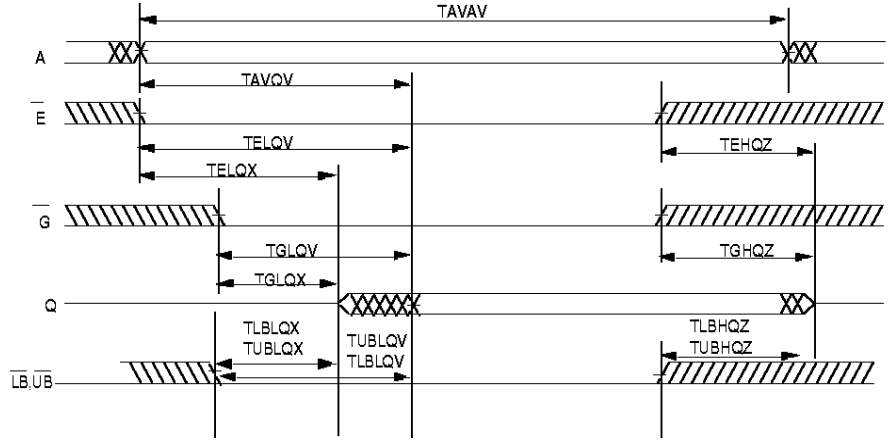
	Symbol		20ns		25ns		35ns		
Parameter	**JEDEC**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Read Cycle Time	TAVAV	TR	20		25		35		ns
Address Access Time	TAVQV	TAA		20		25		35	ns
Chip Enable Access Time	TELQV	TACS		20		25		35	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	5		5		5		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ	0	7	0	8	0	10	ns
Output Hold from Address Change	TAVQX	TOH	4		5		5		ns
Output Enable to Output Valid	TGLQV	TOE		10		12		15	ns
Output Enable to Output in Low Z (1)	TGLQX	TLOZ	0		0		0		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ	0	7	0	8	0	10	ns
$\overline{LB}$, $\overline{UB}$ Access Time	TUBLQV TLBLQV	TBA		10		12		15	ns
$\overline{LB}$, $\overline{UB}$ Enable to Low Z Output	TUBLQX TLBLQX	TBLZ	0		0		0		ns
$\overline{LB}$, $\overline{UB}$ disable to High Z Output	TLBHQZ TUBHQZ	TBHZ	0	7	0	8	0	10	ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1 - W High, G, E Low



Read Cycle 2 - W High

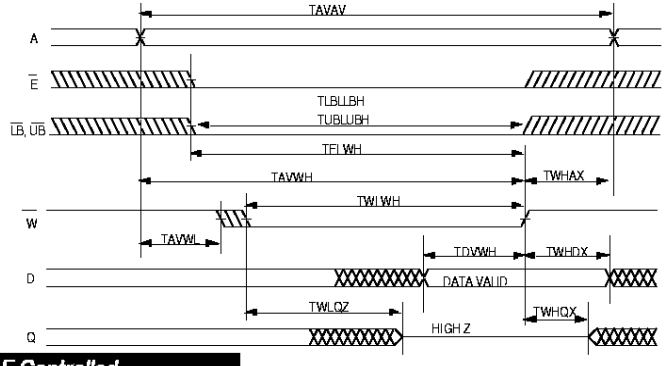


AC Characteristics Write Cycle

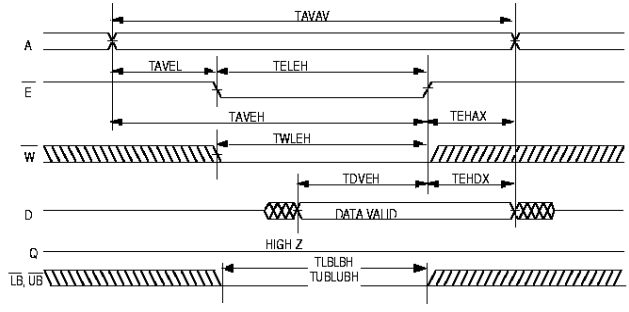
	Symbol		20ns		25ns		35ns		
Parameter	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Units
Write Cycle Time	TAVAV	TWC	20		25		35		ns
Chip Enable to End of Write	TELWH	TCW	15		17		20		ns
	TELEH	TCW	15		17		20		ns
Address Setup Time	TAVWL	TAS	0		0		0		ns
	TAVEL	TAS	0		0		0		ns
	TAVUBL	TAS	0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	15		17		20		ns
	TAVEH	TAW	15		17		20		ns
	TAVUBH	TAW	15		17		20		ns
Write Pulse Width	TWLWH	TWP	15		17		20		ns
	TWLEH	TWP	15		17		20		ns
Write Recovery Time	TWHAX	TWR	0		0		0		ns
	TEHAX	TWR	0		0		0		ns
Data Hold Time(1)	TWHDX	TDH	0		0		0		ns
	TEHDX	TDH	0		0		0		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	8	0	8	0	8	ns
Data to Write Time	TDVWH	TDW	10		12		15		ns
	TDVEH	TDW	10		12		15		ns
Output Active from End of Write (1)	TWHQX	TWLZ	0		12		15		ns
LB,UB Valid to End of Write	TLBLLBH	TBW	16		18		20		ns
	TUBLUBH								

Note 1: Parameter guaranteed, but not tested.

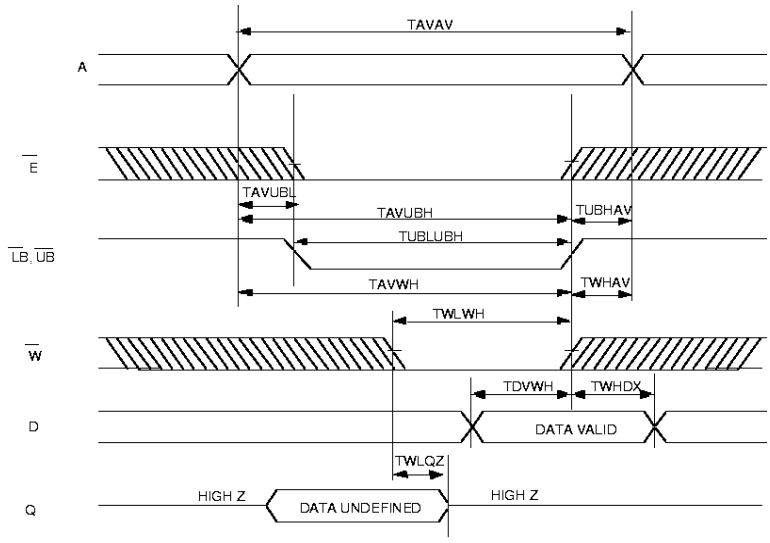
Write Cycle 1 - W Controlled



Write Cycle 2 - E Controlled



Write Cycle 3 - LB, UB Controlled



Data Retention Characteristics

EDI816256LPA Only

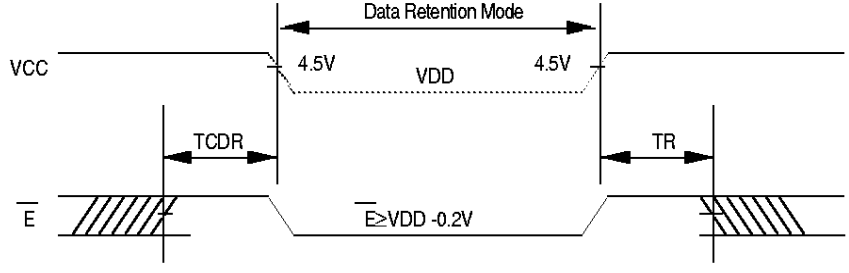
(TA = -55°C to +125°C)

Characteristic	Sym	Test Conditions	VDD	Min	Typ	Max	Unit
Data Retention Voltage	VDD	$\overline{E} \geq$ VDD -0.2V VIN $\geq$ VDD -0.2V or VIN $\leq$ 0.2V	2V	2	--	–	V
Data Retention Quiescent Current	ICCDR			–	–	2	mA
Chip Disable to Data Retention Time(1)	TCDR			0	--	–	ns
Operation Recovery Time (1)	TR			TAVAV*		–	ns

Note 1: Parameter guaranteed, but not tested.

*Read Cycle Time

Data Retention E Controlled



Ordering Information

Military

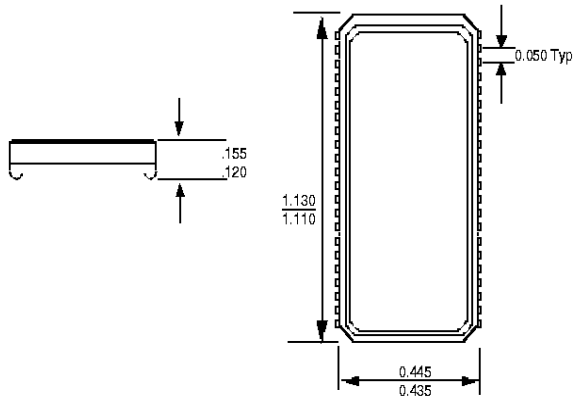
Part No. Standard Power	Speed ns	Package No.
EDI816256CA20F44B	20	323
EDI816256CA25F44B	25	323
EDI816256CA35F44B	35	323
EDI816256CA20N44B	20	322
EDI816256CA25N44B	25	322
EDI816256CA35N44B	35	322

Low Power with Data Retention	Speed ns	Package No.
EDI816256LPA20F44B	20	323
EDI816256LPA25F44B	25	323
EDI816256LPA35F44B	35	323
EDI816256LPA20N44B	20	322
EDI816256LPA25N44B	25	322
EDI816256LPA35N44B	35	322

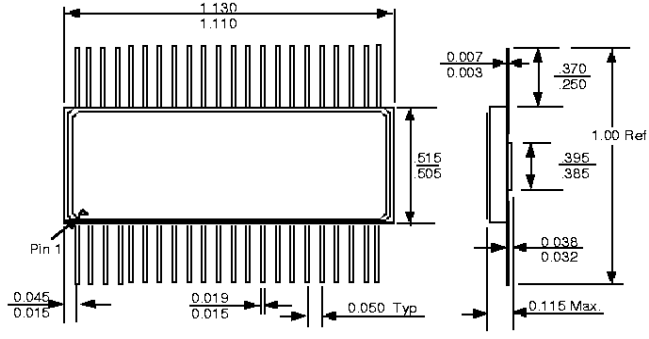
For Commercial, Industrial or Military grade product use C, I or M respectively, to replace B in the suffix of part number, e.g. EDI816256CA20F44B becomes EDI816256CA20F44C (Commercial temp range), EDI816256CA20F44I (Industrial temp range) or EDI816256CA20F44M (Military temp range).

Package Description

Package No. 322
44 Lead Ceramic
SOJ Package



Package No. 323
44 Pin Ceramic
Flatpack



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