HARRIS

2N6849

Avalanche-Energy-Rated P-Channel Power MOSFETs

August 1991

Features

- -6.5A, -100V
- $r_{DS(on)} = 0.30\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

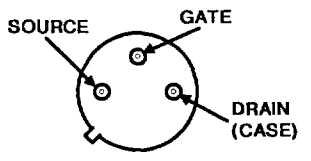
Description

The 2N6849 is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. This is a p-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6849 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

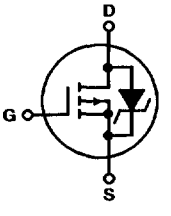
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^oC$) Unless Otherwise Specified

		2N6849	UNITS
Drain-Source Voltage	V_{DS}	-100*	V
Drain-Gate Voltage ($R_{GS} = 20k\Omega$)	V_{DGR}	-100*	V
Continuous Drain Current			
$T_C = +25^oC$	I_D	-6.5*	A
$T_C = +100^oC$	I_D	-4.1*	A
Pulsed Drain Current (Note 2)	I_{DM}	-25*	A
Gate-Source Voltage	V_{GS}	±20*	V
Maximum Power Dissipation			
$T_C = +25^oC$ (See Figure 14)	P_D	25*	W
Above $T_C = +25^oC$, Derate Linearly (See Figure 14)		0.2*	W/^oC
Single Pulse Avalanche Energy (Note 3)	E_{AS}	500	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	^oC
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	^oC

NOTES:

*JEDEC registered values

1. Pulse Test: Pulse width $\leq$ 300μs, Duty Cycle $\leq$ 2%
2. Repetitive Rating: Pulse width limited by maximum junction temperature, See Transient Thermal Impedance Curve (Figure 5)
3. V_{DD} = 25V, Starting T_J = 25°C, L = 17.25mH, $R_G \approx 25\Omega$, Peak I_L = 6.5A, (See Figure 15 and 16)

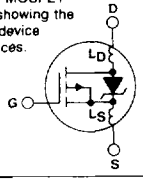
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number **2219**

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	−100*	—	—	V	V_{GS} = 0V, I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	−2.0*	—	−4.0*	V	V_{DS} = V_{GS}, I_D = −0.25mA
I_{GSS}	Gate-Source Leakage Forward	—	—	−100	nA	V_{GS} = −20V
I_{GSS}	Gate-Source Leakage Reverse	—	—	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	—	—	−0.25*	μA	V_{DS} = Max. Rating, V_{GS} = 0V
		—	—	−1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Drain Voltage ①	—	—	−2.1	V	V_{DS} > $I_{D(on)}R_{DS(on)}$max., V_{GS} = −10V, I_D = 6.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	—	—	0.30*	Ω	V_{GS} = −10V, I_D = −4.1A
g_{fs}	Forward Transconductance ①	2.5	3.5	7.5	S(℧)	V_{DS} = −5V, $I_{D(on)}$ × $R_{DS(on)}$ max., I_D = −4.1A
C_{iss}	Input Capacitance	—	500	—	pF	V_{GS} = 0V, V_{DS} = −25V, f = 1.0 MHz
C_{oss}	Output Capacitance	—	300	—	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	—	100	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	30	60	ns	V_{DD} = −42V, I_D = −4.1A, Z_o = 50Ω
t_r	Rise Time	—	70	140	ns	See Fig. 17
$t_{d(off)}$	Turn-Off Delay Time	—	70	140	ns	(MOSFET switching times are essentially independent of operating temperature.)
t_f	Fall Time	—	70	140	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	25	45	nC	V_{GS} = −15V, I_D = −15A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	13	23	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	12	22	nC	
L_D	Internal Drain Inductance	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	—	15	—	nH	Measured from the source lead, 5 mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

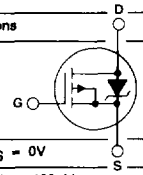


Thermal Resistance

$R\theta_{JC}$	Junction-to-Case	—	—	5.0*	°C/W	
$R\theta_{JA}$	Junction-to-Ambient	—	—	175	°C/W	Typical socket mount

Source-Drain Diode Ratings and Characteristics

Parameter		Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	−6.5*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
I_{SM}	Pulse Source Current (Body Diode) ②	—	—	−25	A	
V_{SD}	Diode Forward Voltage ①	—	—	−1.5	V	T_C = 25°C, I_S = −6.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	—	—	250	ns	T_J = 25°C, I_F = −6.5A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	—	1.8	—	μC	T_J = 25°C, I_F = −6.5A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



*JEDEC Registered Value

① Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

② Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

③ V_{DD} = 25V, starting T_J = 25°C, L = 17.25 mH, R_G = 25Ω, Peak I_L = 6.5A. (See Fig. 15 and 16)

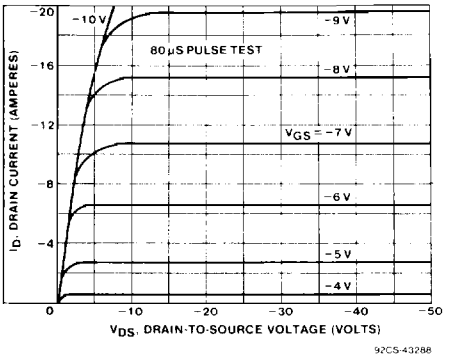


Fig. 1 - Typical Output Characteristics

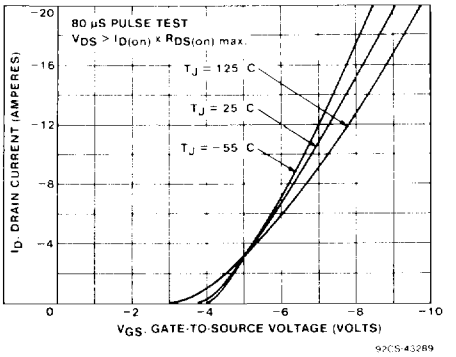


Fig. 2 - Typical Transfer Characteristics

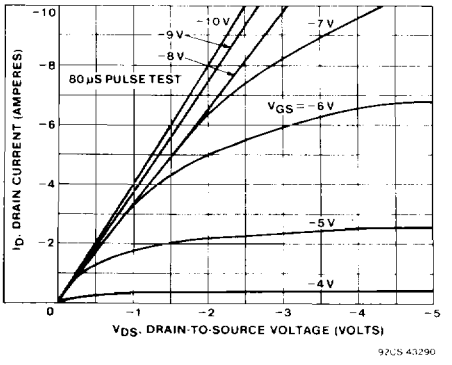


Fig. 3 - Typical Saturation Characteristics

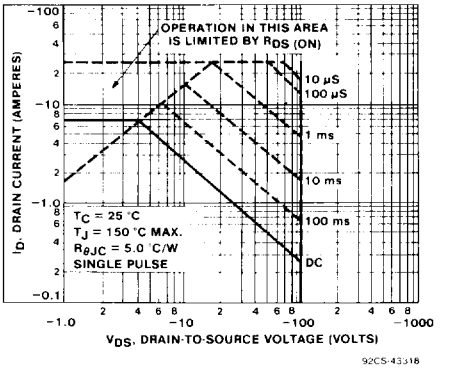


Fig. 4 - Maximum Safe Operating Area

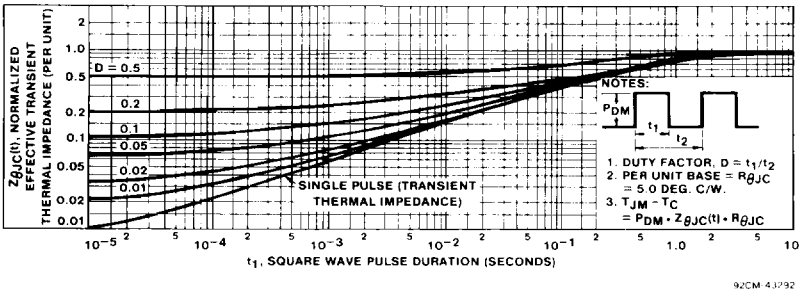


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

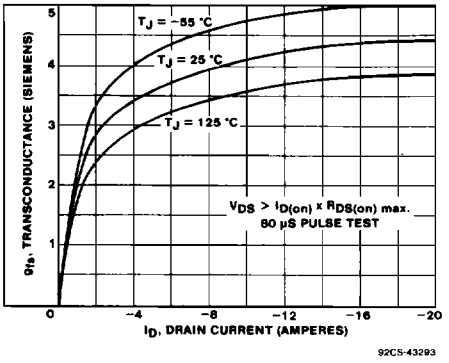


Fig. 6 - Typical Transconductance Vs. Drain Current

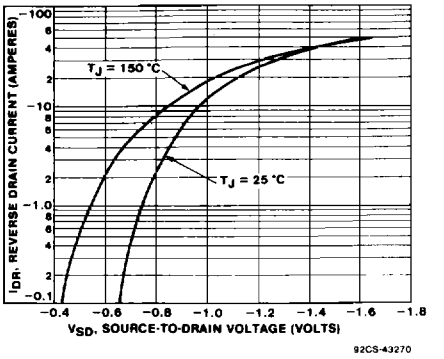


Fig. 7 - Typical Source-Drain Diode Forward Voltage

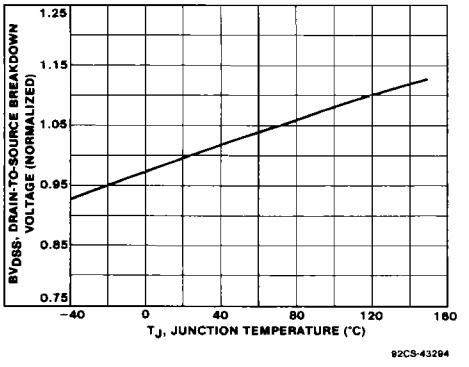


Fig. 8 - Breakdown Voltage Vs. Temperature

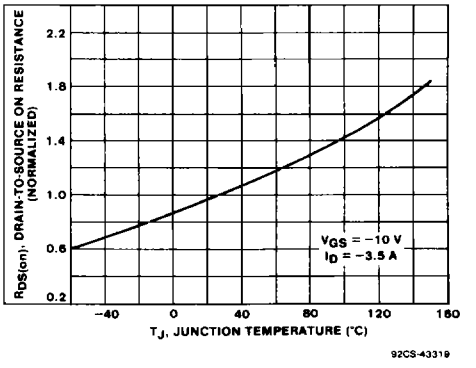


Fig. 9 - Normalized On-Resistance Vs. Temperature

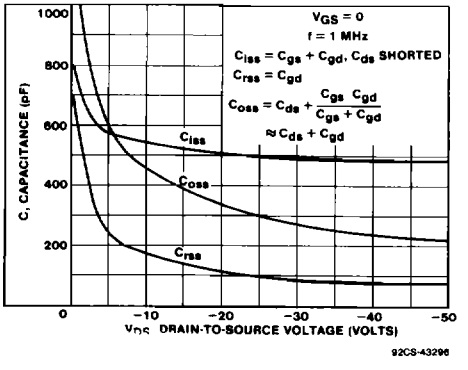


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

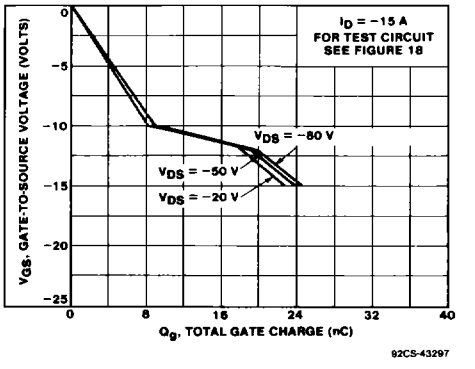


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

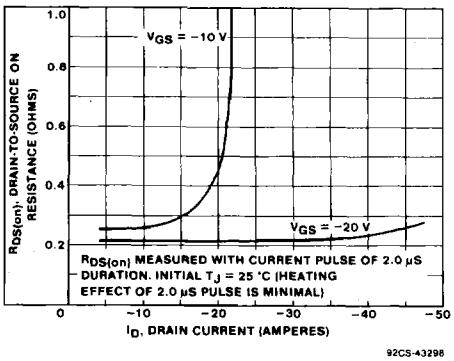


Fig. 12 - Typical On-Resistance Vs. Drain Current

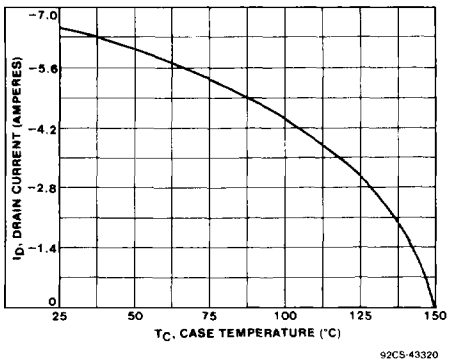


Fig. 13 - Maximum Drain Current Vs. Case Temperature

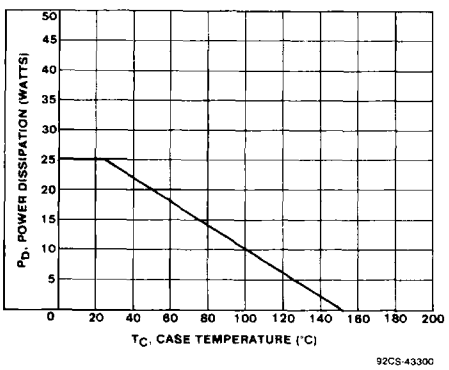


Fig. 14 - Power Vs. Temperature Derating Curve

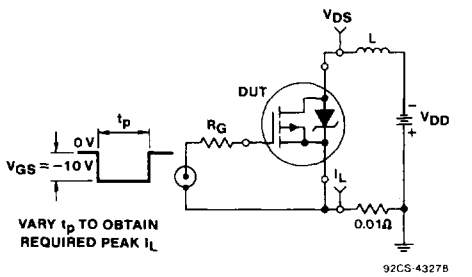


Fig. 15 - Unclamped Inductive Test Circuit

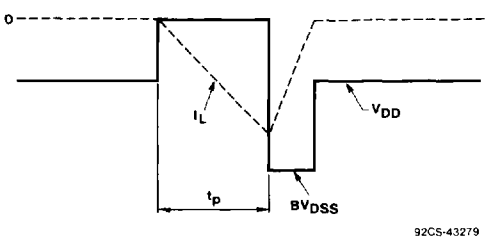


Fig. 16 - Unclamped Inductive Waveforms

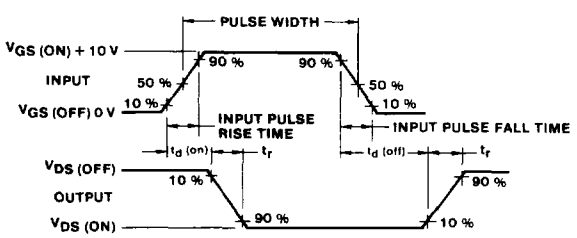


Fig. 17 - Switching Time Test Circuit

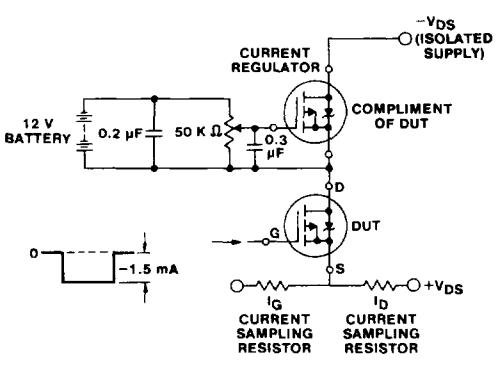


Fig. 18 - Gate Charge Test Circuit