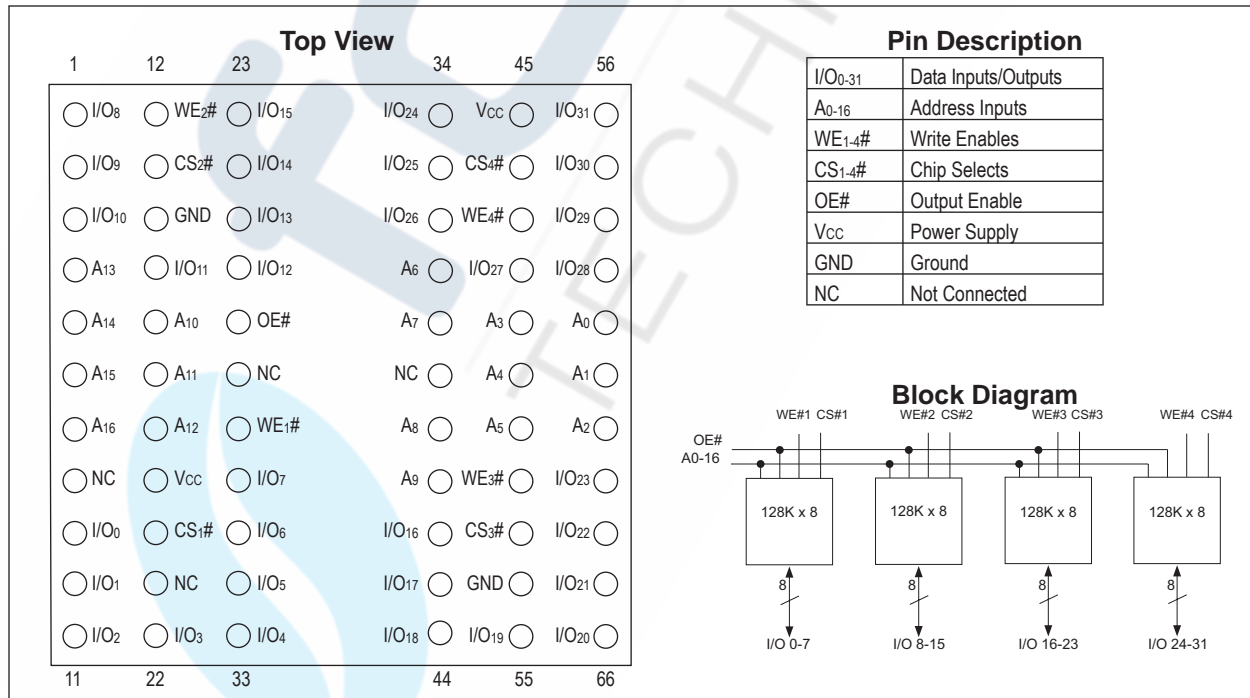


## 128Kx32 SRAM MODULE

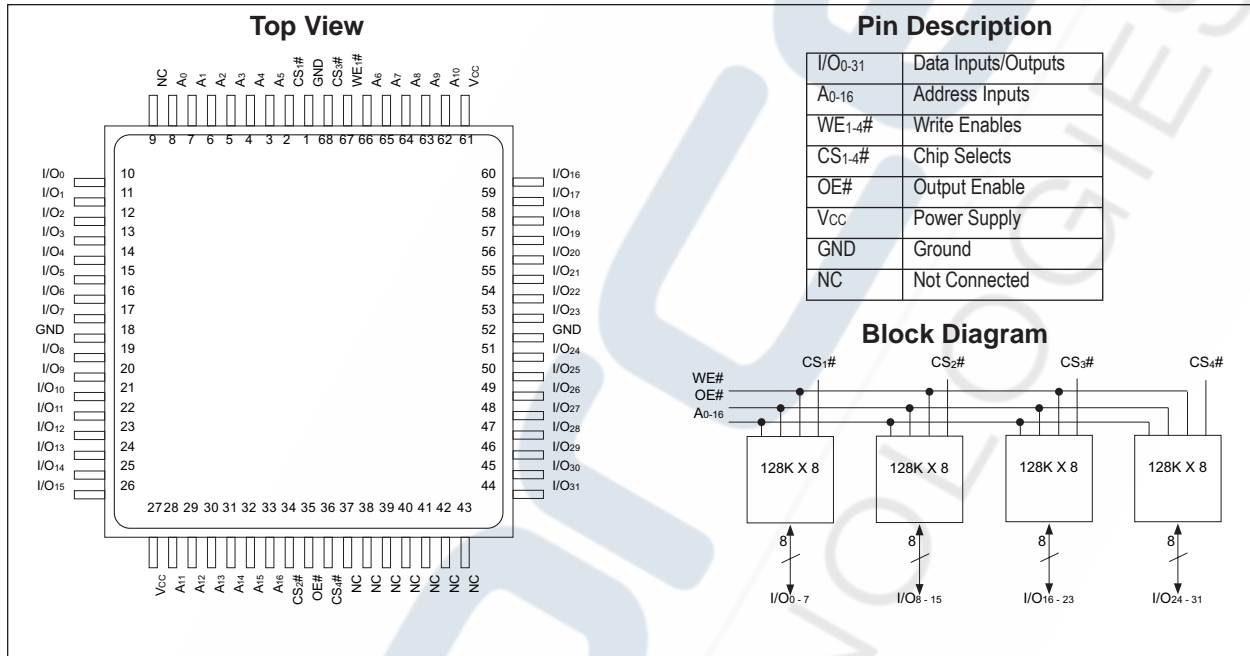
### FEATURES

- Access Times of 15, 17, 20, 25, 35, 45, 55ns
- MIL-STD-883 M5004 Devices Available
- Packaging
  - 66 pin, PGA Type, 1.075" square, Hermetic Ceramic HIP
  - 68 lead, 40mm CQFP (G4T)<sup>1</sup>, 3.56mm (0.140")
  - 68 lead, 22.4mm CQFP (G2U), 3.56mm (0.140"),
  - 68 lead, 22.4mm (0.880") square, CQFP (G2L), 5.08mm (0.200") high
- Organised as 128Kx32; User Configurable as 256Kx16 or 512Kx8
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Devices are upgradeable to 512Kx32

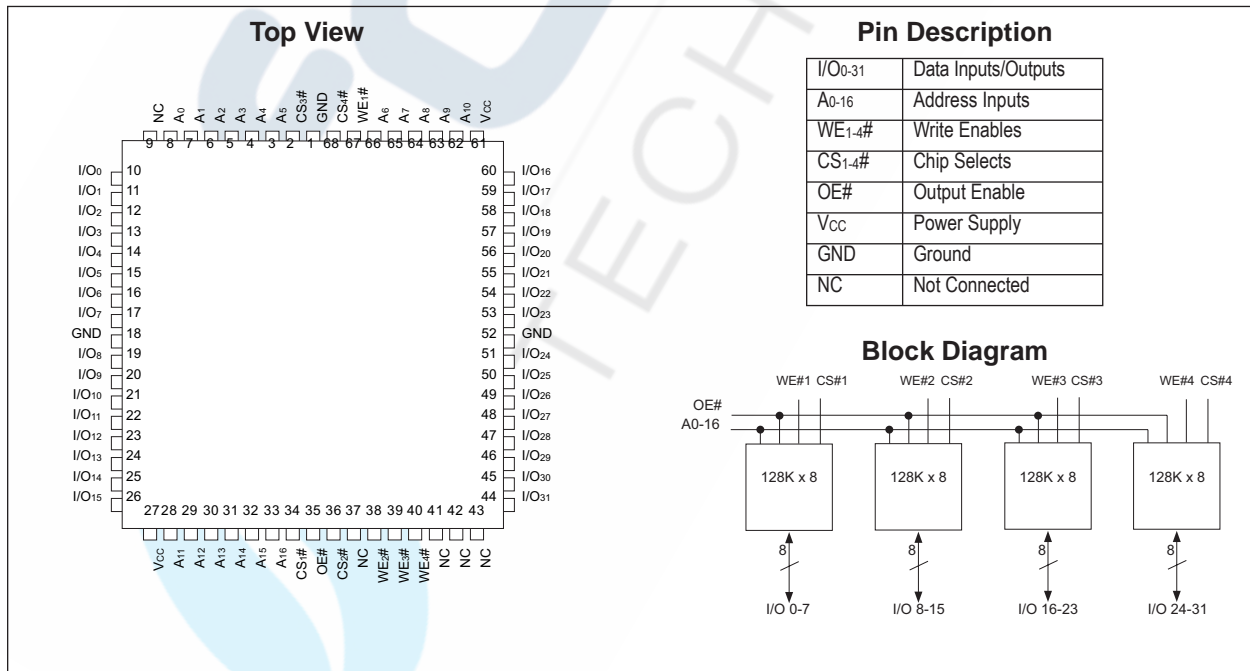
**FIGURE 1 – PIN CONFIGURATION FOR FTS128K32N-XH1X**



**FIGURE 2 – PIN CONFIGURATION FOR FTS128K32-XG4TX**



**FIGURE 3 – PIN CONFIGURATION FOR FTS128K32-XG2UX AND FTS128K32-XG2LX**



## ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T <sub>A</sub>	-55	+125	°C
Storage Temperature	T <sub>STG</sub>	-65	+150	°C
Signal Voltage Relative to GND	V <sub>G</sub>	-0.5	V <sub>CC</sub> +0.5	V
Junction Temperature	T <sub>J</sub>		150	°C
Supply Voltage	V <sub>CC</sub>	-0.5	7.0	V

## RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.5	V
Input High Voltage	V <sub>IH</sub>	2.2	V <sub>CC</sub> + 0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.5	+0.8	V
Operating Temp (Mil)	T <sub>A</sub>	-55	+125	°C

## TRUTH TABLE

CS	OE	WE	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

## CAPACITANCE

T<sub>A</sub> = +25°C

Parameter	Symbol	Conditions	Max	Unit
OE# capacitance	C <sub>OE</sub>	V <sub>IN</sub> = 0V, f = 1.0 MHz	50	pF
WE1-4# capacitance HIP (PGA) H1 CQFP G4T CQFP G2U/G2L	C <sub>WE</sub>	V <sub>IN</sub> = 0V, f = 1.0 MHz	20 50 20	pF
CS1-4# capacitance	C <sub>CS</sub>	V <sub>IN</sub> = 0V, f = 1.0 MHz	20	pF
Data# I/O capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0V, f = 1.0 MHz	20	pF
Address input capacitance	C <sub>AD</sub>	V <sub>IN</sub> = 0V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

## DC CHARACTERISTICS

V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter	Sym	Conditions	-15		-17		-20		-25		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub>		10		10		10		10	μA
Output Leakage Current	I <sub>LO</sub>	CS# = V <sub>IH</sub> , OE# = V <sub>IH</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub>		10		10		10		10	μA
Operating Supply Current	I <sub>CC</sub>	CS# = V <sub>IL</sub> , OE# = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5		600		600		600		600	mA
Standby Current	I <sub>SB</sub>	CS# = V <sub>IH</sub> , OE# = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5		80		80		80		60	mA
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8mA, V <sub>CC</sub> = 4.5		0.4		0.4		0.4		0.4	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0mA, V <sub>CC</sub> = 4.5	2.4		2.4		2.4		2.4		V

Parameter	Sym	Conditions	-35		-45		-55		Units
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub>		10		10		10	μA
Output Leakage Current	I <sub>LO</sub>	CS# = V <sub>IH</sub> , OE# = V <sub>IH</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub>		10		10		10	μA
Operating Supply Current	I <sub>CC</sub>	CS# = V <sub>IL</sub> , OE# = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5		600		600		600	mA
Standby Current	I <sub>SB</sub>	CS# = V <sub>IH</sub> , OE# = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5		60		60		60	mA
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8mA, V <sub>CC</sub> = 4.5		0.4		0.4		0.4	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0mA, V <sub>CC</sub> = 4.5	2.4		2.4		2.4		V

NOTE: DC test conditions: V<sub>IH</sub> = V<sub>CC</sub> - 0.3V, V<sub>IL</sub> = 0.3V

## DATA RETENTION CHARACTERISTICS (For FTS128K32L-XXX Only)

-55°C ≤ T<sub>A</sub> ≤ +125°C, -40°C ≤ T<sub>A</sub> ≤ +85°C

Characteristic	Sym	Conditions	Min	Typ	Max	Units
Data Retention Voltage	V <sub>CC</sub>	V <sub>CC</sub> = 2.0V	2	-	-	V
Data Retention Quiescent Current	I <sub>CCDR</sub>	CS# = V <sub>CC</sub> - 0.2V	-	1	2	mA
Chip Disable to Data Retention Time (1)	T <sub>CDR</sub>	V <sub>IN</sub> = V <sub>CC</sub> - 0.2V	0	-	-	ns
Operation Recovery Time (1)	T <sub>R</sub>	or V <sub>IN</sub> = 0.2V	TRC	-	-	ns

NOTE: Parameter guaranteed, but not tested.

## AC CHARACTERISTICS

$V_{CC} = 5.0V, GND = 0V, -55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter	Symbol	-15		-17		-20		-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	$t_{RC}$	15		17		20		25		35		45		55		ns
Address Access Time	$t_{AA}$		15		17		20		25		35		45		55	ns
Output Hold from Address Change	$t_{OH}$	0		0		0		0		0		0		0		ns
Chip Select Access Time	$t_{ACS}$		15		17		20		25		35		45		55	ns
Output Enable to Output Valid	$t_{OE}$		10		10		12		15		20		25		30	ns
Chip Select to Output in Low Z	$t_{OLZ}^1$	3		3		3		3		3		3		3		ns
Output Enable to Output in Low Z	$t_{OLZ}^1$	0		0		0		0		0		0		0		ns
Chip Disable to Output in High Z	$t_{CHZ}^1$		12		12		12		12		15		20		20	ns
Output Disable to Output in High Z	$t_{OHZ}^1$		12		12		12		12		15		20		20	ns

1. This parameter is guaranteed by design but not tested.

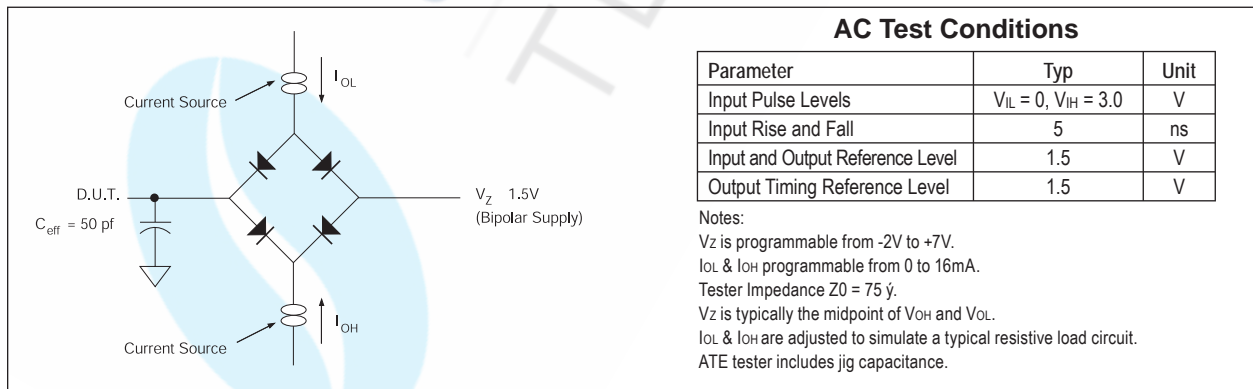
## AC CHARACTERISTICS

$V_{CC} = 5.0V, GND = 0V, -55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter	Symbol	-15		-17		-20		-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	$t_{WC}$	15		17		20		25		35		45		55		ns
Chip Select to End of Write	$t_{CW}$	14		14		15		20		25		30		45		ns
Address Valid to End of Write	$t_{AW}$	14		15		15		20		25		30		45		ns
Data Valid to End of Write	$t_{DW}$	10		10		12		15		20		25		25		ns
Write Pulse Width	$t_{WP}$	14		14		15		20		25		30		45		ns
Address Setup Time	$t_{AS}$	0		0		0		0		0		0		0		ns
Address Hold Time	$t_{AH}$	0		0		0		0		0		0		0		ns
Output Active from End of Write	$t_{OW}^1$	3		3		3		3		4		4		4		ns
Write Enable to Output in High Z	$t_{WHZ}^1$		10		10		12		15		20		25		25	ns
Data Hold Time	$t_{DH}$	0		0		0		0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

FIGURE 4 – AC TEST CIRCUIT



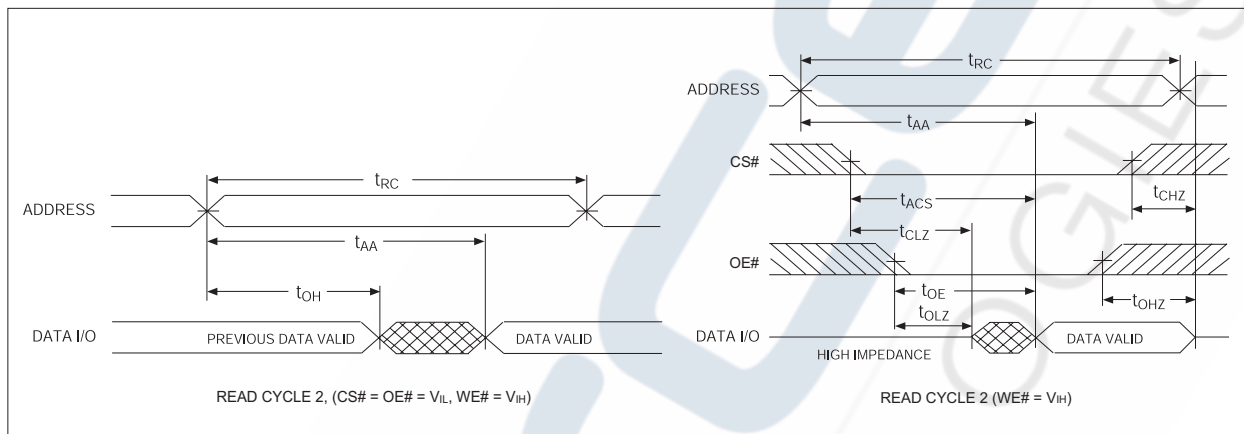
### AC Test Conditions

Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0, V_{IH} = 3.0$	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

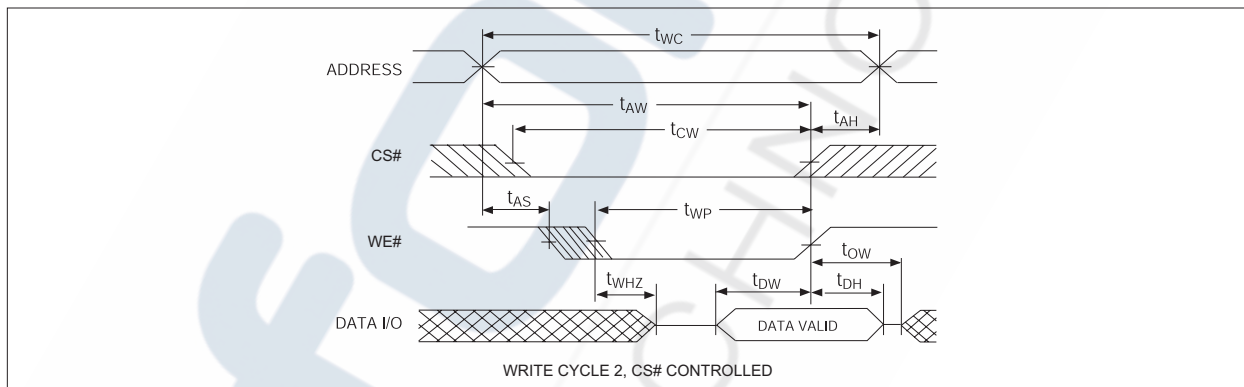
#### Notes:

$V_Z$  is programmable from -2V to +7V.  
 $I_{OL}$  &  $I_{OH}$  programmable from 0 to 16mA.  
 Tester Impedance  $Z_0 = 75 \Omega$ .  
 $V_Z$  is typically the midpoint of  $V_{OH}$  and  $V_{OL}$ .  
 $I_{OL}$  &  $I_{OH}$  are adjusted to simulate a typical resistive load circuit.  
 ATE tester includes jig capacitance.

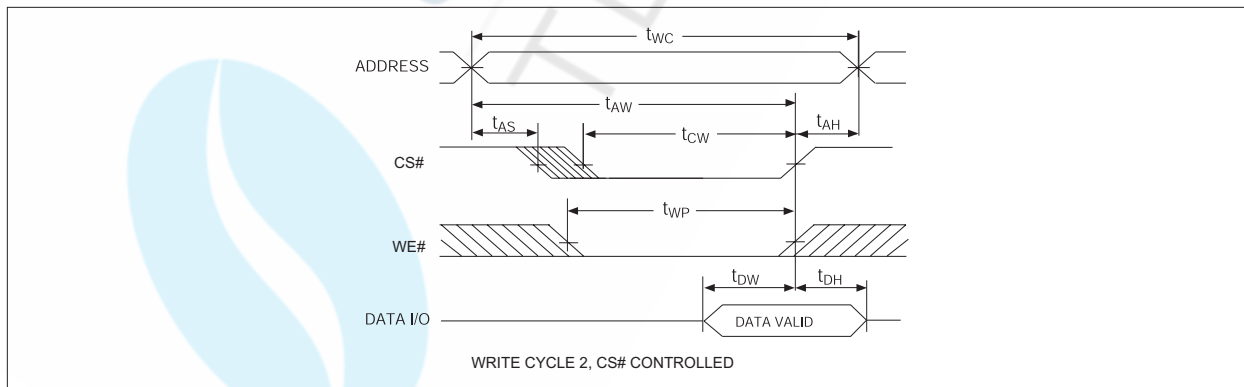
**FIGURE 5 – TIMING WAVEFORM - READ CYCLE**



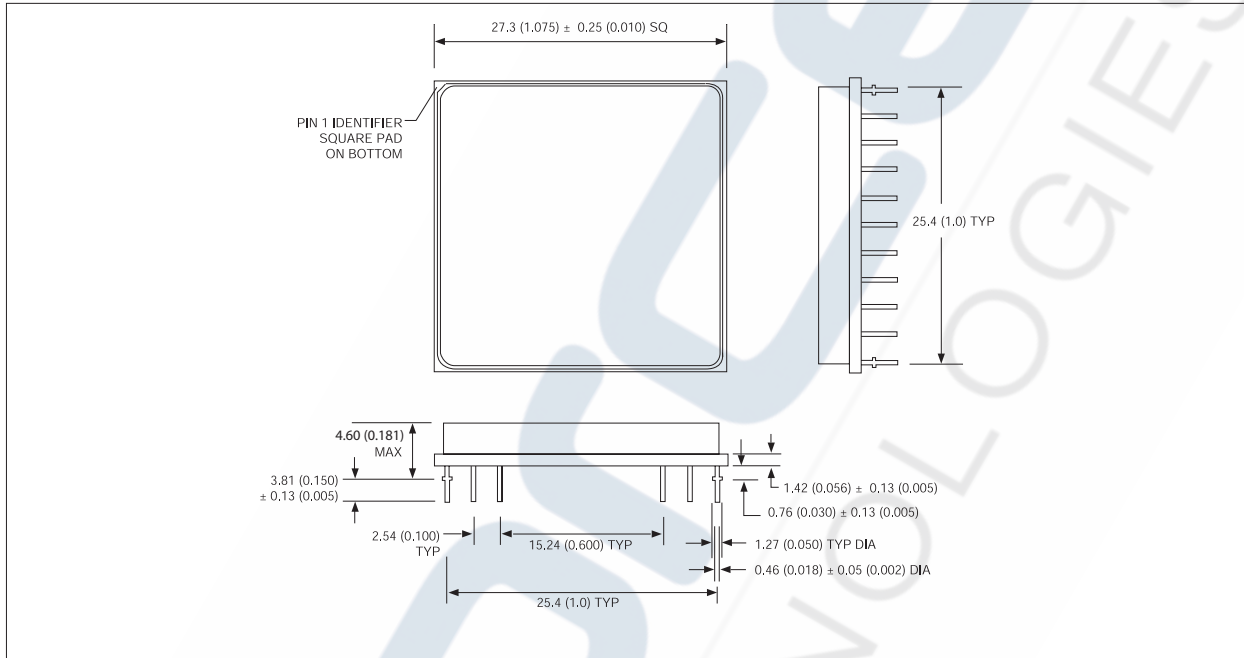
**FIGURE 6 – WRITE CYCLE - WE# CONTROLLED**



**FIGURE 7 – WRITE CYCLE - CS# CONTROLLED**



**66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, )**





## ORDERING INFORMATION

**FT S 128K 32 X - XXX X X X**

**LEAD FINISH:**

Blank = Gold plated leads  
 A = Solder dip leads

**DEVICE GRADE:**

Q = MIL-STD-883 Compliant  
 M = Military Screened -55°C to +125°C  
 I = Industrial -40°C to +85°C  
 C = Commercial 0°C to +70°C

**PACKAGE TYPE:**

H1 = 1.075" sq. Ceramic Hex-In-line Package,  
 G2U = 22.4mm Ceramic Quad Flat Pack, CQFP  
 G2L = 22.4mm Ceramic Quad Flat Pack, CQFP

**ACCESS TIME (ns)**

**IMPROVEMENT MARK:**

N = No Connect at pin 8, 21, 28 and 39 in HIP for Upgrades  
 L = Low Power\*

**ORGANISATION, 128Kx32**

User configurable as 256Kx16 or 512Kx8

**SRAM**

**FORCE TECHNOLOGIES**

\* Low Power Data Retention only available in G2U, G2L, PackageTypes





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