OKI semiconductor

MSM5165AL

8,192-Word x 8-Bit CMOS STATIC RAM

GENERAL DESCRIPTION

The MSM5165AL is a 8192-word by 8-bit CMOS static RAM featuring a 5V power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to use. The MSM5165AL is also a CMOS silicon gate device that requires very low power during standby (standby current of 100 μA) when there is no chip selection.
A byte system is adopted, and since pins are compatible with standard ultraviolet EPROMs, this device is ideal to use as a peripheral memory for microcomputers and data terminal units, etc. The pins $\overline{CE}_1$, CE_2 and $\overline{OE}$ are provided as control signals that permit the outputs to be tri-stated, allowing easy memory expansion on a system bus.

FEATURES

- Single 5V Supply
- 0°C ~ 70°C
- Low Power Dissipation
  Standby: 0.55 mW MAX
  Operation: 330 mW MAX
- High Speed (Equal Access and Cycle Time)
  100-120 ns MAX
- Direct TTL Compatible (Input and Output)
- 3-State Output
- Pin Compatibility with 64K EPROM (MSM2764)
- 28-pin DIP PKG
- 28-pin FLAT PKG

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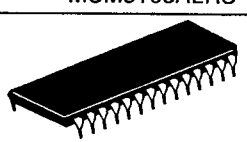
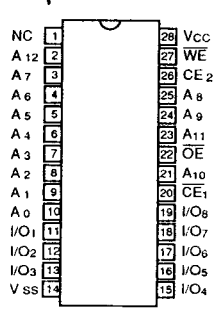
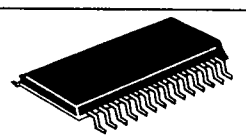
PIN CONFIGURATION (TOP VIEW)

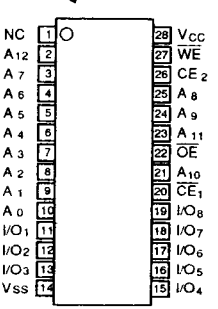
MSM5165ALRS





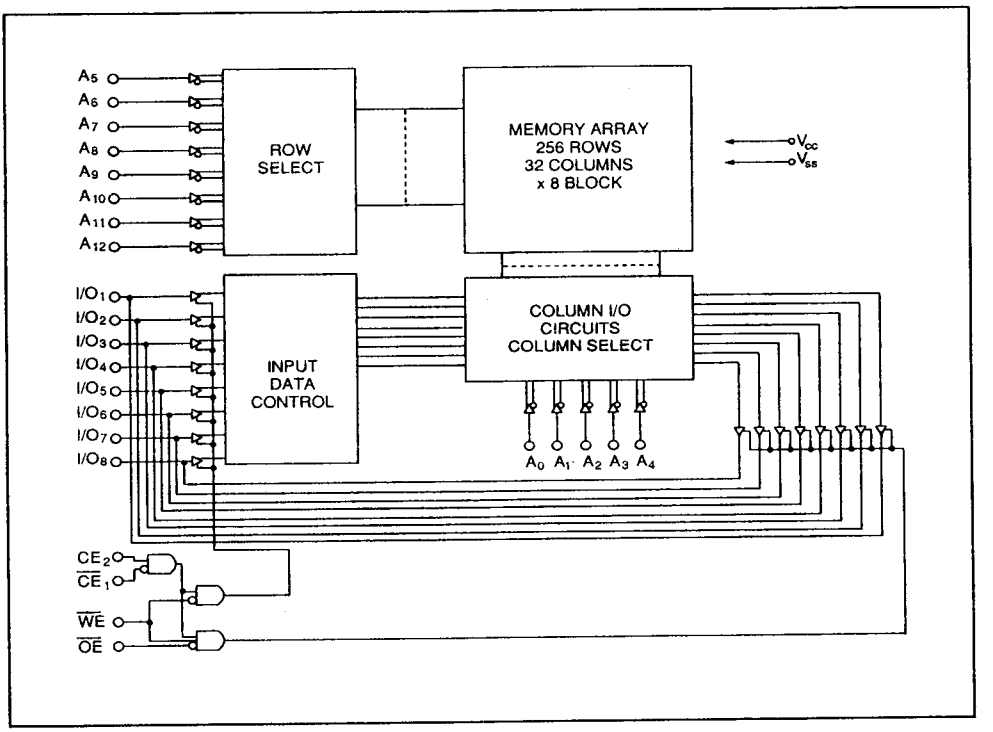
MSM5165ALGS





Pin Names	Function
A_0 ~ A_{12}	Address input
I/O_1 ~ I/O_8	Data input/output
$\overline{CE}_1$, CE_2	Chip select
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
Vcc, Vss	Supply voltage

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

Mode/Pins	$\overline{CE}_1$	CE_2	$\overline{WE}$	$\overline{OE}$	I/O Operation
Standby	H	X	X	X	High Z
	X	L	X	X	
Read	L	H	H	H	High Z
	L	H	H	L	D_{OUT}
Write	L	H	L	X	D_{IN}

X: H or L

ELECTRICAL CHARACTERISTICS
ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit
Supply Voltage	V_{CC}	Referenced to GND	-0.3~7.0	V
Input Voltage	V_{IN}		-0.3*~V_{CC} +0.3	V
Operating Temperature	T_{opr}	———	0~70	°C
Storage Temperature	T_{stg}	———	-55~150	°C
Power Dissipation	P_D	T_a = 25°C	1.0	W

* Pulse Width < 30 ns: -3.0V MIN

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Supply Voltage	V_{CC}	5V ± 10%	4.5	5	5.5	V
	V_{SS}	———	—	0	—	V
Data Retention Voltage	V_{CCH}	———	2	5	5.5	V
Input Voltage	V_{IH}	5V ± 10%	2.2	—	V_{CC}+0.3	V
	V_{IL}		-0.3*	—	0.8	V
Output Voltage	C_L	———	—	—	100	pF
	TTL		—	—	1	—

* Pulse Width < 30 ns: -3.0V MIN

DC CHARACTERISTICS

(V_{CC} = 5V ± 10%, Ta = 0 ~ 70°C)

Parameter	Symbol	Conditions	MSM5165AL			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 0~V_{CC}	-1	—	1	µA
Output Leakage Current	I_{LO}	$\overline{CE_1}$=V_{IH} or CE_2=V_{IL} or $\overline{OE}$ = V_{IH} $V_{I/O}$=0~V_{CC}	-1	—	1	µA
Output Voltage	V_{OH}	I_{OH} = -1mA	2.4	—	—	V
	V_{OL}	I_{OL} = 2.1mA	—	—	0.4	V
Standby Supply Current	I_{CCS}	$\overline{CE_1} \geqq V_{CC}$ -0.2 V, $CE_2 \geqq V_{CC}$ -0.2V V_{IN} =0~V_{CC}	—	2	100	µA
		$CE_2 \leqq 0.2V$ V_{IN} =0~V_{CC}				
	I_{CCS1}	$\overline{CE_1}$ = V_{IH} , CE_2 = V_{IL}	—	—	3	mA
Operating Supply Current	I_{CCA}	T_{CYC} = Min Cycle, I_{OUT} = 0 mA	—	—	①	mA
		T_{CYC} = 1 µs, I_{OUT} = 0 mA			15	

① 5165AL-10 60 mA 5165AL-12 55 mA

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AC CHARACTERISTICS

Test Condition

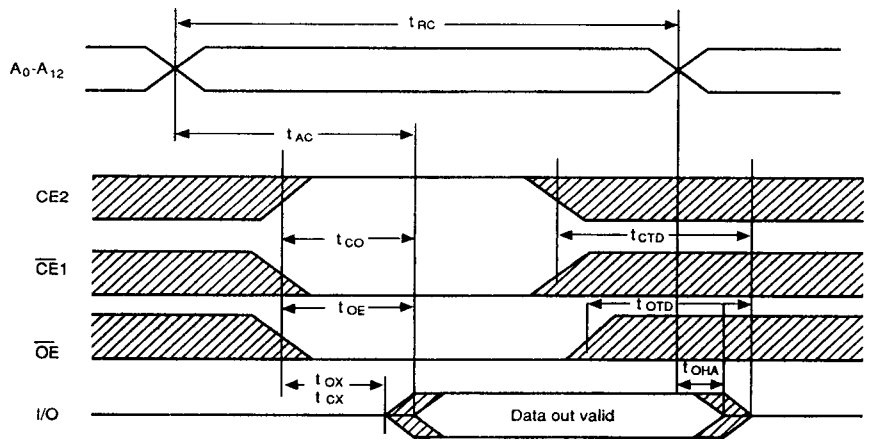
Parameter	Conditions
Input Pulse Level	V_{IH} = 2.4V, V_{IL} = 0.6V
Input Rise and Fall Times	10 ns
I/O Timing Reference Level	1.5V
Output Load	C_L=100pF, 1TTL Gate

READ CYCLE

(Vcc = 5 V ±10%, Ta = 0 ~ +70°C)

Parameter	Symbol	MSM5165AL-10		MSM5165AL-12		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	100	—	120	—	ns
Address Access Time	t_{AC}	—	100	—	120	ns
Chip Enable Access Time	t_{CO}	—	100	—	120	ns
Output Enable to Output Valid	t_{OE}	—	50	—	60	ns
Chip Selection to Output Active	t_{CX}	10	—	10	—	ns
Output Hold Time from Address Change	t_{OHA}	10	—	10	—	ns
Output 3-State from Output Disable	t_{OTD}	—	35	—	40	ns
Output 3-State from Chip Deselection	t_{CTD}	—	50	—	60	ns
Output Enable to Output Active	t_{OX}	5	—	5	—	ns

READ CYCLE



Notes: 1. A Read occurs during the overlap of a low $\overline{CE}_1$, a high CE_2, a low $\overline{OE}$ and a high $\overline{WE}$.
2. t_{CX} is specified from $\overline{CE}_1$ or CE_2 whichever occurs last.
3. t_{CTD} is specified from $\overline{CE}_1$ or CE_2 whichever occurs first.
4. t_{CTD} and t_{OTD} are specified by the time when DATA OUT is floating.

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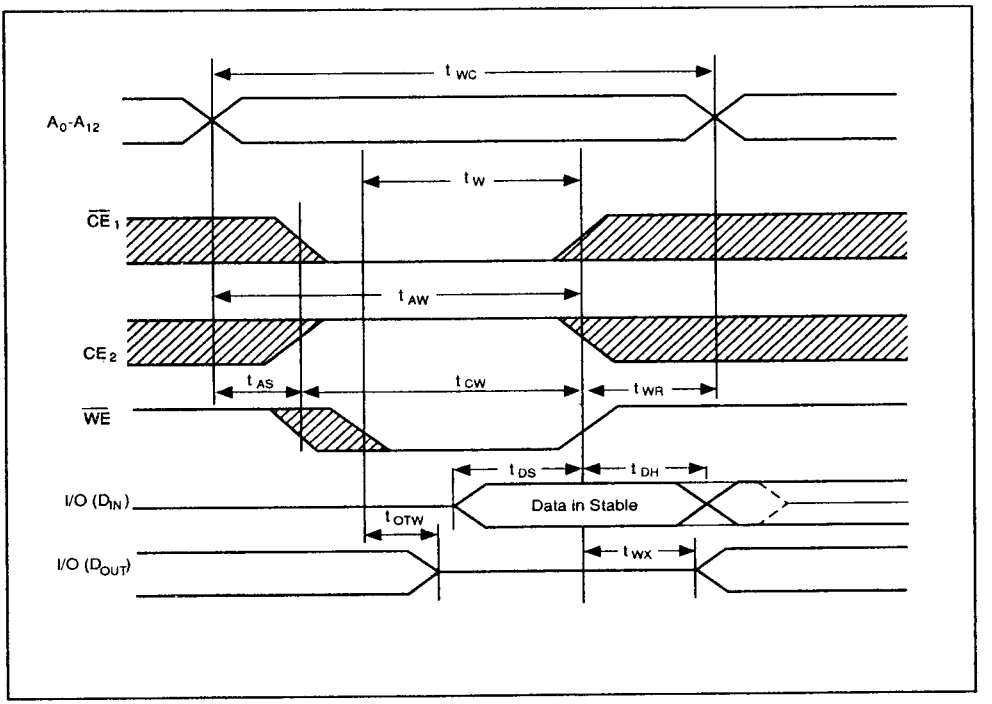
WRITE CYCLE

(Vcc = 5 V ±10%, Ta = 0 ~ +70°C)

Parameter	Symbol	MSM5165AL-10		MSM5165AL-12		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	100	—	120	—	ns
Address to Write Setup Time	t_{AS}	0	—	0	—	ns
Write Time	t_W	60	—	70	—	ns
Write Recovery Time	t_{WR}	15	—	15	—	ns
Data Setup Time	t_{DS}	40	—	50	—	ns
Data Hold from Write Time	t_{DH}	0	—	0	—	ns
Output 3-State from Write	t_{OTW}	0	35	0	40	ns
Chip Selection to End of Write	t_{CW}	80	—	100	—	ns
Address Valid to End of Write	t_{AW}	80	—	100	—	ns
Output Active from End of Write	t_{WX}	5	—	5	—	ns

Notes: 1. A Write Cycle occurs during the overlap of a low $\overline{CE}_1$, a high CE_2 and a low $\overline{WE}$.
2. $\overline{OE}$ may be both high and low in a Write Cycle.
3. t_{AS} is specified from $\overline{CE}_1$, CE_2 or $\overline{WE}$, whichever occurs last.
4. t_W is an overlap time of a low $\overline{CE}_1$, a high CE_2 and a low $\overline{WE}$.
5. t_{WR}, t_{DS} and t_{DH} are specified from $\overline{CE}_1$, CE_2 or $\overline{WE}$, whichever occurs first.
6. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
7. When I/O pins are Data output mode, don't force inverse signals to those pins.

WRITE CYCLE



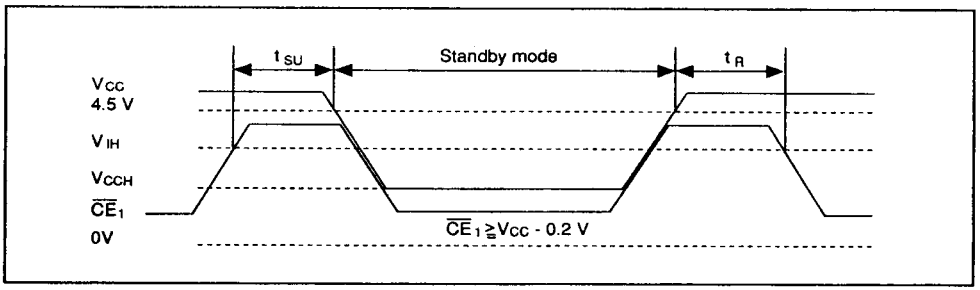
LOW Vcc DATA RETENTION CHARACTERISTICS

(Ta = 0 ~ +70°C, unless otherwise noted)

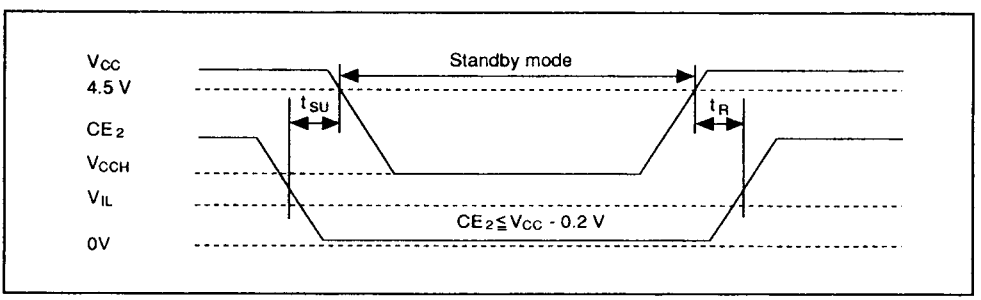
Parameter	Symbol	Conditions	Value			Unit
			Mix.	Typ.	Max.	
V_{CC} for Data Retention	V_{CCH}	$\overline{CE}_1 \geqq V_{CC}$ -0.2V, $CE_2 \geqq V_{CC}$ -0.2V $CE_2 \leqq 0.2V$	2	—	5.5	V
Data Retention Current	I_{CCH}	V_{CC}=3V, $\overline{CE}_1 \geqq V_{CC}$ -0.2V $CE_2 \geqq V_{CC}$ -0.2V	—	1	50*	μA
		V_{CC}=3V, $CE_2 \leqq 0.2V$				
CS to Data Retention Time	t_{SU}	———	0	—	—	ns
Operation Recovery Time	t_R	———	** t_{RC}	—	—	ns

* Ta = 0 to 40°C: 15 μA MAX
** t_{RC} : Read Cycle Time

$\overline{CE_1}$ CONTROL



CE_2 CONTROL



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CAPACITANCE

(Ta=25°C, f=1MHz)

Parameter	Symbol	Conditions	Value		Unit
			Min.	Max.	
I/O Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	10	pF
Input Capacitance	C_{IN}	V_I = 0V	—	6	pF

Note: This parameter is periodically sampled and not 100% tested.