



Integrated Device Technology, Inc.

### 3.3V PENTIUM™ CLOCK SYNTHESIZER

### IDT74FCT3907 ADVANCE INFORMATION

#### FEATURES:

- 0.5 MICRON CMOS Technology
- Generates keyboard, floppy disk, system reference, PCI and CPU clocks
- 6 copies of PCI clock & 4 copies of CPU clock available
- 14.31818MHz crystal input
- CPU clock output skew <250ps  
Bus clock output skew <500ps
- 0.03% output frequency accuracy
- Power-on reset
- Selectable CPU clock frequency (50/60/66.66MHz)
- Internal loop filter
- Vcc = 3.3 ±0.3V
- Available in 28 pin SOIC
- Supports Pentium™ processor based designs
- Meets Intel Pentium™ processor 3.3V Clock Driver specification (External Draft 1.0)

#### DESCRIPTION:

The IDT74FCT3907 Clock synthesizer is built using advanced dual metal CMOS technology. This device uses a 14.31818 MHz crystal input to synthesize the various motherboard clock frequencies.

The output frequencies supported by the IDT74FCT3907 are as follows:

Reference clocks (2) = 14.31818MHz

Keyboard clock (1) = 12MHz

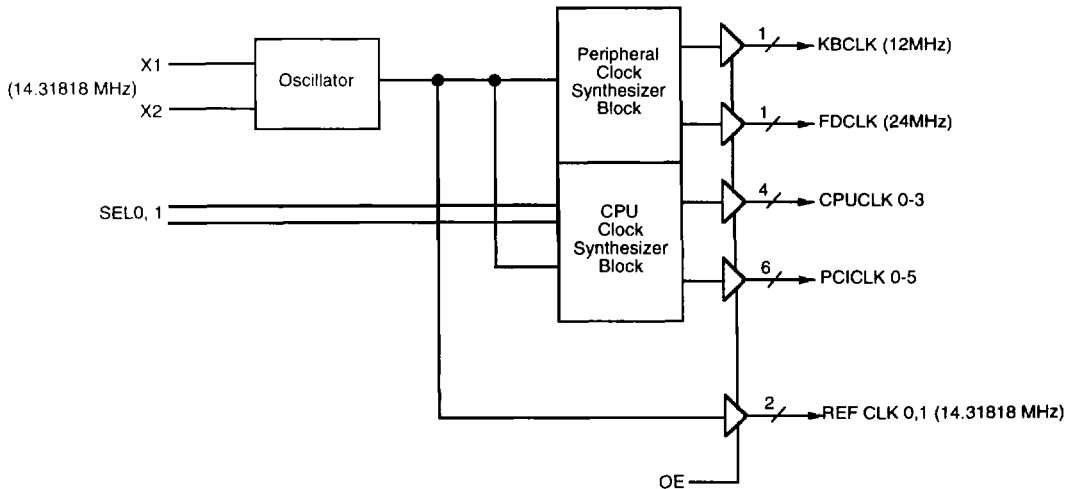
Floppy disk clock (1) = 24MHz

CPU clock (4) = 50/60/66.66 MHz (Selectable by SEL pins)

Bus clock (6) = CPU clock ÷ 2

The SEL0, 1 pins are used to choose appropriate CPUCLK and PCICLK frequencies or to put the device in a test mode. In the test mode, the device outputs various divisors of the test clock frequency. Refer to the function table in this datasheet for details on the different operating modes.

#### FUNCTIONAL BLOCK DIAGRAM



3245 drw 01

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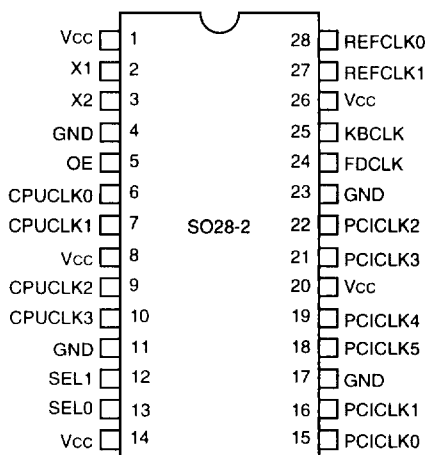
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#### COMMERCIAL TEMPERATURE RANGES

AUGUST 1995

## PIN CONFIGURATION



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## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Rating	Commercial	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
V <sub>TERM</sub> <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to V <sub>CC</sub> + 0.5	V
T <sub>A</sub>	Operating Temperature	0 to 70	°C
T <sub>BIAS</sub>	Temperature Under Bias	0 to +70	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	°C
I <sub>OUT</sub>	DC Output Current	-60 to +60	mA

### NOTES:

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- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stressing rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>CC</sub> terminals.
- Input, Output and I/O terminals.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4.5	6.0	pF
C <sub>I/O</sub>	I/O Capacitance	V <sub>OUT</sub> = 0V	5.5	8.0	pF

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### NOTE:

- This parameter is measured at characterization but not tested.

## PIN DESCRIPTION

Pin Name	I/O	Description
X1	I	14.31818 MHz Crystal Input. This is also the test clock input.
X2	O	14.31818 MHz Crystal Output
SEL0, 1	I	CPUCLK Control Inputs
KBCLK	O	Keyboard Clock (12MHz)
FDCLK	O	Floppy Disk Clock (24MHz)
REFCLK 0, 1	O	Reference Clocks (14.31818 MHz)
CPUCLK 0-3	O	CPU Clocks
PCICLK 0-5	O	PCI Bus Clocks
OE	I	Output Enable

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## FUNCTION TABLE

OE	SEL0	SEL1	INPUT CLK	CPUCLK	PCICLK	REFCLK	FDCLK	KBCLK
0	X	X	14.31818MHz	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1	0	0	14.31818MHz	50MHz	CPUCLK/2	14.31818MHz	24MHz	12MHz
1	0	1	14.31818MHz	60MHz	CPUCLK/2	14.31818MHz	24MHz	12MHz
1	1	0	14.31818MHz	66.66MHz	CPUCLK/2	14.31818MHz	24MHz	12MHz
1	1	1	TCLK (Test Clock)	TCLK/2	TCLK/4	TCLK	TCLK/4	TCLK/8

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**DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE**

Following Conditions Apply Unless Otherwise Specified:  
Commercial:  $T_A = 0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ ,  $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit	
V <sub>IH</sub>	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level	2.0	—	5.5	V	
	Input HIGH Level (I/O pins)		2.0	—	V <sub>CC</sub> +0.5		
V <sub>IL</sub>	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V	
I <sub>IH</sub>	Input HIGH Current (Input pins) <sup>(5)</sup>	V <sub>CC</sub> = Max. V <sub>I</sub> = 5.5V	—	—	±1	µA	
	Input HIGH Current (I/O pins) <sup>(5)</sup>		V <sub>I</sub> = V <sub>CC</sub>	—	±1		
I <sub>IL</sub>	Input LOW Current (Input pins) <sup>(5)</sup>		V <sub>I</sub> = GND	—	—		±1
	Input LOW Current (I/O pins) <sup>(5)</sup>		V <sub>I</sub> = GND	—	—		±1
I <sub>OZH</sub>	High Impedance Output Current (3-State Output pins) <sup>(16)</sup>	V <sub>CC</sub> = Max. V <sub>O</sub> = V <sub>CC</sub>	—	—	±1	µA	
			V <sub>O</sub> = GND	—	—		±1
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>CC</sub> = Min., I <sub>IIN</sub> = -18mA	—	-0.7	-1.2	V	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min. I <sub>OH</sub> = -0.1mA	V <sub>CC</sub> -0.2	—	—	V	
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -8mA COM'L.	V <sub>CC</sub> -0.6V	3.0	—		
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min. I <sub>OL</sub> = 0.1mA	—	—	0.2	V	
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 8mA	—	0.3	0.5		
I <sub>OS</sub>	Short Circuit Current <sup>(4,6)</sup>	V <sub>CC</sub> = Max., V <sub>O</sub> = GND <sup>(3)</sup>	-43	-135	-206	mA	
I <sub>OS</sub>	Short Circuit Current <sup>(4,7)</sup>	V <sub>CC</sub> = Max., V <sub>O</sub> = GND <sup>(3)</sup>	-34	-135	-195	mA	
I <sub>CCZ</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = GND or V <sub>CC</sub>	—	3.0	4.0	mA	

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**NOTES:**

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- The test limit for this parameter is ±5µA at T<sub>A</sub> = -55°C.
- Applies to CPUCLK.
- Applies to PCICLK.

**DYNAMIC OUTPUT DRIVE CHARACTERISTICS**

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit
I <sub>ODH</sub>	CPUCLK Output HIGH Current	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> = 2.4V	V <sub>CC</sub> = 3.135V (3.3V -5%)	-23	—	mA
		V <sub>CC</sub> = 3.465V (3.3V +5%)	—	—	-109	
I <sub>ODH</sub>	PCICLK Output HIGH Current	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> = 2.4V	V <sub>CC</sub> = 3.135V	-14.5	—	mA
		V <sub>CC</sub> = 3.465V	—	—	-100	
I <sub>ODL</sub>	CPUCLK Output LOW Current	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> = 0.4V	V <sub>CC</sub> = 3.135V	16	—	mA
		V <sub>CC</sub> = 3.465V	—	—	40	
I <sub>ODL</sub>	PCICLK Output LOW Current	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> = 0.4V	V <sub>CC</sub> = 3.135V	9.4	—	mA
		V <sub>CC</sub> = 3.465V	—	—	38	

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**NOTES:**

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- The test limit for this parameter is ±5µA at T<sub>A</sub> = -55°C.



**OSCILLATOR CHARACTERISTICS OVER OPERATING RANGE**

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit
Cx1	X1 Input Capacitance			20		pF
Cx2	X2 Output Capacitance			20		pF
I <sub>IH</sub>	X1 Input HIGH Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>CC</sub>		5		μA
I <sub>IL</sub>	X1 Input LOW Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = GND		-5		μA
I <sub>ODH</sub>	X2 Output HIGH Current	V <sub>OUT</sub> = V <sub>CC</sub>		-1		mA
I <sub>ODL</sub>	X2 Output LOW Current	V <sub>OUT</sub> = GND		1		mA

**NOTES:**

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1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.
3. This parameter is guaranteed but not tested.

**POWER SUPPLY CHARACTERISTICS**

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit				
ΔI <sub>CC</sub>	Quiescent Power Supply Current TTL Inputs HIGH	V <sub>CC</sub> = Max. V <sub>IN</sub> = V <sub>CC</sub> - 0.6V		—	2.0	30	μA				
I <sub>C</sub>	Total Power Supply Current	V <sub>CC</sub> = Max. Outputs Open 50% Duty Cycle OE = V <sub>CC</sub>	<table border="1"> <tr> <td>CPUCLK = 50MHz</td> <td rowspan="3">V<sub>IN</sub> = V<sub>CC</sub> V<sub>IN</sub> = GND</td> </tr> <tr> <td>CPUCLK = 60MHz</td> </tr> <tr> <td>CPUCLK = 66.66MHz</td> </tr> </table>	CPUCLK = 50MHz	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND	CPUCLK = 60MHz	CPUCLK = 66.66MHz	—			mA
CPUCLK = 50MHz	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND										
CPUCLK = 60MHz											
CPUCLK = 66.66MHz											

**NOTES:**

3245 tbl 08

1. Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.
2. Per TTL driven input (V<sub>IN</sub> = V<sub>CC</sub> - 0.6V); all other inputs at V<sub>CC</sub> or GND.

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**

Symbol	Parameter	Condition <sup>(1)</sup>	74FCT3907						Unit
			66.66MHz		60MHz		50MHz		
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
tCPU	CPUCLK Period	TBD	15	—	16.7	—	20	—	ns
tCPUH	CPUCLK HIGH Time <sup>(3)</sup>		4	—	4	—	4	—	ns
tCPL	CPUCLK LOW Time <sup>(4)</sup>		4	—	4	—	4	—	ns
tR1, tF1	CPUCLK Rise, Fall Times (Between 0.4V & 2.4V)		0.8	2.0	0.8	2.0	0.8	2.0	ns
tSK1(o)	CPUCLK Output Skew		—	250	—	250	—	250	ps
tSK1(p)	CPUCLK Pulse Skew  tPLH-tPHL		—	—	—	—	—	—	ps
tPCI	PCICLK Period		30	—	33.3	—	40	—	ns
tPCIH	PCICLK HIGH Time		12	—	13.3	—	16	—	ns
tPCIL	PCICLK LOW Time		12	—	13.3	—	16	—	ns
tR2, tF2	PCICLK Rise, Fall Time (Between 0.4V & 2.4V)		0.5	2.0	0.5	2.0	0.5	2.0	ns
tSK2(o)	PCICLK Output Skew		—	500	—	500	—	500	ps
tSK2(p)	PCICLK Pulse Skew  tPLH-tPHL		—	—	—	—	—	—	ps
tSK3(o)	CPUCLK to PCICLK Output Delay		1.0	5.0	1.0	5.0	1.0	5.0	ns
tPS	CPUCLK, PCICLK Period Stability		—	250	—	250	—	250	ps
tCLOCK	CPUCLK Lock Time		—	2	—	2	—	2	ms
tPLOCK	PCICLK Lock Time		—	3	—	3	—	3	ms
tPZL	Output Enable Time OE to KBCLK, FDCLK, REFCLK, CPUCLK, PCICLK (Test Mode)		1.5	8.0	1.5	8.0	1.5	8.0	ns
tPLZ	Output Disable Time OE to KBCLK, FDCLK, REFCLK, CPUCLK, PCICLK (Test Mode)		1.5	8.0	1.5	8.0	1.5	8.0	ns

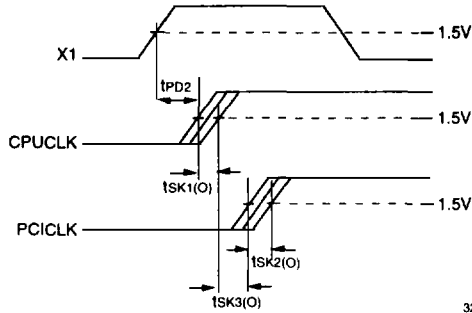
**NOTES:**

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

3245 tbl 09

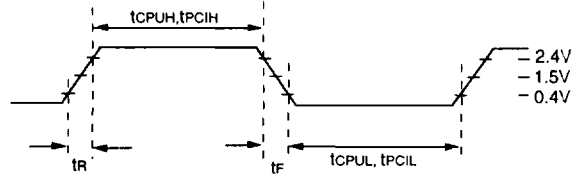
**TEST WAVEFORMS**

**PROPAGATION DELAY, OUTPUT SKEW**



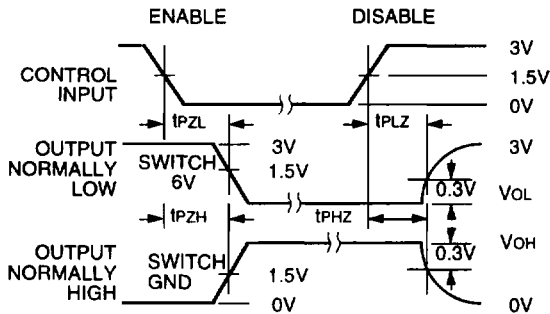
3245 drw 03

**PULSE WIDTH, RISE/FALL TIMES**



3245 drw 04

**ENABLE AND DISABLE TIMES**

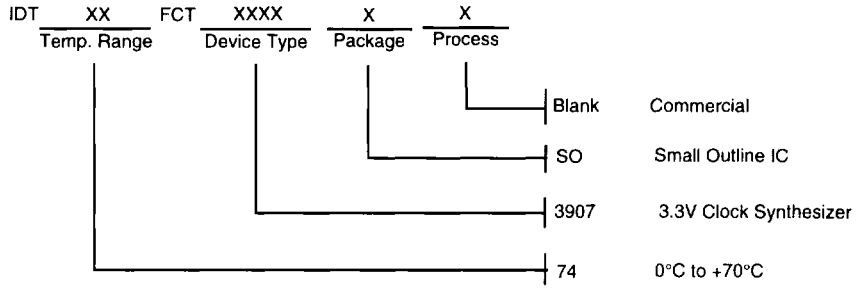


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**NOTES:**

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_F \leq 2.5\text{ns}$ ;  $t_R \leq 2.5\text{ns}$

**ORDERING INFORMATION**



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