# IS 61C88

## 16K X 4 HIGH SPEED CMOS STATIC RAM

**AUGUST 1990**

**ISSI**

## FEATURES

- Very High Speed - 15, 20, 25, 30 ns (Max.)
- **Fast output enable (tDOE) for cache applications**
- Automatic power-down when chip is deselected
- CMOS Low Power Operation
  - 400mW (Typical) Operating
  - 55mW (Typical) TTL standby
  - 25µW (Typical) CMOS standby (L-version)
- TTL compatible interface levels
- Single 5V power supply
- Fully static operation-no clock refresh required
- Three state outputs
- Chip enable $\overline{CE}$ for simple memory expansion
- Data retention as low as 2V for battery back-up (L-version)

## DESCRIPTION

The ISSI IS61C88 is a very high speed, low power, 16384 words by 4 bit static RAM. The device is fabricated using ISSI's high performance CMOS double metal technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 15ns with low power consumption.

When $\overline{CE}$ is high the device assumes a standby with low power consumption mode at which the power dissipation can be reduced down to 25µW (typical) with CMOS input levels.
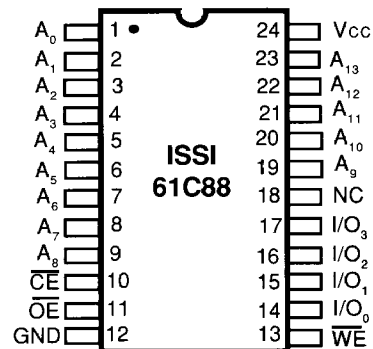
Easy memory expansion is provided by using an active low Chip Enable, $\overline{CE}$ and three-state drivers. The IS61C88 has an active low Output Enable ($\overline{OE}$) feature.

The IS61C88 is packaged in the JEDEC standard 24 pin, 300 mil DIP and SOJ surface mount packages.

## FUNCTIONAL BLOCK DIAGRAM
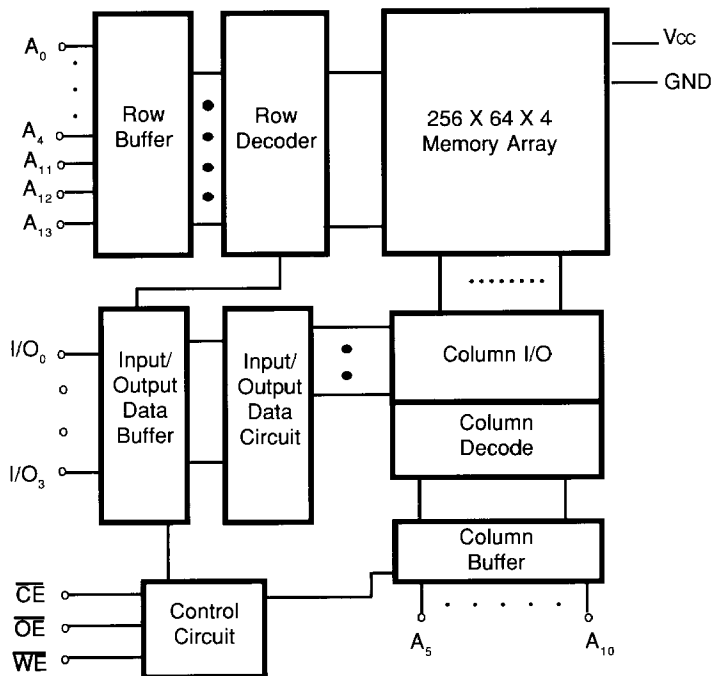


## PIN CONFIGURATION



**DIP/SOJ**

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# IS 61C88

## ABSOLUTE MAXIMUM RATINGS [1]

| Symbol | Parameter | Value | Unit |
|--------|-----------|-------|------|
| $V_{TERM}$ | Terminal Voltage with Respect to GND | -0.5 to +7.0 | V |
| $T_{BIAS}$ | Temperature Under Bias | -55 to +125 | °C |
| $T_{STG}$ | Storage Temperature | -65 to +150 | °C |
| $P_T$ | Power Dissipation | 1.0 | W |
| $I_{OUT}$ | DC output Current (low) | 20 | mA |

## OPERATING RANGE

| Range | Ambient Temperature | Vcc |
|-------|---------------------|-----|
| Commercial | 0°C to 70°C | 5V ±10% |
| Industrial | -40°C to 85°C | 5V ±10% |

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Electrical Characteristics over Operating Range

| Symbol | Description | Test Conditions | -15 -L15 MIN. | -15 -L15 MAX. | -20 -L20 MIN. | -20 -L20 MAX. | -25 -L25 MIN. | -25 -L25 MAX. | -30 -L30 MIN. | -30 -L30 MAX. | Units |
|--------|-------------|-----------------|------|------|------|------|------|------|------|------|-------|
| $V_{OH}$ | Output High Voltage | Vcc = Min., IOH = -4.0mA | 2.4 | | 2.4 | | 2.4 | | 2.4 | | V |
| $V_{OL}$ | Output Low Voltage | Vcc = Min., IOL = 8.0 mA | | 0.4 | | 0.4 | | 0.4 | | 0.4 | V |
| $V_{IH}$ | Input High Voltage | | 2.2 | Vcc | 2.2 | Vcc | 2.2 | Vcc | 2.2 | Vcc | V |
| $V_{IL}$ | Input Low Voltage (2) | | -0.5 | 0.8 | -0.5 | 0.8 | 0.5 | 0.8 | -0.5 | 0.8 | V |
| $I_{LI}$ | Input Leakage | GND ≤ VIN ≤ Vcc | -10 | 10 | -10 | 10 | -10 | 10 | -10 | 10 | µA |
| $I_{LO}$ | Output Leakage | GND ≤ VOUT ≤ Vcc, Output Disabled | -10 | 10 | -10 | 10 | -10 | 10 | -10 | 10 | µA |
| $I_{OS}$ | Output Short Circuit Current (1) | Vcc = Max., VOUT = GND | | -150 | | -150 | | -150 | | -150 | mA |
| $I_{CC_1}$ | Vcc Operating Supply Current | Vcc = Max., IOUT = 0mA, f = 0 (3) | | 160 | | 140 | | 120 | | 120 | mA |
| $I_{CC_2}$ | Vcc Dynamic Operating Supply Current | Vcc = Max., IOUT = 0 mA, f = fMAX. (3) | | 190 | | 170 | | 145 | | 145 | mA |
| $I_{SB_1}$ | TTL Standby Current (TTL Inputs) | Vcc = Max., VIN = VIH OR VIL CE ≥ VIH, f = 0 (3) | | 40 | | 30 | | 25 | | 20 | mA |
| $I_{SB_2}$ | CMOS Standby | Vcc = Max., CE ≥ Vcc -0.2V VIN ≥ Vcc -0.2V, OR VIN ≤ 0.2V, f = 0 (3) | | 6 | | 5 | | 4 | | 3 | mA |
| | | | L | 100 | L | 100 | L | 100 | L | 100 | µA |

Notes:
1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. $V_{IL}$ = -3.0V for pulse width less than 10ns.
3. At f = fmax address and data input are cycling at the maximum frequency, f = 0 means no input lines change.

## Capacitance (1,2)

| Symbol | Parameter | Conditions | Max. | Unit |
|--------|-----------|------------|------|------|
| $C_{IN}$ | Input Capacitance | VIN = 0V | 5 | pF |
| $C_{OUT}$ | Output Capacitance | VOUT = 0V | 7 | pF |

1. This parameter is guaranteed and not tested.
2. Test condition: TA = 25°C, f = 1MHz, Vcc = 5.0V

## TRUTH TABLE

| MODE | $\overline{WE}$ | $\overline{CE}$ | $\overline{OE}$ | I/O OPERATION | $V_{cc}$ CURRENT |
|------|------|------|------|------|------|
| Not Selected (Power Down) | X | H | X | High Z | $I_{SB_1}$, $I_{SB_2}$ |
| Output Disabled | H | L | H | High Z | $I_{cc_1}$, $I_{cc_2}$ |
| Read | H | L | L | $D_{OUT}$ | $I_{cc_1}$, $I_{cc_2}$ |
| Write | L | L | X | $D_{IN}$ | $I_{cc_1}$, $I_{cc_2}$ |

## Switching Characteristics Over Operating Range (1)

| Symbol | Description | IS61C88-15 IS61C88-L15 MIN. | MAX. | IS61C88-20 IS61C88-L20 MIN. | MAX. | IS61C88-25 IS61C88-L25 MIN. | MAX. | IS61C88-30 IS61C88-L30 MIN. | MAX. | Units |
|------|------|------|------|------|------|------|------|------|------|------|
| **READ CYCLE** | | | | | | | | | | |
| tRC | Read Cycle Time | 15 | | 20 | | 25 | | 30 | | ns |
| tAA | Address Access Time | | 15 | | 20 | | 25 | | 30 | ns |
| tOHA | Output Hold Time | 3 | | 3 | | 3 | | 3 | | ns |
| tACE | $\overline{CE}$ Access Time | | 15 | | 20 | | 25 | | 30 | ns |
| tDOE | $\overline{OE}$ Access Time | | 7 | | 7 | | 9 | | 12 | ns |
| tLZOE | $\overline{OE}$ to Low Z Output | 0 | | 0 | | 0 | | 0 | | ns |
| tHZOE(2) | $\overline{OE}$ to High Z Output | | 8 | | 10 | | 12 | | 15 | ns |
| tLZCE | $\overline{CE}$ to Low Z Output | 3 | | 3 | | 3 | | 3 | | ns |
| tHZCE(2) | $\overline{CE}$ to High Z Output | | 8 | | 10 | | 12 | | 15 | ns |
| tPU | $\overline{CE}$ to Power Up | 0 | | 0 | | 0 | | 0 | | ns |
| tPD | $\overline{CE}$ to Power Down | | 15 | | 20 | | 20 | | 20 | ns |
| **WRITE CYCLE (3)** | | | | | | | | | | |
| tWC | Write Cycle Time | 15 | | 20 | | 25 | | 30 | | ns |
| tSCE | $\overline{CE}$ to Write End | 12 | | 17 | | 22 | | 25 | | ns |
| tAW | Address Set-up Time to Write End | 12 | | 15 | | 20 | | 25 | | ns |
| tHA | Address Hold from Write End | 0 | | 0 | | 0 | | 0 | | ns |
| tSA | Address Set-up Time | 0 | | 0 | | 0 | | 0 | | ns |
| tPWE (4) | $\overline{WE}$ Pulse Width | 10 | | 12 | | 15 | | 18 | | ns |
| tSD | Data Set-up to Write End | 9 | | 10 | | 12 | | 15 | | ns |
| tHD | Data hold from Write End | 0 | | 0 | | 0 | | 0 | | ns |
| tHZWE (2) | $\overline{WE}$ LOW to High-Z Output | | 6 | | 7 | | 8 | | 10 | ns |
| tLZWE | $\overline{WE}$ HIGH to Low-Z Output | 0 | | 0 | | 0 | | 0 | | ns |

Notes:
1. Test conditions assume signal transition times of 5ns or less, timing reference levels of 1.5V, Input pulse levels of 0 to 3.0V and output loading specified in figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ± 500mV from steady state voltage.
3. The internal write time is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. All signals must be in valid states to initiate a Write, but anyone can go inactive to terminate the Write. The Data input Setup and Hold timing are referenced to the rising edge of the signal that terminates the write.
4. Tested with $\overline{OE}$ high.
5. WE is high for a Read Cycle.
6. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = VIL.
7. Address is valid prior to or coincident with $\overline{CE}$ Low transitions.
8. I/O will assume the High-Z state if $\overline{OE}$=VIH.

# IS 61C88

## AC TEST CONDITIONS

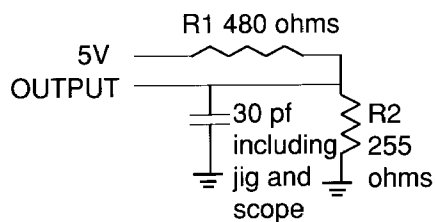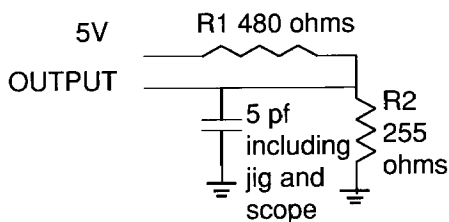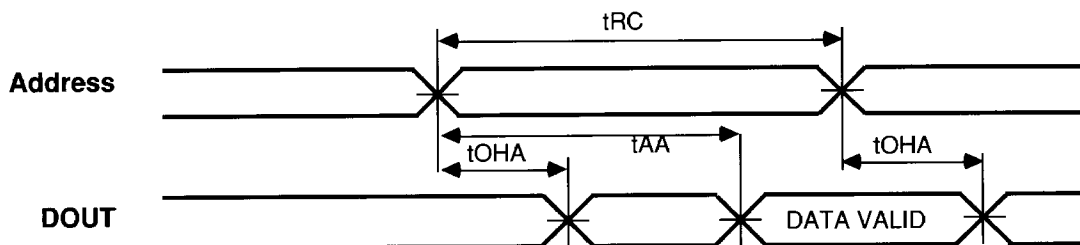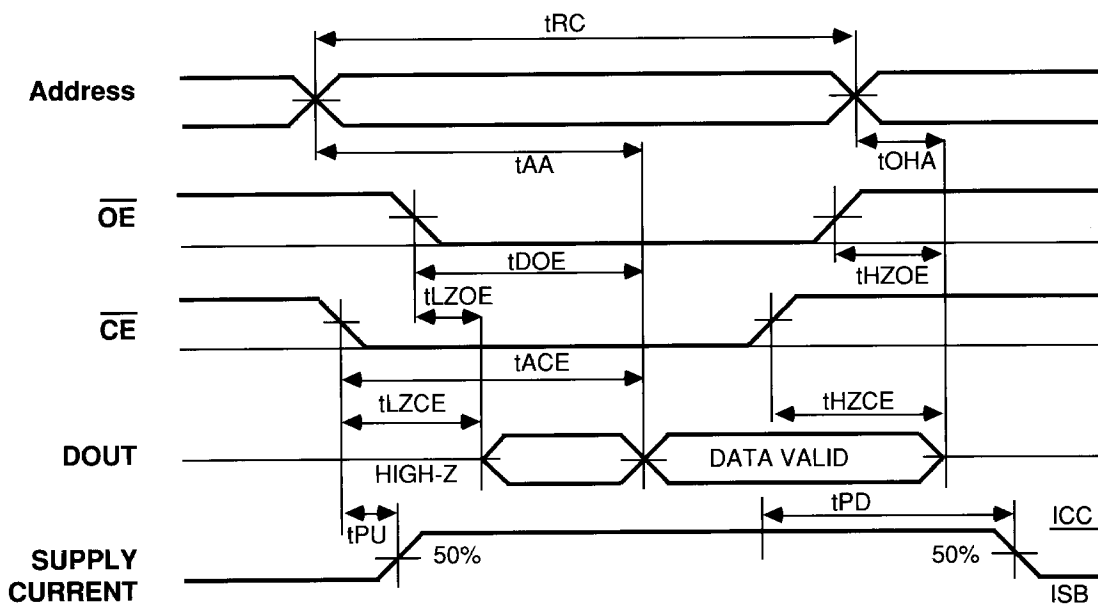| Input Pulse Level | 0V to 3.0V |
| Input Rise and Fall Times | 5ns |
| Input and Output Timing and Reference Level | 1.5V |

## AC TEST LOADS
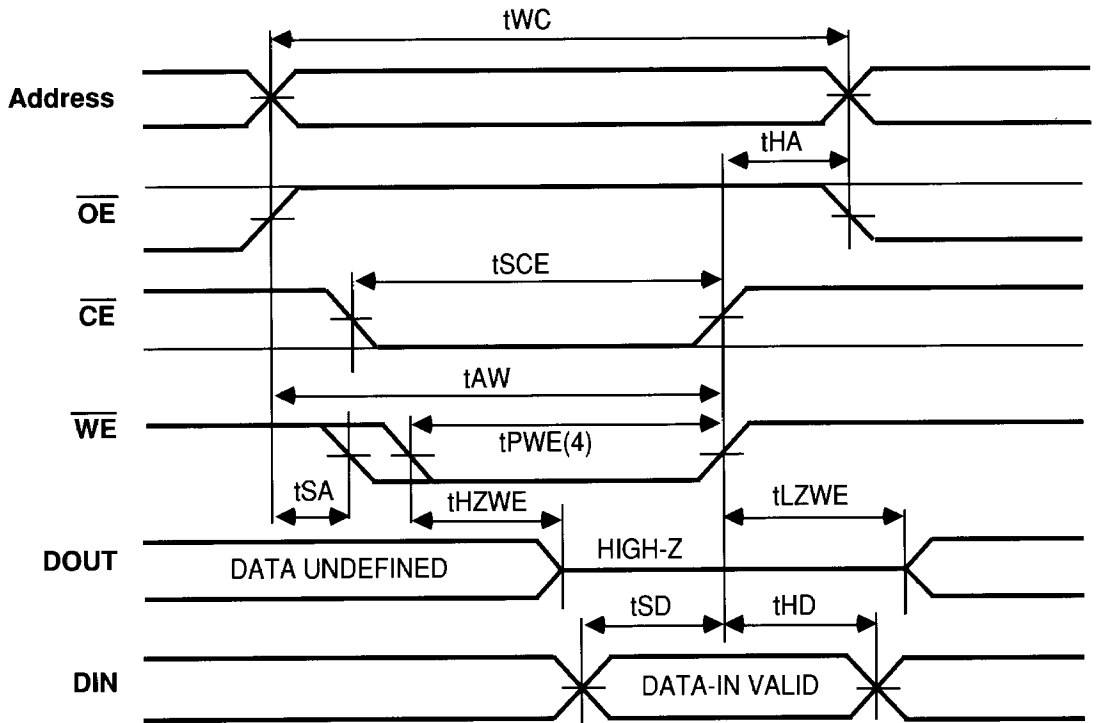


Figure 1a

Figure 1b

## AC WAVEFORMS

### READ CYCLE NO. 1 (Note 5,6)



### READ CYCLE NO. 2 (Note 5,7)

**WRITE CYCLE NO. 1** ($\overline{\text{WE}}$ controlled) (Note 3,8)



**WRITE CYCLE NO. 2** ($\overline{\text{CE}}$ controlled) (Note 3,8)
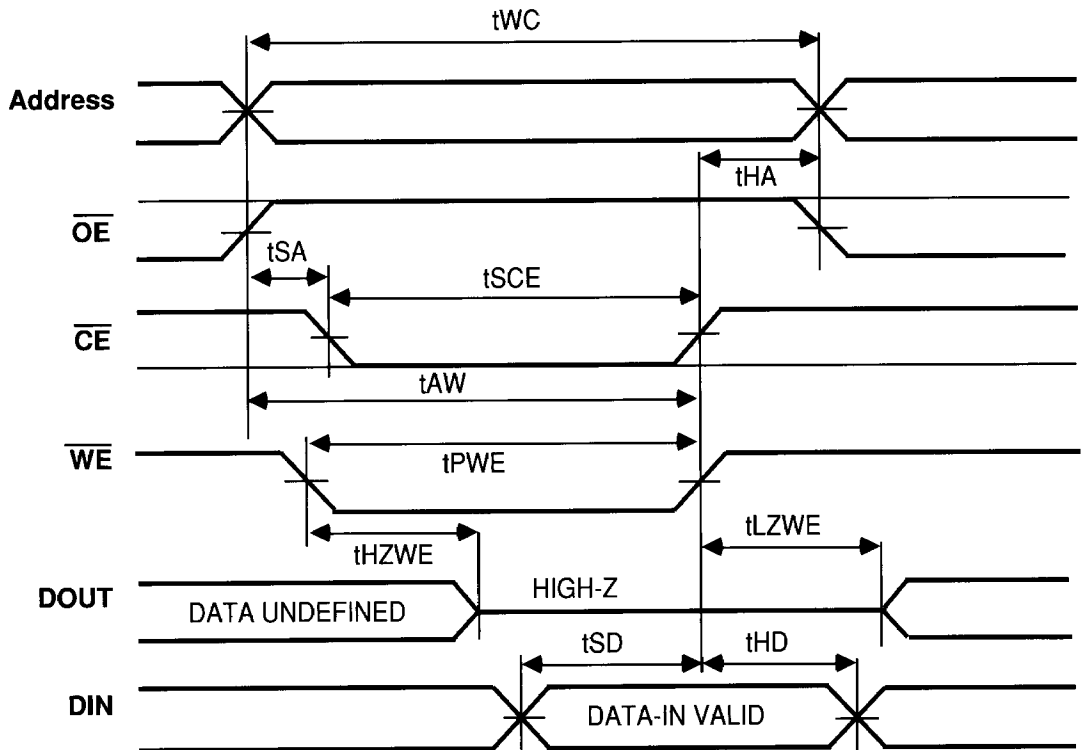
## DATA RETENTION CHARACTERISTICS (L Version only)

| Parameter | Description | Test Conditions | Min. | Max. | Units |
|-----------|-------------|-----------------|------|------|-------|
| VDR | VCC for retention of data | VCC = 2.0V | 2.0 | ----- | V |
| ICCDR | Data retention current | $\overline{CE}$ ≥ VCC - 0.2V, | ----- | 100 | μA |
| tCDR | Chip deselect to data retention time | CMOS Inputs | 0 | ----- | ns |
| tR | Operation recovery time | | tRC | ----- | ns |
| IL I | Input leakage current | | ----- | 2 | μA |

## DATA RETENTION WAVEFORM
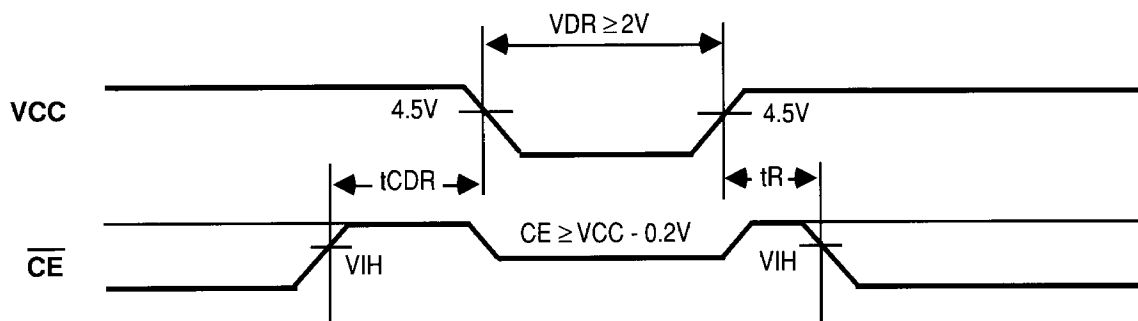


## PIN DESCRIPTIONS

### $A_0$ - $A_{13}$ Address Inputs
These 14 address inputs select one of the 16384 4-bit words in the RAM.

### $\overline{CE}$ Chip Enable Input
$\overline{CE}$ is active Low. The chip enable must be active to read from or write to the device. If the chip enable is not active, the device is deselected and is in a standby power mode. The I/O pins will be in the high-impedance state when the device is deselected.

### $\overline{OE}$ Output Enable Input
The ouput enable input is active Low. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the I/O pins. The I/O pins will be in the high-impedance state when $\overline{OE}$ is inactive.

### $\overline{WE}$ Write Enable Input
The write enable input is active Low and controls read and write operations. With the chip selected, when $\overline{WE}$ is Low, Input data present on the I/O pins will be written into the selected memory location.
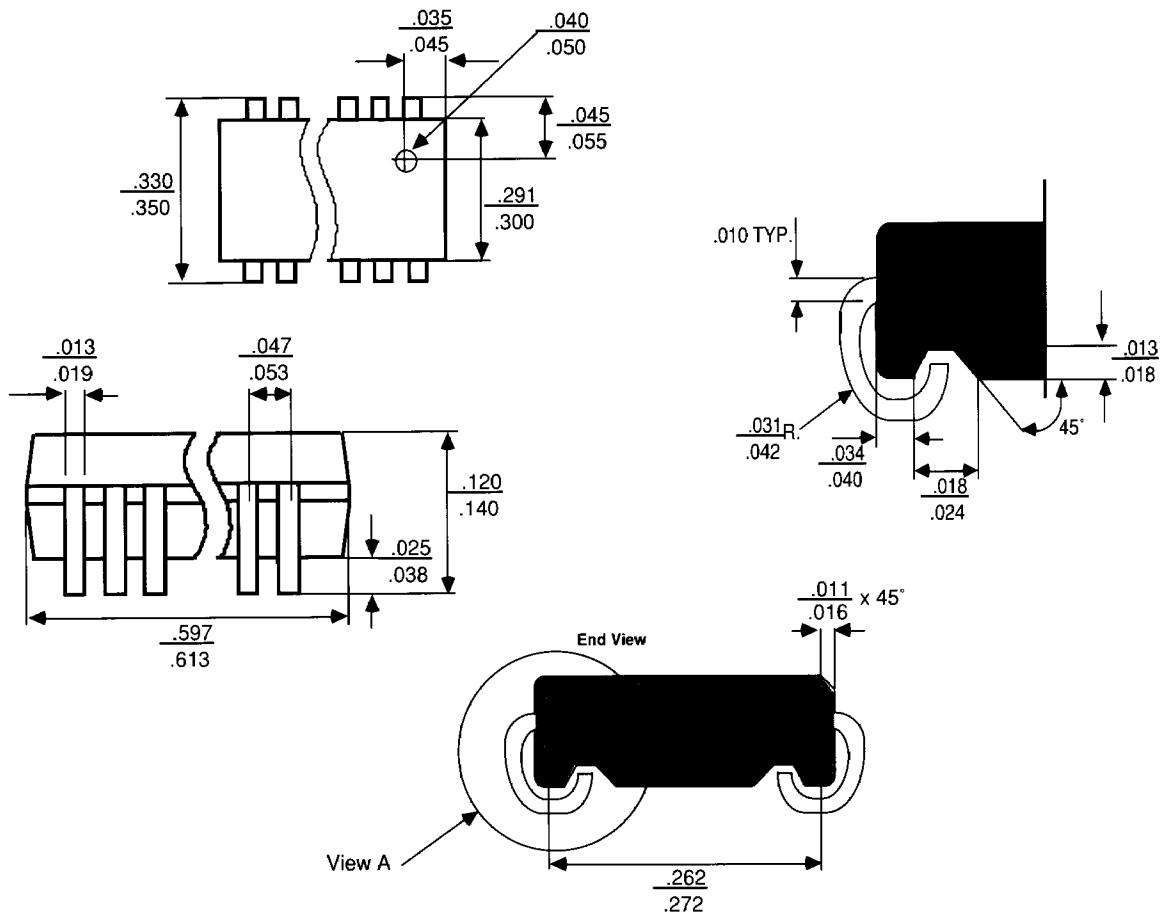
### $I/O_0$ - $I/O_3$
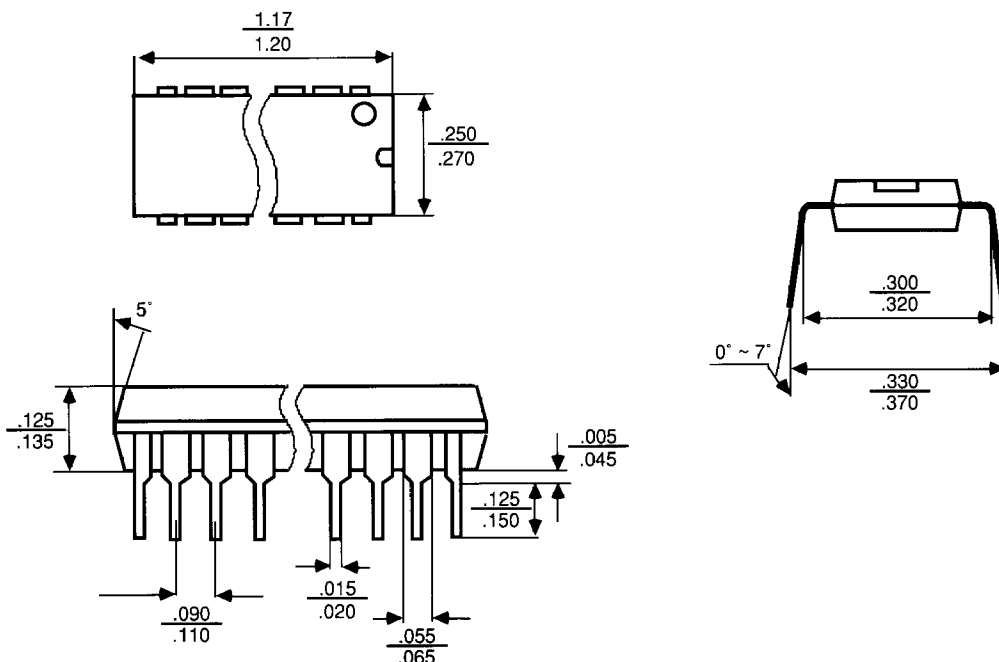These 4 bidirectional ports are used to read data from or write data into the RAM.

### Vcc - Power

### GND - Ground

# 24 PIN SOJ PACKAGE

## 24 Pin 300 MIL PLASTIC DIP Package

| SPEED (ns) | ORDER<br>PART NUMBER | PACKAGE | TEMPERATURE<br>RANGE |
|---|---|---|---|
| 15 | IS61C88-15N | Plastic DIP - 300 mil | 0°C to +70°C |
| 15 | IS61C88-15J | Plastic Small Outline J | 0°C to +70°C |
| 15 LOW | IS61C88-L15N | Plastic DIP - 300 mil | 0°C to +70°C |
| 15 POWER | IS61C88-L15J | Plastic Small Outline J | 0°C to +70°C |
| 20 | IS61C88-20N | Plastic DIP - 300 mil | 0°C to +70°C |
| 20 | IS61C88-20J | Plastic Small Outline J | 0°C to +70°C |
| 20 LOW | IS61C88-L20N | Plastic DIP - 300 mil | 0°C to +70°C |
| 20 POWER | IS61C88-L20J | Plastic Small Outline J | 0°C to +70°C |
| 25 | IS61C88-25N | Plastic DIP - 300 mil | 0°C to +70°C |
| 25 | IS61C88-25J | Plastic Small Outline J | 0°C to +70°C |
| 25 LOW | IS61C88-L25N | Plastic DIP - 300 mil | 0°C to +70°C |
| 25 POWER | IS61C88-L25J | Plastic Small Outline J | 0°C to +70°C |
| 30 | IS61C88-30N | Plastic DIP - 300 mil | 0°C to +70°C |
| 30 | IS61C88-30J | Plastic Small Outline J | 0°C to +70°C |
| 30 LOW | IS61C88-L30N | Plastic DIP - 300 mil | 0°C to +70°C |
| 30 POWER | IS61C88-L30J | Plastic Small Outline J | 0°C to +70°C |