Saratoga Semiconductor

SSM2148/9

4K 1,024 Words by 4 Bits BiCMOS TTL Static RAM

FEATURES

- **Fast Access Times**
  15/20/25ns Commercial Temperature
  20/25/35ns Military Temperature
- **Common Data Inputs & Outputs**
- **Full Military Temperature Range**
- **Automatic Power Down when Deselected** (SSM2148)
- **Industry Standard 18-Pin DIP**
- **SABiC BiCMOS Fabrication Technology**

DESCRIPTION

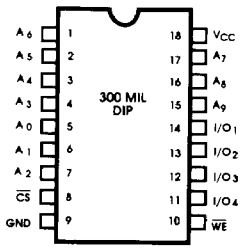
The SSM2148 and SSM2149 are high performance 4K Bi-CMOS static RAMs organized 1024 words by 4 bits. These devices are targeted for use in main, cache and buffer memories, as well as writeable control store in mid-range computers. They are also designed for use in communication, industrial and military equipment applications.

The high speed (2148 at 20ns and 2149 at 15ns), low active power consumption (2148 at 50mA and 2149 at 90mA) and high output drive (16mA) of the SSM2148 and SSM2149 when compared to equivalent CMOS TTL circuits is achieved through utilization of Saratoga Semiconductor's exclusive "Self-Aligned Bipolar CMOS" (SABiC) wafer fabrication technology. SABiC integrates bipolar and CMOS in the same monolithic circuit thus providing an increase in both performance and reliability.

Writing to the device occurs when both the Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) inputs are low. Data on the Input/Output pins (I/O_1- I/O_4) is written into the memory cell specified by the 10 bit address placed on the Address inputs (A_0- A_9). With $\overline{CS}$ LOW, $\overline{WE}$ HIGH and the Output Enable input ($\overline{OE}$) LOW, the content of the addressed memory cell is transferred to the Input/Output pins.

All inputs and outputs of the device are TTL compatible and operate from a single 5V supply. Fully static circuitry is used and balanced read and write cycles are provided.

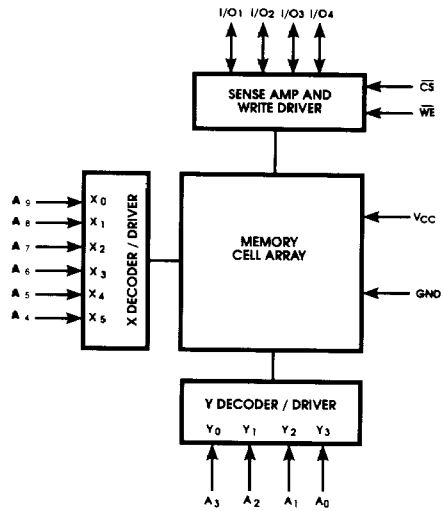
PIN CONFIGURATION



PIN IDENTIFICATION

A_0 - A_9	Address Inputs
I/O_1 - I/O_4	Data Inputs/Outputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
V_{CC}	Power Supply Pins
GND	Ground Pin

FUNCTIONAL BLOCK DIAGRAM



April 1989

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	I/On	POWER
Read	L	H	DO	ACTIVE
Write '0'	L	L	L	ACTIVE
Write '1'	L	L	H	ACTIVE
Disabled	H	X	HIGH Z	STANDBY (1)

H = High Voltage Level
L = Low Voltage Level
X = Irrelevant
DO = Valid Data Out
X = Irrelevant(1) For SSM2148 only.

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Storage Temperature	T_{STG}	-65	+150	°C
Temperature Under Bias	T_A	-65	+125	°C
Output Current (DC, Output High)	I_{OUT}		20	mA
Power Dissipation	P_D		250	mW
Power Supply Voltage	V_{CC}	-0.5	+7	V

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

SPECIFIED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Commercial Temperature Range	T_A	0	+70	°C
MilitaryTemperature Range	T_A	-55	+125	°C
Supply Voltage	V_{CC}	+4.5	+5.5	V
Input High Voltage	V_{IH}	2	V_{CC} +	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V

NOTE: Specified Operating Conditions define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS V_{CC} = 5V ±10% over specified temperature range

SYMBOL	PARAMETER	TEST CONDITIONS	SSM2148/9 MIN	SSM2148/9 MAX	UNIT
V_{OH}	Output High Voltage	I_{OH}=-4mA; V_{CC} = min	2.4		V
V_{OL}	Output Low Voltage	I_{OL}=16mA ; V_{CC}= min		0.4	V
I_{IX}	Input Leakage Current	V_{CC} = max GND ≤ V_{IN} ≤ V_{CC}	-10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{CS}$ = V_{IH} ; V_{CC}= max GND ≤ V_{OUT} ≤ V_{CC}	-50	+50	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC}= max; V_{OUT}= GND		-150	mA
I_{CC}	Operating Supply Current	$\overline{CS}$ = V_{IL} ; V_{CC} = max Output Open		50/90	mA

[1] Duration of short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.

AC CHARACTERISTICS

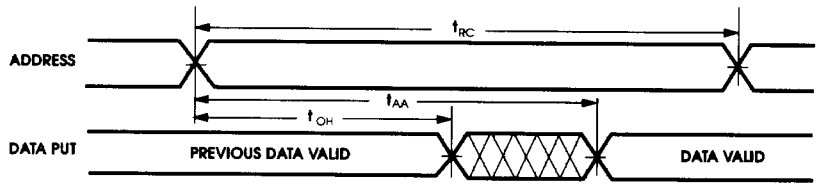
READ CYCLE

PARAMETER	SYMBOL	VALUE				UNIT
		COM SSM2148/9-15	COM/MIL SSM2148/9-20	COM/MIL SSM2148/9-25	MIL SSM2148/9-35	
		MIN MAX	MIN MAX	MIN MAX	MIN MAX	
Read Cycle Time	t_{RC}	15	20	25	35	ns
Address Access Time	t_{AA}	15	20	25	35	ns
Chip Select Access Time	t_{ACS}	10	15	20	25	ns
Output Hold from Address Change	t_{OH}	3	3	3	3	ns
Chip Selection to Output in LOW Z	t_{LZ}	3	3	3	3	ns
Chip Selection to Output in HIGH Z	t_{HZ}	12	15	20	25	ns
Chip Selection to Power Up Time	t_{PU}[2]	0	0	0	0	ns
Chip Deselection to Power Down Time	t_{PD}[2]	10	15	20	25	ns

[2] These parameters are sampled and not 100% tested.

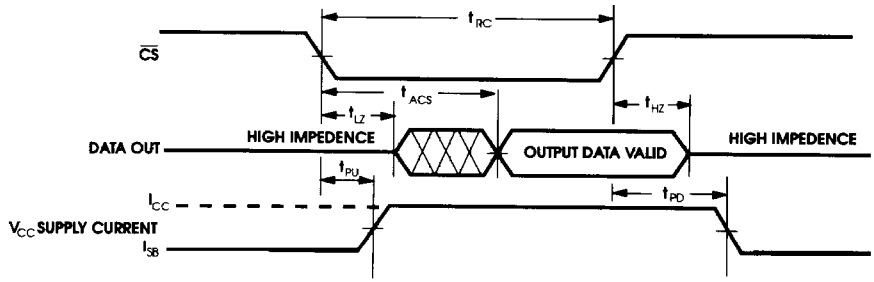
READ CYCLE TIMING DIAGRAM NO. 1

$\overline{WE}$ is high for Read Cycle. $\overline{CS}$ is low, device is continuously selected. All read Cycle timings are referenced from the last valid address to the first transitioning address.



READ CYCLE TIMING DIAGRAM NO. 2

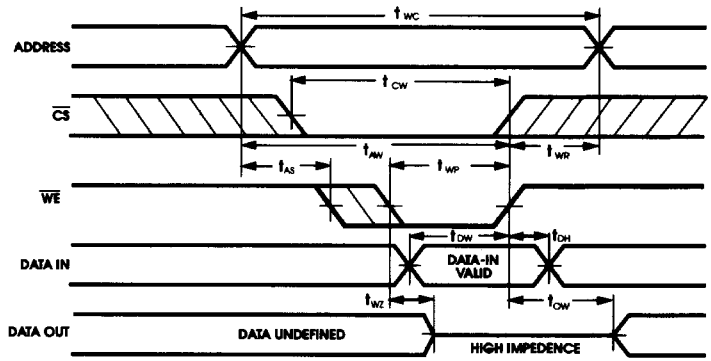
$\overline{WE}$ = V_{IH}, $\overline{OE}$ = V_{IL}. Transition is measured ±500mV from steady state. Address valid prior to $\overline{CS}$ transition low.



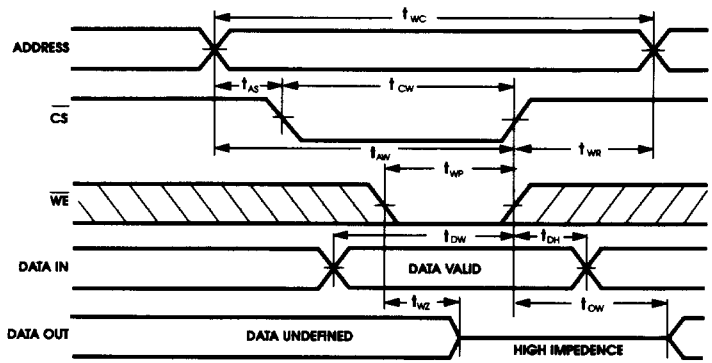
WRITE CYCLE

		VALUE				
		COM SSM2148/9-15	COM/MIL SSM2148/9-20	COM/MIL SSM2148/9-25	MIL SSM2148/9-35	
	SYMBOL	MIN MAX	MIN MAX	MIN MAX	MIN MAX	UNIT
Write Cycle Time	t_{WC}	15	20	25	35	ns
Chip Selection to End of Write	t_{CW}	15	20	25	35	ns
Address Valid to End of Write	t_{AW}	15	20	25	35	ns
Address Set-up Time	t_{AS}	0	0	0	0	ns
Write Pulse Width	t_{WP}	15	20	25	35	ns
Write Recovery Time	t_{WR}	0	0	0	0	ns
Data Valid to End of Write	t_{DW}	10	12	15	20	ns
Data Hold Time	t_{DH}	0	0	0	0	ns
Write Enable to Output in HIGH Z	t_{WZ}[2]	8	8	10	15	ns
Output Active from End of Write	t_{OW}[2]	0	0	0	0	ns

WRITE CYCLE TIMING DIAGRAM NO.1 (WE CONTROLLED)[3]



WRITE CYCLE TIMING DIAGRAM NO.2 (CS CONTROLLED)[3]



[3] If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedence state. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions. All write timings are referenced from the last valid address to the first transitioning address. Transition is measured ±500mV from steady state voltage.

CAPACITANCE

PARAMETER	SYMBOL	MAX VALUE	UNIT
Input Pin Capacitance	C_{IN}	5	pF
Output Pin Capacitance	C_{OUT}	7	pF

AC TEST CONDITIONS

[4] Including scope and jig

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Level	1.5V
Output Load	Figures 1 and 2

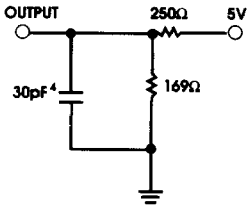


Figure 1

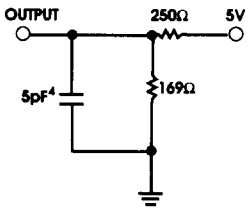
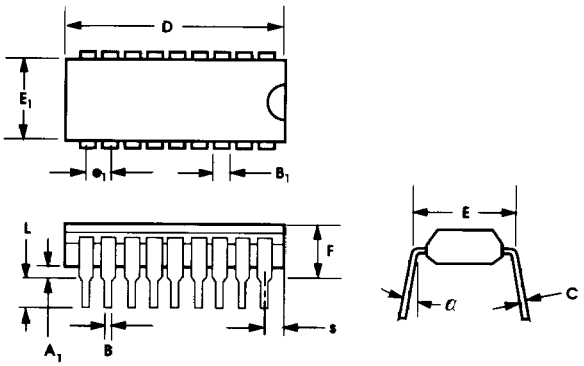


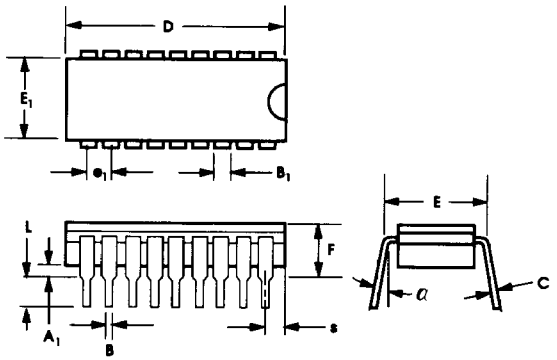
Figure 2

PACKAGE DIMENSIONS



18 LEAD 300 MIL PDIP

	INCHES	
PARAMETER	MIN	MAX
A_1	.015	
B	.016	.020
B_1	.045	.065
C	.008	.012
D	.890	.910
E	.280	.300
E_1	.255	.265
e_1	.100	
F		.170
L	.125	.135
s	.060	.070
α	0°	15°



18 LEAD 300 MIL CERDIP

	INCHES	
PARAMETER	MIN	MAX
A_1	.015	.045
B	.014	.023
B_1	.050	.065
C	.009	.015
D		.920
E	.300	.320
E_1	.285	.310
e_1	.100	
F		.200
L	.125	.200
s		.080
α	0°	15°

ORDERING INFORMATION

	PART NUMBER	SPEED	PACKAGE	TEMPERATURE RANGE MIN	MAX	UNIT
DISCONTINUED	SSM2148-20PC SSM2148-25PC	20ns 25	18-Pin PDIP	0	+70	°C
DISCONTINUED	SSM2148-20CC SSM2148-25CC	20ns 25	18-Pin CERDIP			
DISCONTINUED	SSM2148-25CM SSM2148-35CM	25ns 35	18-Pin CERDIP	-55	+125	°C
	SSM2149-15PC SSM2149-20PC SSM2149-25PC	15ns 20 25	18-Pin PDIP	0	+70	°C
	SSM2149-15CC SSM2149-20CC SSM2149-25CC	15ns 20 25	18-Pin CERDIP			
	SSM2149-20CM SSM2149-25CM SSM2149-35CM	20ns 25 35	18-Pin CERDIP	-55	+125	°C