

TRIPLE 3-INPUT POSITIVE AND GATE WITH OPEN COLLECTOR OUTPUT**DESCRIPTION**

The M74LS15P is a semiconductor integrated circuit containing 3 triple-input positive AND and negative OR gates with open collector outputs.

FEATURES

- Usable in wire-AND connection
- High breakdown input voltage ($V_I \geq 15V$)
- High breakdown output voltage ($V_O \geq 7V$)
- Low power dissipation ($P_D = 13mW$ typical)
- High speed ($t_{PD} = 13ns$ typical)
- Wide operating temperature range ($T_a = -20 \sim +75^\circ C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

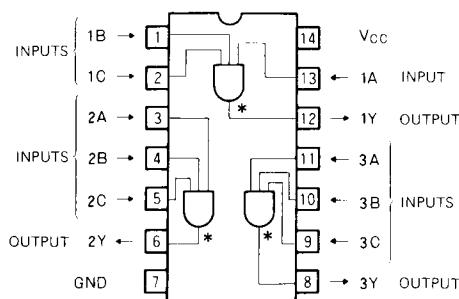
With the use of Schottky TTL Technology and open collector outputs with a high breakdown voltage, the high-level output impedance can be selected freely by use of an external load resistor. This permits wire-AND connection which has been impossible with conventional gates.

When inputs A, B and C are high, output Y is high and when one or more of the inputs is low, Y is low.

FUNCTION TABLE

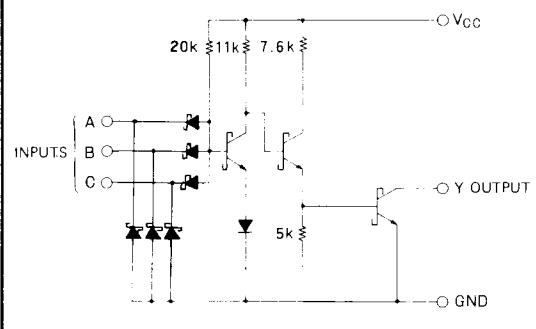
A	N	Y
L	L	L
H	L	L
L	H	L
H	H	H

$N = B \cdot C$

PIN CONFIGURATION (TOP VIEW)

* : OPEN COLLECTOR OUTPUT

Outline 14P4

CIRCUIT SCHEMATIC (EACH GATE)

UNIT : Ω

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^\circ C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		-0.5 ~ + 7	V
V_I	Input voltage		-0.5 ~ + 15	V
V_O	Output voltage	High-level state	-0.5 ~ + 7	V
T_{OPR}	Operating free-air ambient temperature range		-20 ~ + 75	°C
T_{STG}	Storage temperature range		65 ~ + 150	°C

TRIPLE 3-INPUT POSITIVE AND GATE WITH OPEN COLLECTOR OUTPUT

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V _{CC}	Supply voltage	4.75	5	5.25	V
I _{OH}	High-level output current	0		100	μA
I _{OL}	Low-level output current	V _{OL} \leq 0.4V	0	4	mA
		V _{OL} \leq 0.5V	0	8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

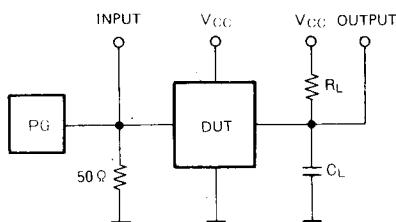
Symbol	Parameter	Conditions	Limits			Unit	
			Min	Typ *	Max		
V _{IH}	High-level input voltage		2			V	
V _{IL}	Low-level input voltage				0.8	V	
V _{IC}	Input clamp voltage	V _{CC} = 4.75V, I _{IC} = -18mA			-1.5	V	
I _{OH}	High-level output current	V _{CC} = 4.75V, V _I = 2V, V _O = 5.5V			100	μA	
V _{OL}	Low-level output voltage	V _{CC} = 4.75V V _I = 0.8V	I _{OL} = 4mA I _{OL} = 8mA	0.25 0.35	0.4 0.5	V	
I _{IH}	High-level input current	V _{CC} = 5.25V, V _I = 2.7V V _{CC} = 5.25V, V _I = 10V			20 0.1	μA mA	
I _{IL}	Low-level input current	V _{CC} = 5.25V, V _I = 0.4V			-0.4	mA	
I _{ICCH}	Supply current, all outputs high	V _{CC} = 5.25V, V _I = 4.5V			1.8	3.6	mA
I _{ICCL}	Supply current, all outputs low	V _{CC} = 5.25V, V _I = 0			3.3	6.6	mA

* : All typical values are at $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$.

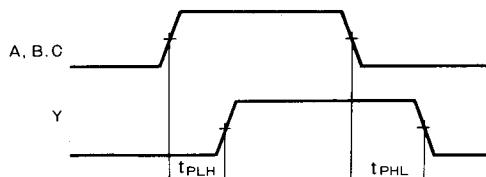
SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t _{PLH}	Low-to-high-level output propagation time	R _L = 2k Ω		15	35	ns
t _{PHL}	High-to-low-level output propagation time	C _L = 15pF (Note)		10	35	ns

Note: Measurement circuit



TIMING DIAGRAM (Reference level = 1.3V)



(1) The pulse generator (PG) has the following characteristics:

PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,

V_p = 3V_{p-p}, Z₀ = 50 Ω .

(2) C_L includes probe and jig capacitance.

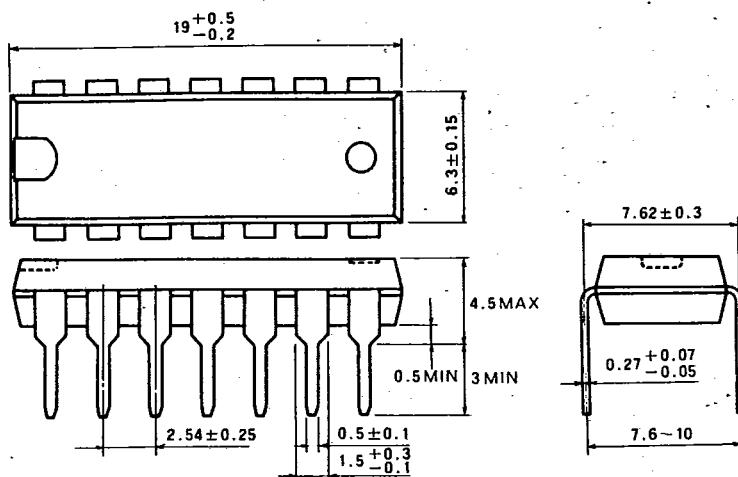
MITSUBISHI LSTTLs
PACKAGE OUTLINES

MITSUBISHI {DGTL LOGIC} 07E D | 6249827 0013561 3

T-90-20

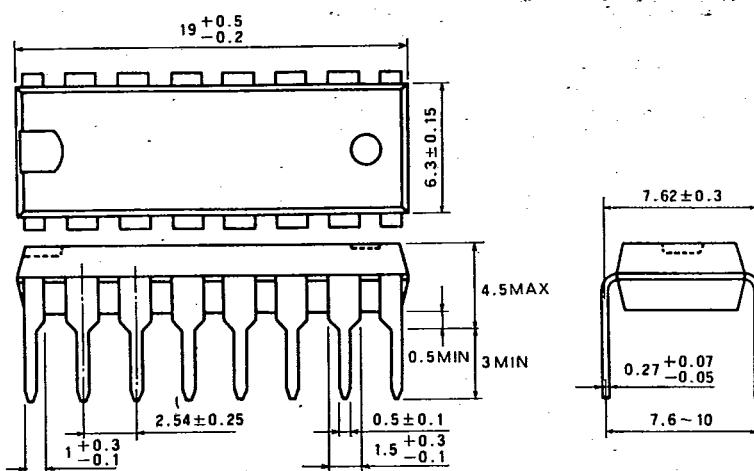
TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimension in mm

