

# SN54LS171, SN74LS171 QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

DECEMBER 1983 — REVISED MARCH 1988

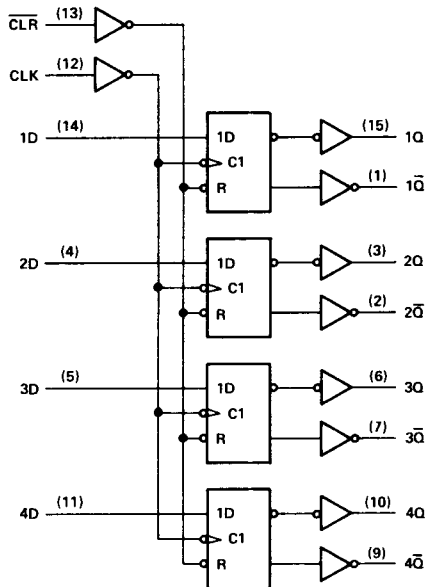
- Contains Four Flip-Flops with Double Rail Outputs
- Buffered Clock and Clear Inputs
- Individual Data Inputs to Each Flip-Flop

## description

These monolithic, positive-edge triggered flip-flops utilize the latest low-power Schottky circuitry to implement D-type flip-flop logic. They have a direct clear input and complementary outputs from each flip-flop.

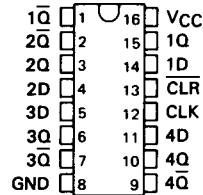
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

## logic diagram (positive logic)

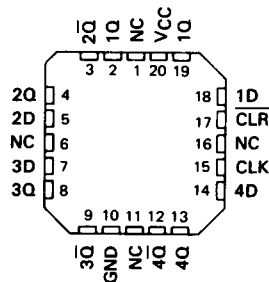


Pin numbers shown are for D, J, N, and W packages.

SN54LS171 . . . J OR W PACKAGE  
SN74LS171 . . . D OR N PACKAGE  
(TOP VIEW)



SN54LS171 . . . FK PACKAGE  
(TOP VIEW)

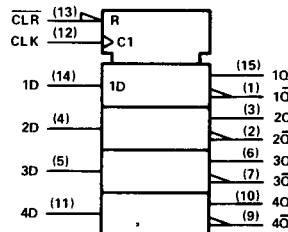


NC—No internal connection

FUNCTION TABLE  
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLR	CLK	D	Q	$\bar{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	$Q_0$	$\bar{Q}_0$

## logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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# SN54LS171, SN74LS171 QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS171			SN74LS171			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
$V_{OH}$ High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, I_{OH} = -1 \text{ mA}$	2.5	3.4		2.7	3.4		V
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V
						0.35	0.5	V
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	$\mu\text{A}$
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$	D inputs		-0.4			-0.4	mA
		All others		-0.2			-0.2	mA
$I_{OS}§$ Short-circuit output current	$V_{CC} = \text{MAX}, V_O = 0 \text{ V}$	-20		-100	-20		-100	mA
$I_{CC}$ Supply current	$V_{CC} = \text{MAX}, \text{ See Note 1}$		14	25		14	25	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

NOTE 1:  $I_{CC}$  is measured with all inputs grounded and all outputs open.

switching characteristics,  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$  (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS171			UNIT
				MIN	TYP	MAX	
$f_{max}$			$R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF}$	20	30		MHz
$t_{PLH}$	CLK	Q, $\bar{Q}$		15	25		ns
$t_{PHL}$				18	30		ns
$t_{PLH}$	$\bar{CLR}$	Q		18	30		ns
$t_{PHL}$				24	40		ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

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