



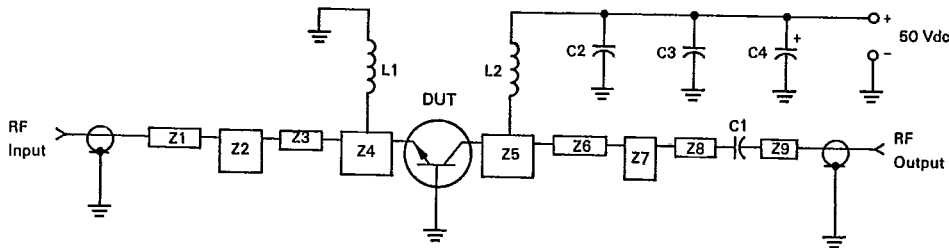
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ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector-Emitter Breakdown Voltage (I <sub>C</sub> = 25 mA, V <sub>BE</sub> = 0)	V <sub>(BR)CES</sub>	70	—	—	V <sub>dc</sub>
Collector-Base Breakdown Voltage (I <sub>C</sub> = 25 mA, I <sub>E</sub> = 0)	V <sub>(BR)CBO</sub>	70	—	—	V <sub>dc</sub>
Emitter-Base Breakdown Voltage (I <sub>E</sub> = 5.0 mA, I <sub>C</sub> = 0)	V <sub>(BR)EBO</sub>	4.0	—	—	V <sub>dc</sub>
Collector Cutoff Current (V <sub>CB</sub> = 50 V <sub>dc</sub> , I <sub>E</sub> = 0)	I <sub>CBO</sub>	—	—	5.0	mA <sub>dc</sub>
<b>ON CHARACTERISTICS</b>					
DC Current Gain* (I <sub>C</sub> = 2.5 A <sub>dc</sub> , V <sub>CE</sub> = 5.0 V <sub>dc</sub> )	h <sub>FE</sub>	10	30	—	—
<b>DYNAMIC CHARACTERISTICS</b>					
Output Capacitance (V <sub>CB</sub> = 50 V <sub>dc</sub> , I <sub>E</sub> = 0, f = 1.0 MHz)	C <sub>ob</sub>	—	12	16	pF
<b>FUNCTIONAL TESTS (Pulse Width = 10 μs, Duty Cycle = 1.0%)</b>					
Common-Base Amplifier Power Gain (V <sub>CC</sub> = 50 V <sub>dc</sub> , P <sub>out</sub> = 90 W pk, f = 1090 MHz)	G <sub>PB</sub>	8.4	10.8	—	dB
Collector Efficiency (V <sub>CC</sub> = 50 V <sub>dc</sub> , P <sub>out</sub> = 90 W pk, f = 1090 MHz)	η	35	40	—	%
Load Mismatch (V <sub>CC</sub> = 50 V <sub>dc</sub> , P <sub>out</sub> = 90 W pk, f = 1090 MHz) VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Power Output			

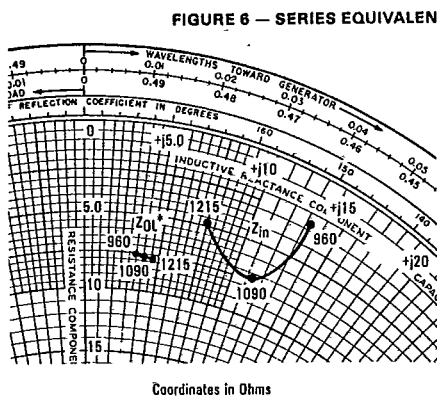
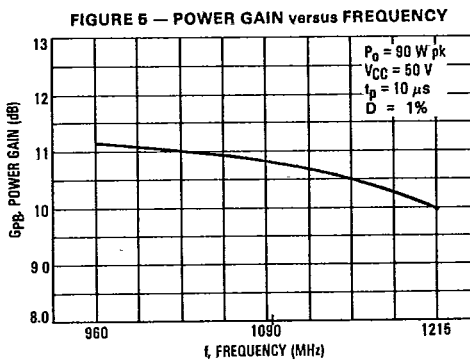
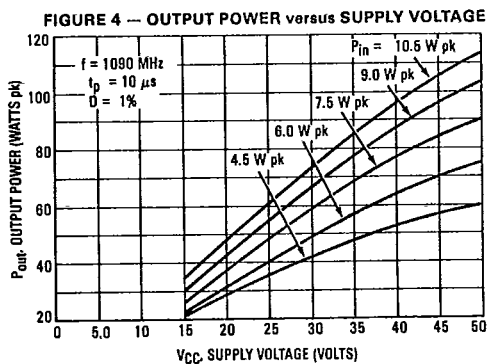
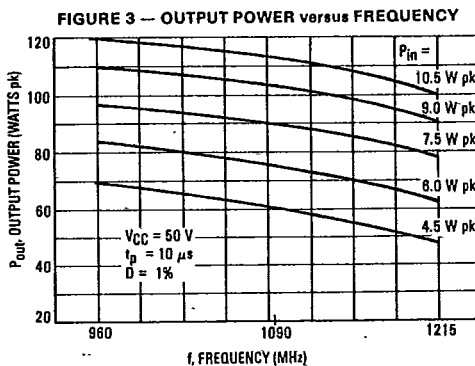
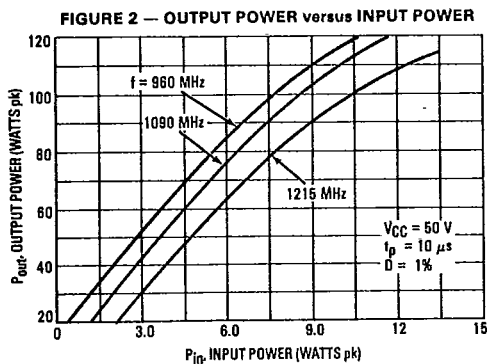
\* 80 μs Pulse on Tektronix 576 or equivalent.

FIGURE 1 — 1090 MHz TEST CIRCUIT



- C1, C2 — 220 pF Chip Capacitor, 100-mil ATC
- C3 — 0.1 μF
- C4 — 47 μF, 75 V
- L1, L2 — 3 Turns, #18 AWG, 1/8" ID
- Z1-Z9 — Distributed Microstrip Elements — See Figure 9
- Board Material — 0.031" Thick Glass Teflon,  
ε<sub>r</sub> = 2.5

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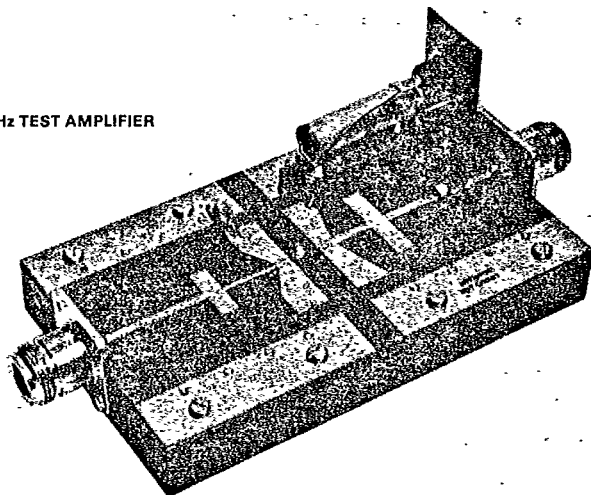
$P_{out} = 90$  W pk  $V_{CC} = 50$  V  
 $t_p = 10 \mu s$   $D = 1\%$

$f$ MHz	$Z_{in}$ Ohms	$Z_{OL}^*$ Ohms
960	$2.8 + j13.2$	$7.6 + j3.5$
1090	$7.4 + j11.4$	$7.8 + j4.0$
1215	$4.7 + j7.5$	$7.7 + j4.5$

\* $Z_{OL}$  = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

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FIGURE 7 — 1090 MHz TEST AMPLIFIER



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FIGURE 8 — TYPICAL PULSE PERFORMANCE

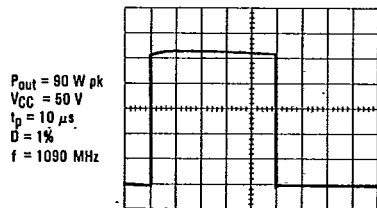
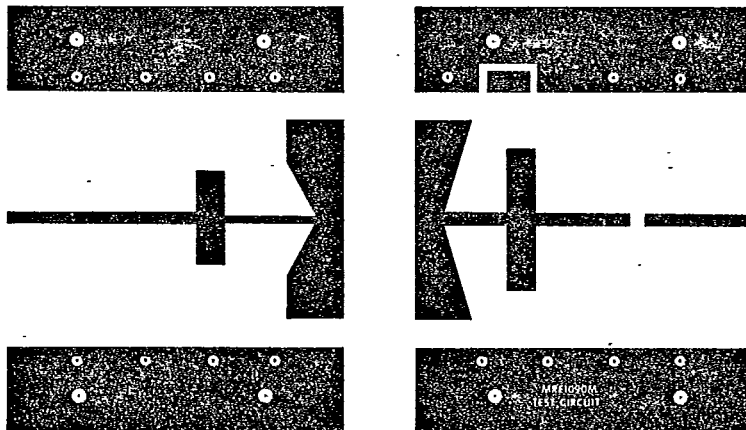


FIGURE 9 — PRINTED CIRCUIT BOARD LAYOUT — 1090 MHz TEST CIRCUIT



- ⊙ Soldered Eyelet
- ⊙ 4-40 Screw Placement

NOTE: The Printed Circuit Board shown is 75% of the original.