REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22											
REV STATUS OF SHEETS	REV																		
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14				

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
96-02-20

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, X 9 CLOCKED FIFO'S, MONOLITHIC SILICON

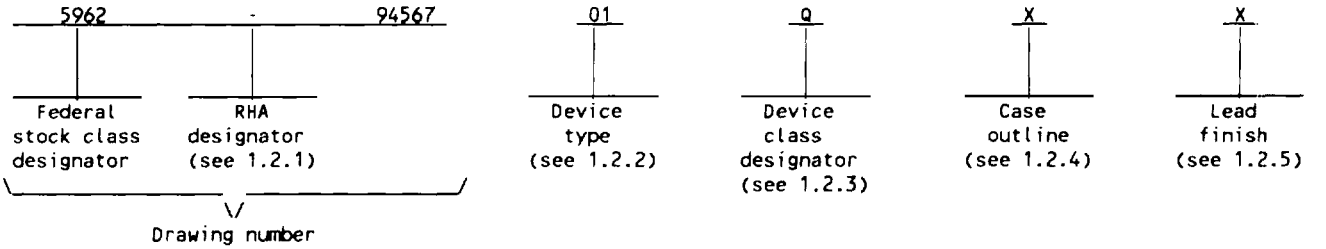
SIZE	CAGE CODE	
A	67268	**5962-94567**

SHEET 1 OF 22

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time
01	7C443	2K x 9 Clocked FIFO	30 ns
02	7C443	2K x 9 Clocked FIFO	20 ns
03	7C443	2K x 9 Clocked FIFO	14 ns
04	7C441	512 x 9 Clocked FIFO	30 ns
05	7C441	512 x 9 Clocked FIFO	20 ns
06	7C441	512 x 9 Clocked FIFO	14 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP4-T28	32	Dual-in-line Package
Y	CQCC1-N32	32	Rectangular leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103 (see 6.7.3 herein).

1.3 Absolute maximum ratings. 2/

Supply voltage range to ground potential (V_{CC})	-0.5 V dc to +7.0 V dc
DC voltage applied to the outputs in the high Z state	-0.5 V dc to +7.0 V dc
DC input voltage	-3.0 V dc to +7.0 V dc
Maximum power dissipation	0.825 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Case X	11°C/W
Case Y	See MIL-STD-1835
Junction temperature (T_J)	+175°C
Storage temperature range	-65°C to +150°C
Temperature under bias	-55°C to +125°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc minimum to +5.5 V dc maximum
Ground voltage (GND)	0 V dc
Input high voltage (V_{IH})	2.2 V dc minimum
Input low voltage (V_{IL})	0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) . . . . . 3/ percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ Values will be added when they become available.

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Pennsylvania Street, N.W., Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit will be provided when RHA product becomes available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in for device class M (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -2.0 mA $V_{IN} = V_{IH}(Min)$, $V_{IL}(Max)$	1,2,3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8.0 mA $V_{IN} = V_{IH}(Min)$, $V_{IL}(Max)$	1,2,3	All		0.4	V
Input high voltage 1/	V_{IH}		1,2,3	All	2.2		V
Input low voltage 1/	V_{IL}		1,2,3	All		0.8	V
Input leakage current	I_{IX}	V_{CC}= Max	1,2,3	All	-10	+10	µA
Output short circuit current 2/	I_{OS}	V_{CC} = max. $V_{OUT} = V_{SS}$	1,2,3	All	-90		mA
Power supply current 3/	I_{CC1}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, V_{IN} = 0 to 3.0 V	1,2,3	01,04		110	mA
				02,05		130	
				03,06		150	
Power supply current 4/	I_{CC2}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, V_{IN} = 0 to 3.0 V	1,2,3	ALL		80	mA
Standby current 5/	I_{CC3}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, All inputs = V_{CC}	1,2,3	All		30	mA
Input capacitance 6/	C_{IN}	V_{CC} = 5.0 V, T = 25°C, f = 1 MHz, (see 4.4.1e)	4	All		10	pF
Output capacitance 6/	C_{OUT}	V_{CC} = 5.0 V, T = 25°C, f = 1 MHz (see 4.4.1e)	4	All		12	pF
Functional testing		See 4.4.1c	7,8A,8B	All			

See footnotes at end of table

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Write clock cycle	t_{CKW}	See figures 3 and 4 7/	9,10,11	01,04	30		ns
				02,05	20		
				03,06	14		
Read clock cycle	t_{CKR}		9,10,11	01,04	30		ns
				02,05	20		
				03,06	14		
Clock high	t_{CKH}		9,10,11	01,04	12		ns
				02,05	9		
				03,06	6.5		
Clock low	t_{CKL}		9,10,11	01,04	12		ns
				02,05	9		
				03,06	6.5		
Data access time 8/	t_A		9,10,11	01,04		20	ns
				02,05		15	
				03,06		10	
Previous output data hold after read high	t_{OH}		9,10,11	ALL	0		ns
Previous flag hold after read/write high	t_{FH}		9,10,11	ALL	0		ns
Data set-up	t_{SD}		9,10,11	01,04	12		ns
				02,05	9		
				03,06	7		
Data hold	t_{HD}		9,10,11	ALL	0		ns
Enable set-up	t_{SEN}		9,10,11	01,04	12		ns
				02,05	9		
				03,06	7		
Enable hold	t_{HEN}		9,10,11	ALL	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Flag Delay	t_{FD}	See figures 3 and 4 7/	9,10,11	01,04		20	ns
				02,05		15	
				03,06		10	
Opposite clock after clock 9/	t_{SKEW1}		9,10,11	ALL	0		ns
Opposite clock before clock 10/	t_{SKEW2}		9,10,11	01,04	30		ns
				02,05	20		
				03,06	14		
Master peset pulse width (MR low)	t_{PMR}		9,10,11	01,04	30		ns
				02,05	20		
				03,06	14		
Last valid clock low set-up to MR low	t_{SCMR}		9,10,11	ALL	0		ns
Data hold from $\overline{MR}$ low	t_{OHMR}		9,10,11	ALL	0		ns
Master reset recovery ($\overline{MR}$ high set-up to first enabled write/read)	t_{MRR}		9,10,11	01,04	30		ns
				02,05	20		
				03,06	14		
$\overline{MR}$ high to flags valid	t_{MRF}		9,10,11	01,04		30	ns
				02,05		20	
				03,06		14	
$\overline{MR}$ high to data outputs low	t_{AMR}		9,10,11	01,04		30	ns
				02,05		20	
				03,06		14	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

1/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.

2/ Test no more than one output at a time and do not test any output for more than one second.

3/ Input signals switch from 0 V to 3 V with a rise/fall time of 3 ns or less, clocks and clock enables switch at maximum frequency (f_{MAX}), while data inputs switch at $f_{MAX}/2$.

4/ Input signals switch from 0 V to 3 V with a rise/fall time of 3 ns or less, clocks and clock enables switch at 20 MHz, while the data inputs switch at 10 MHz.

5/ All input signals are connected to V_{CC}. All outputs are unloaded. Read and write clocks switch at maximum frequency.

6/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.

7/ AC tests are performed with input rise and fall times of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load in figure 4 unless otherwise noted.

8/ Access time includes all data outputs switching simultaneously.

9/ t_{SKEW1} is the minimum time an opposite clock can occur after a clock and still be guaranteed not to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW1} after the clock, the decision of whether or not to include the opposite clock in the current clock cycle is arbitrary. The opposite clock is the signal to which a flag is not synchronized; i.e., CKW is the opposite clock for Empty and Almost Empty flags, CKR is the opposite clock for the Almost Full flag. The clock is the signal to which a flag is synchronized; i.e., CKW is the clock for the Almost Full flag, CKR is the clock for Empty and Almost Empty flags.

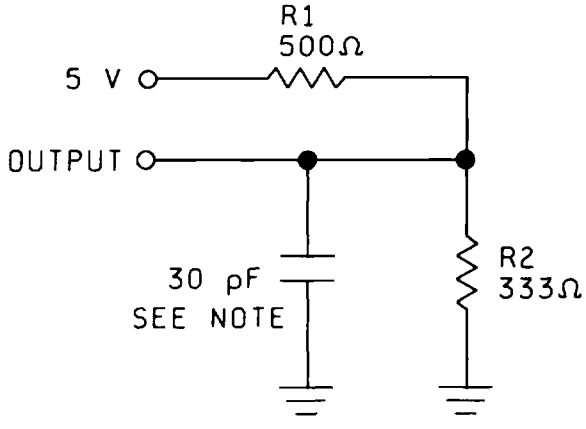
10/ t_{SKEW2} is the minimum time an opposite clock can occur before a clock and still be guaranteed to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW2} before the clock, the decision of whether or not to include the opposite clock in the current clock cycle is arbitrary.

Device Types	ALL	
Case Outlines	X	Y
Terminal Number	Terminal Symbol	
1	D_3	NC
2	D_2	D_3
3	D_1	D_2
4	D_0	D_1
5	$\overline{ENW}$	D_0
6	CKW	$\overline{ENW}$
7	V_{CC}	CKW
8	V_{SS}	V_{CC}
9	F_1	V_{SS}
10	F_2	F_1
11	Q_0	F_2
12	Q_1	NC
13	Q_2	Q_0
14	Q_3	Q_1
15	Q_4	Q_2
16	Q_5	Q_3
17	Q_6	NC
18	Q_7	Q_4
19	Q_8	Q_5
20	$\overline{ENR}$	Q_6
21	CKR	Q_7
22	V_{SS}	Q_8
23	$\overline{MR}$	$\overline{ENR}$
24	D_8	CKR
25	D_7	V_{SS}
26	D_6	$\overline{MR}$
27	D_5	NC
28	D_4	D_8
29	---	D_7
30	---	D_6
31	---	D_5
32	---	D_4

FIGURE 2. Terminal connections.

F1	F2	State	Number of words in FIFO, device types 01-03	Number of words in FIFO, device types 04-06
0	0	Empty	0	0
1	0	Almost Empty	1-16	1-16
1	1	Intermediate Range	17-2031	17-495
0	1	Almost Full or Full	2032-2048	496-512

FIGURE 3. Flag truth tables.



Note: Including scope and jig. (minimum values)

AC test conditions

Input pulse levels	GND to 3.0 V
Input rise and fall levels	≤ 3 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 4. Output load circuit.

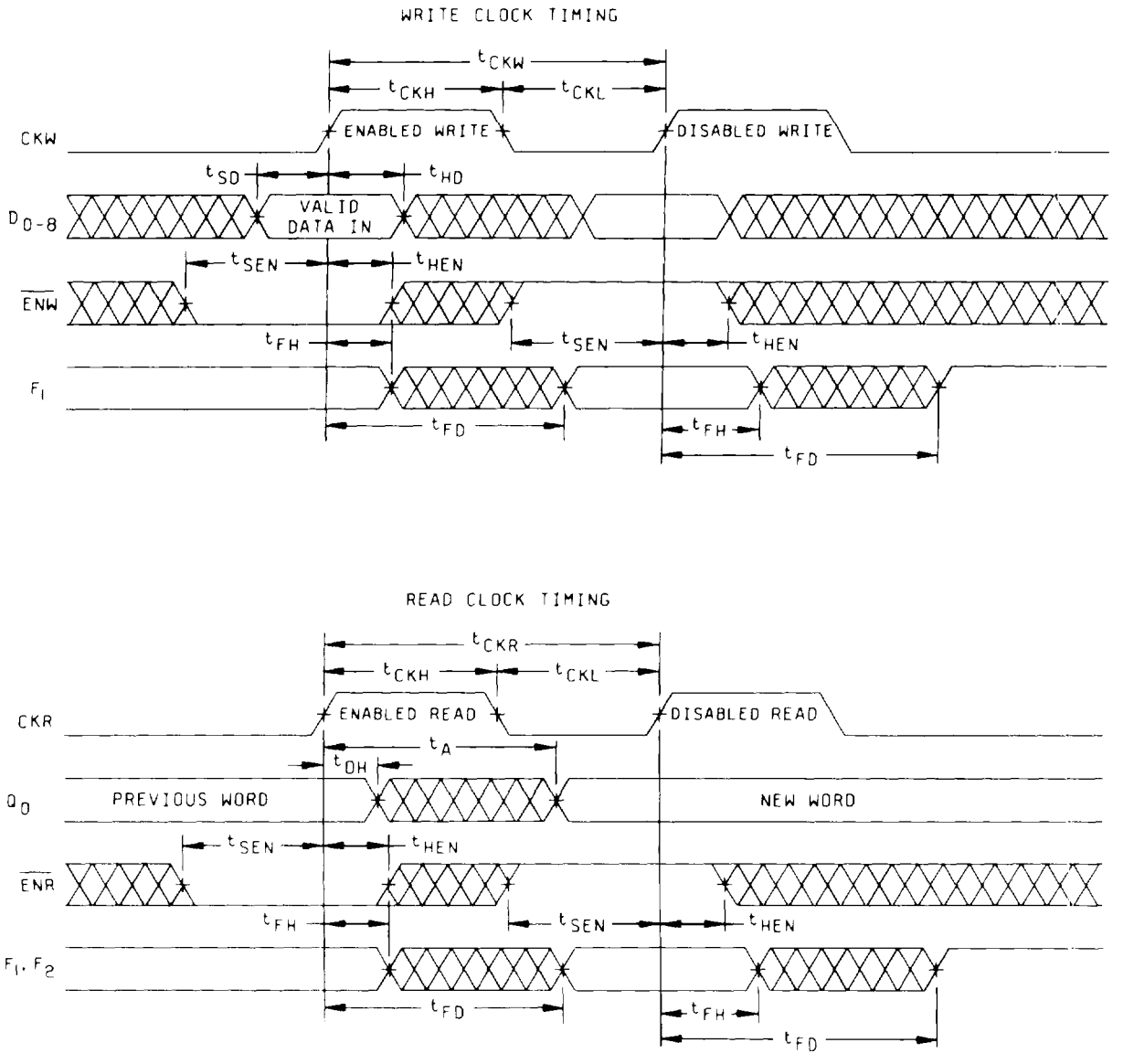


FIGURE 4. Switching waveforms.

MASTER RESET TIMING
SEE NOTES 1, 2, 3, AND 4

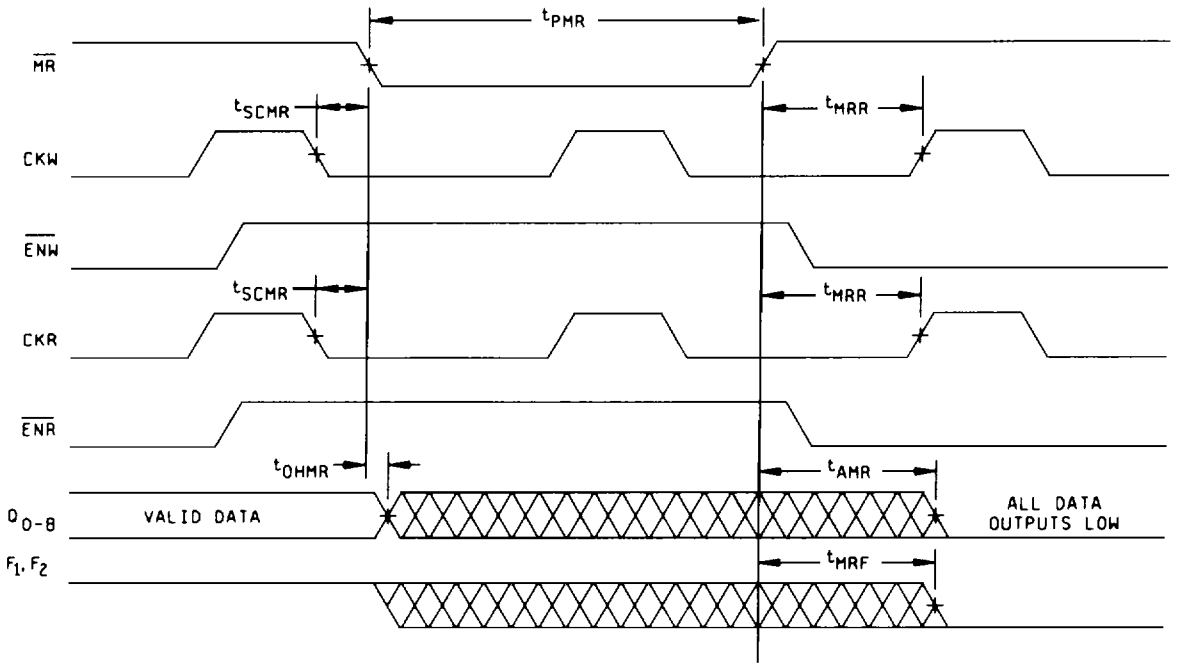
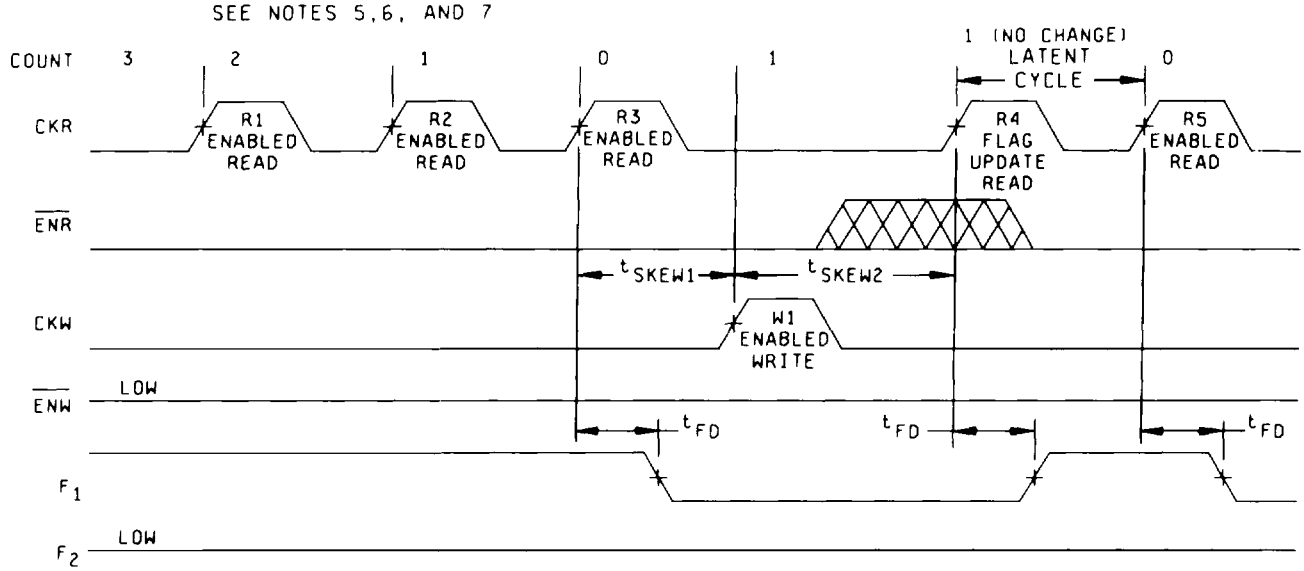


FIGURE 4. Switching waveforms - continued.

READ TO EMPTY TIMING
SEE NOTES 5,6, AND 7



READ TO EMPTY TIMING WITH FREE-RUNNING CLOCKS
SEE NOTES 5,6, AND 8

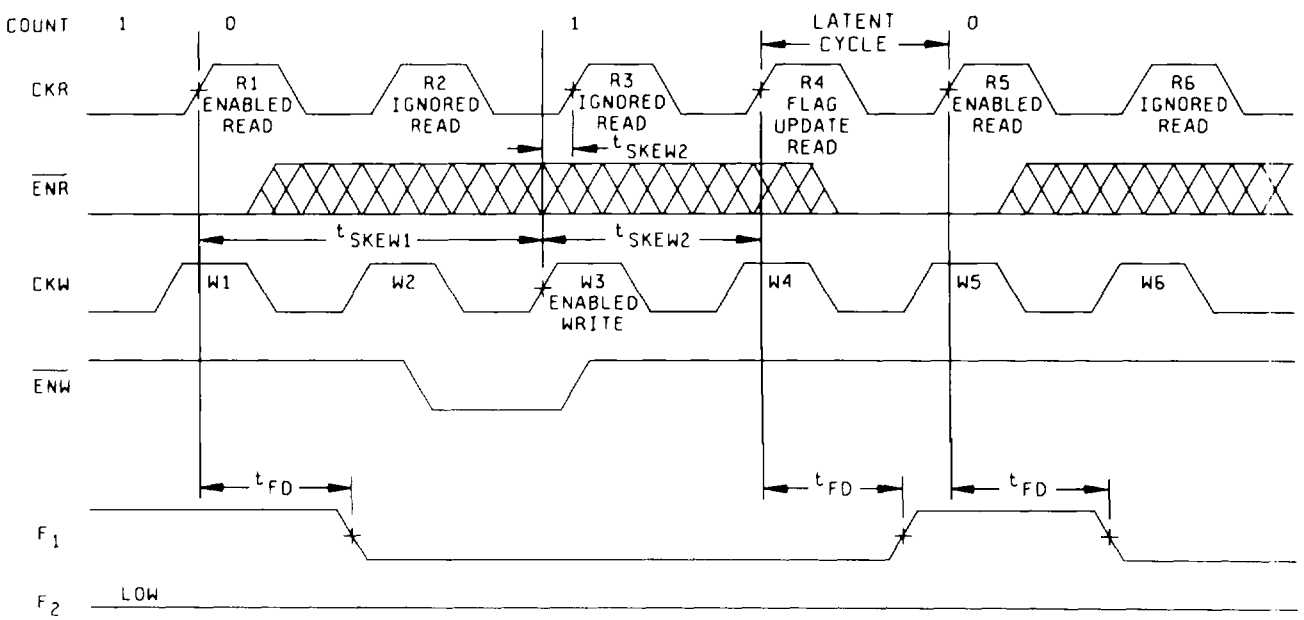


FIGURE 4. Switching waveforms - continued.

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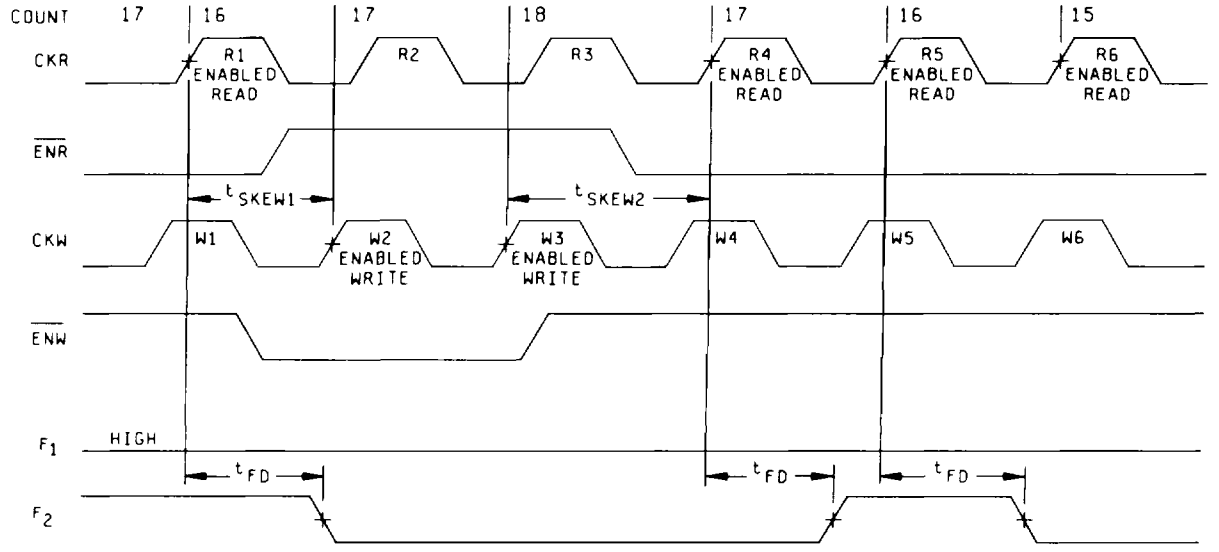
READ TO ALMOST EMPTY TIMING WITH FREE-RUNNING CLOCKS
SEE NOTES 5 AND 6



READ TO ALMOST EMPTY TIMING DIAGRAM WITH READ FLAG UPDATE CYCLE AND FREE-RUNNING CLOCKS
SEE NOTES 5,6,9 AND 10

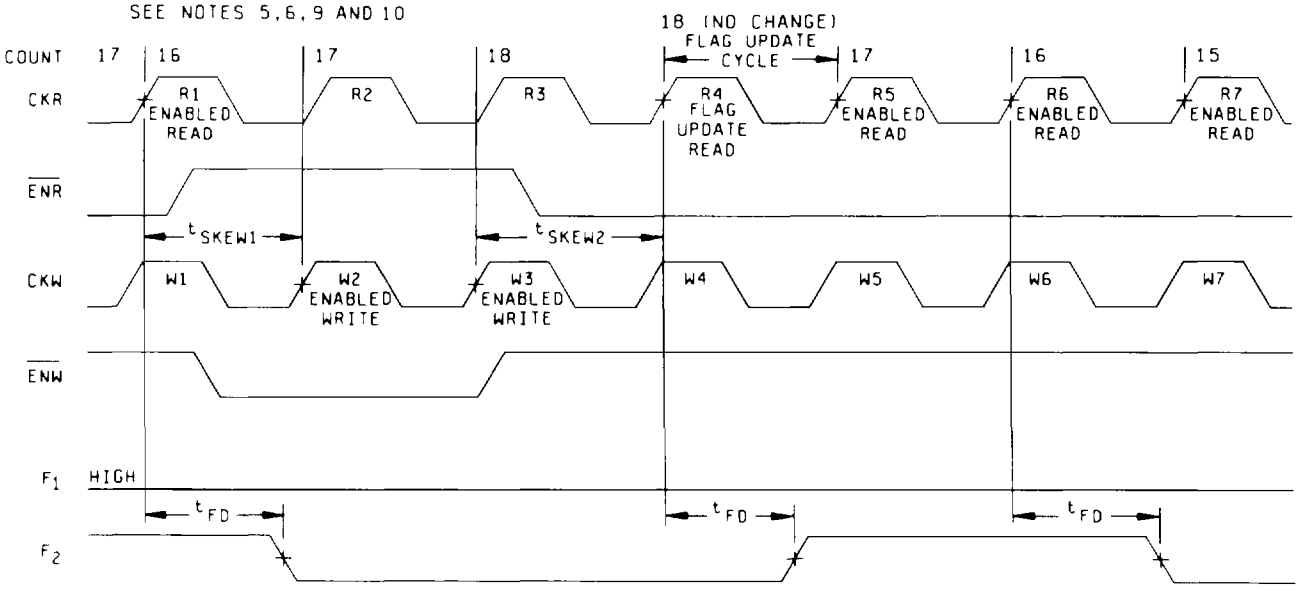
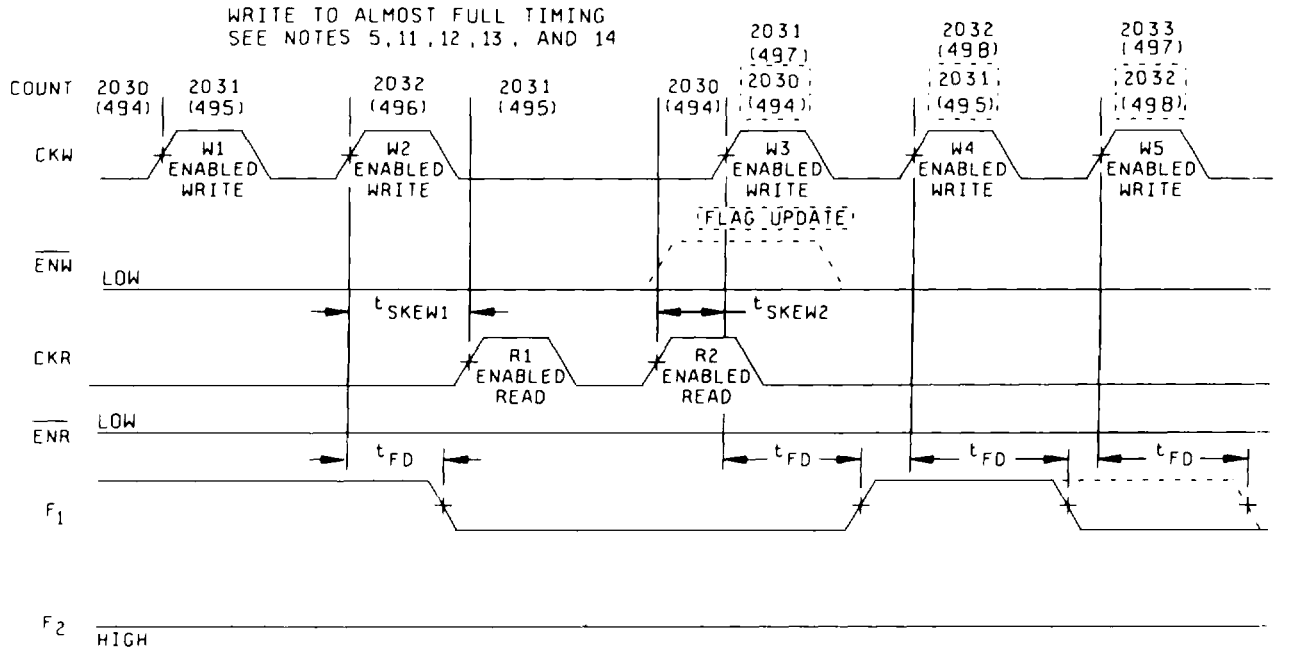


FIGURE 4. Switching waveforms - continued.



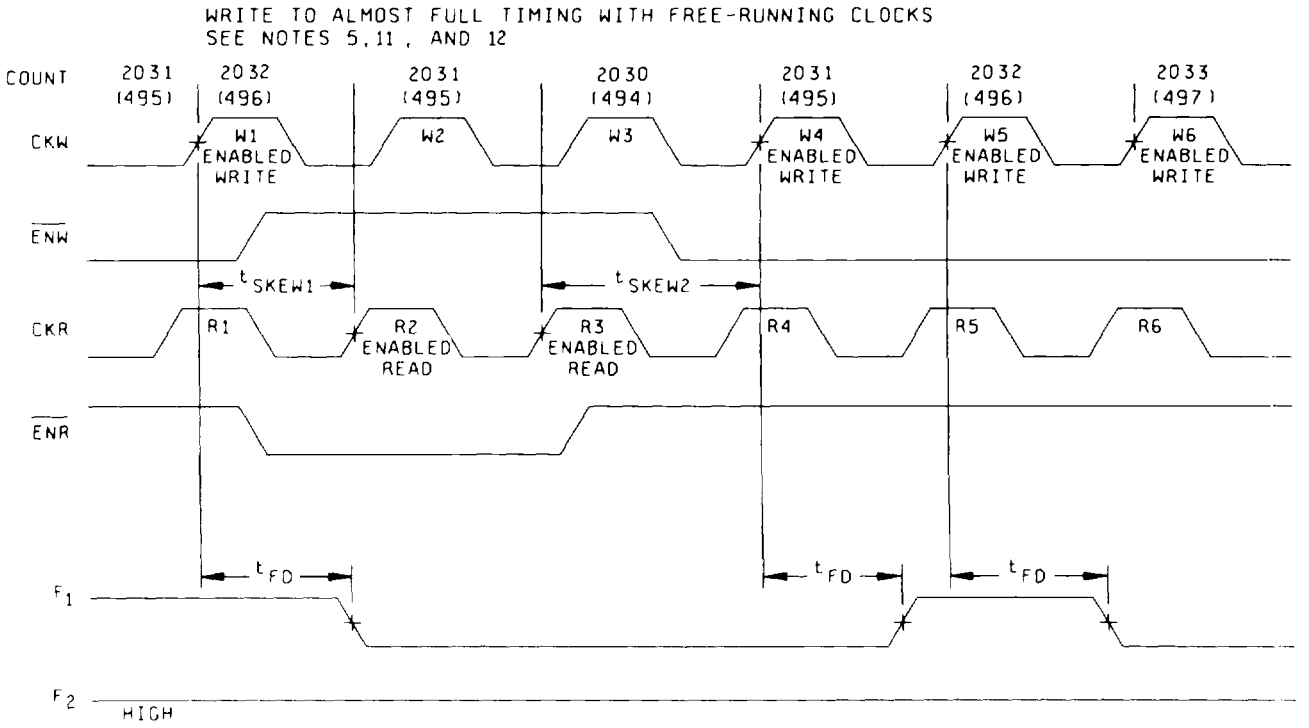


FIGURE 4. Switching waveforms - continued.

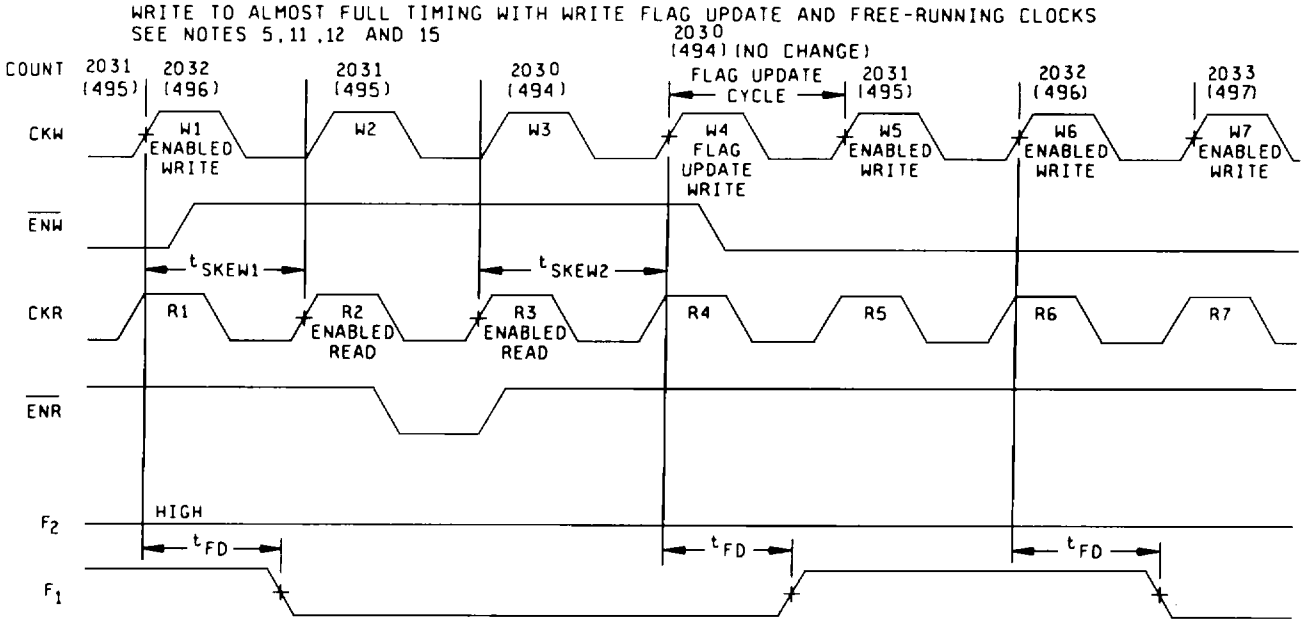


FIGURE 4. Switching waveforms.

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NOTES:

1/ To only perform reset (no programming), the following criteria must be met: $\overline{ENW}$ or CKW must be inactive while MR is low.
2/ To only perform reset (no programming), the following criteria must be met: $\overline{ENR}$ or CKR must be inactive while MR is low.
3/ All data outputs Q_{0-8} go low as a result of the rising edge of $\overline{MR}$ after t_{AMR}.
4/ All data outputs Q_{0-8} will remain valid until t_{OHMR} if either the first read shown did not occur or if the read occurred soon enough such that the valid data was caused by it.
5/ "Count" is the number of words in the FIFO.
6/ CKR is clock; CKW is opposite clock.
7/ R3 updates the flag to the empty state by bringing F1 low. Because W1 occurs greater than t_{SKEW1} after R3, R3 does not recognize W1 when updating flag status. But because W1 occurs greater than t_{SKEW2} before R4, R4 includes W1 in the flag update and, therefore, updates FIFO to almost empty state. It is important to note that R4 is a latent cycle; i.e., it only updates the flag status regardless of the state of ENR. It does not change the count or the FIFO's data outputs.
8/ R2 is ignored because the FIFO is empty (count=0). It is important to note that R3 is also ignored because W3, the first enabled write after empty, occurs less than t_{SKEW2} before R3. Therefore, the FIFO still appears empty when R3 occurs. Because W3 occurs greater than t_{SKEW2} before R4, R4 includes W3 in the flag update.
9/ R4 only updates the flag status. It does not affect the count because ENR is high.
10/ When making the transition from almost empty to intermediate, the count must increase by two (16 - 18; two enabled writes: W2, W3) before a read (R4) can update flags to the less than half full state.
11/ CKW is clock and CKR is opposite clock.
12/ Count = 257 = half full for devices 4,5, and 6; count = 1025 = half full for devices 1,2, and 3.
13/ The dashed lines show W3 as a flag update write rather than an enabled write because ENW is deasserted.
14/ W2 updates the flag to the almost full state by assering PAFE. Because R1 occurs greater than t_{SKEW1} after W2 does not recognize R1 when updating the flag status. W3 includes R2 in the flag update because R2 occurs greater than t_{SKEW2} before W3. Note that W3 does not have to be enabled to update flags.
15/ When making the transition from almost empty to intermediate, the count must increase by two (16 - 18; two enabled writes: W2 and W3) before a read (R4) can update flags to the intermediate state.

FIGURE 4. Switching waveforms - continued.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9	1,7,9
2	Static burn-in I and II (method 1015)	Not required	Not required	Required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9, 10,11
7	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
8	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7, 8A,8B Δ	1,2,3,7, 8A,8B,9, 10,11 Δ
9	Group D end-point electrical parameters	2,3, 8A,8B	2,3, 8A,8B	2,3, 8A,8B
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{IX}	10% of specified value in table IA
I_{OS}	10% of specified value in table IA
I_{CC3}	10% of specified value in table IA

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-PRF-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC standard number 17 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IIB herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device classes Q and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

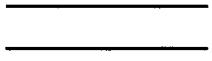
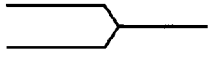
6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows:

C_{IN}	Input terminal capacitance.
C_{OUT}	Output terminal capacitance.
I_{CC}	Supply current.
I_{IX}	Input current.
I_{OZ}	Output current.
T_C	Case temperature.
V_{CC}	Positive supply voltage (5.0 V).

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 96-02-20

Approved sources of supply for SMD 5962-94567 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard Microcircuit Drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-9456701QXX	65786	CY7C443-30DMB
5962-9456701QYX	65786	CY7C443-30LMB
5962-9456702QXX	65786	CY7C443-20DMB
5962-9456702QYX	65786	CY7C443-20LMB
5962-9456703QXX	65786	CY7C443-14DMB
5962-9456703QYX	65786	CY7C443-14LMB
5962-9456704QXX	65786	CY7C441-30DMB
5962-9456704QYX	65786	CY7C441-30LMB
5962-9456705QXX	65786	CY7C441-20DMB
5962-9456705QYX	65786	CY7C441-20LMB
5962-9456706QXX	65786	CY7C441-14DMB
5962-9456706QYX	65786	CY7C441-14LMB

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65786	Cypress Semiconductor 3901 North First Street San Jose, CA 95134 - 1599