PERICOM

PI6C9930

# Zero-Delay Clock Buffer

## Features

- Zero input to output delay
- Seven copies of the REF input divided by 2
- Seven copies of REF input plus one REFx2
- 15 - 80 MHz output operation
- 50% duty cycle
- Low skew (< 250 ps pin to pin)
- Vcc = 3.3V ±0.3V, TA = 0° to 70°
- Low jitter (< 200 ps peak to peak)
- Low noise balanced drive outputs
- Packages available:
  - 24-pin 300 mil wide SOIC (S24)
  - 24-pin 209 mil wide SSOP (H24)

## Applications

- PCI 66 MHz/33MHz systems

## Product Description

The PI6C9930 Clock Buffer offers zero-delay, low-skew system clock distribution. These multiple output clock drivers optimize the timing of high-performance computer systems. Each of eight individual drivers can drive series-terminated transmission lines with impedances as low as 50Ω while delivering minimal output skews and full-swing logic levels.

Any of the eight outputs ($Q_0$-$Q_7$) can be fed back to the FB pin to complete the phase-locked loop and achieve zero-delay synchronization.

When connecting $Q_0$ to FB, the internal synchronous divide by 2 function provides the slower secondary clocks needed for peripheral devices. Connecting one of $Q_1$ - $Q_7$ outputs to FB produces seven copies of the REF input plus one REF x 2 on $Q_0$.

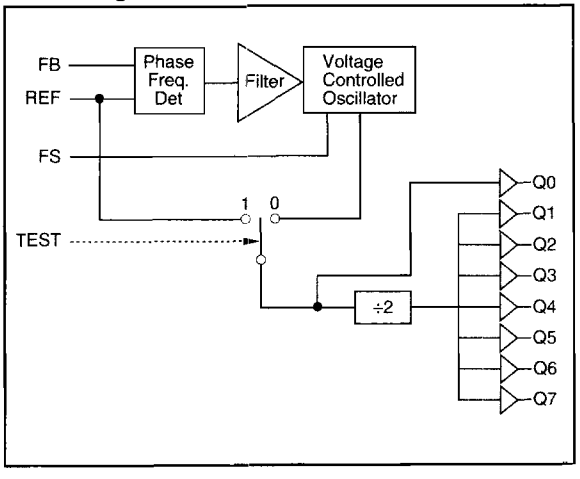
## Test Mode

In normal system operation, this pin is connected to ground.

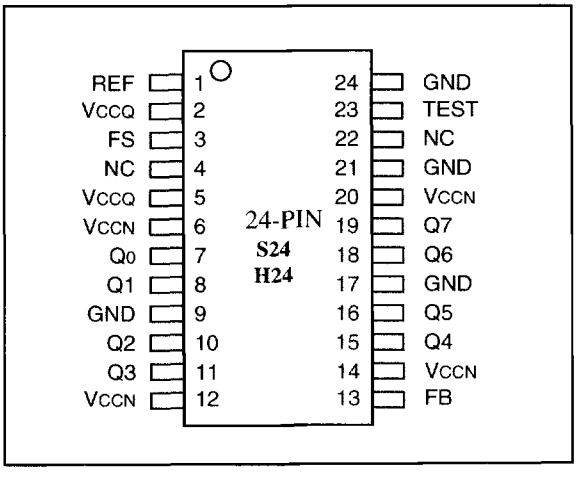
For testing purposes, the TEST pin can have a removable jumper to ground, or be tied LOW through a 100Ω resistor. This will allow drive by an external tester.

If the TEST input is forced HIGH, the device will operate with its internal phase-locked loop disconnected, and input levels supplied to REF will directly control all outputs. Relative output to output functions are the same as in normal mode.

## Block Diagram




## Pinout



## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

| | |
|---|---|
| Storage Temperature | –65°C to +150°C |
| Ambient Temperature with Power Applied | –55°C to +125°C |
| Supply Voltage to Ground Potential | –0.5V to +7.0V |
| DC Input Voltage | –0.5V to +7.0V |
| Output Current into Outputs (LOW) | 64 mA |
| Static Discharge Voltage (per MIL-STD-883, Method 3015) | >2001V |
| Latch-Up Current | >200 mA |
| Maximum Power/Package | TBD |

**Note:**
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Operating Range

| Range | Ambient Temperature | Vcc |
|---|---|---|
| Commercial | 0°C to +70°C | 3.3V ± 0.3V |

## Pin Description

| Pin Name | I/O | Functional Description |
|---|---|---|
| REF | I | Reference Frequency Input. This input supplies the frequency and timing against which all functional variation is measured. |
| FB | I | PLL feedback input (typically connected to one of eight outputs). |
| FS | I | Two-level frequency range select. Internal Pull-up. |
| TEST | I | Two-level select. See Test Mode section. Internal Pull-up |
| Q[0-7] | O | Clock Outputs. |
| $V_{CCN}$ | PWR | Power supply for output drivers. |
| $V_{CCQ}$ | PWR | Power supply for internal circuitry. |
| $\overline{GND}$ | PWR | Ground. |
| NC | - | No Connection |

## Electrical Characteristics Over Operating Range

| Symbol | Parameter | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $I_{OH}$ = -24 mA | 2.4 | — | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $I_{OL}$ = +24 mA | — | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage (REF and FB inputs only) | | 2.0 | Vcc | V |
| $V_{IL}$ | Input LOW Voltage (REF and FB inputs only) | | -0.5 | 0.8 | V |
| $I_{IH}$ | Input HIGH Leakage Current (REF, Test, FS, and FB inputs only) | $V_{CC}$ = Max., $V_{IN}$ = Max. | — | 10 | µA |
| $I_{IL}$ | Input LOW Leakage Current (REF, Test, FS, and FB inputs only) | $V_{CC}$ = Max., $V_{IN}$ = 0.4V | -500 | — | µA |
| $I_{OS}$ | Output Short Circuit Current[2] | $V_{CC}$ = Max., $V_{OUT}$ = GND (25°C only) | — | -250 | mA |
| $I_{CCQ}$ | Operating Current Used by Internal Circuitry | $V_{CCN}$ = $V_{CCQ}$ = Max., All Inputs Select Open | — | 85 | mA |
| $I_{CCN}$ | Output Buffer Current per Output Pair[3] | $V_{CCN}$ = $V_{CCQ}$ = Max., $I_{OUT}$ = 0 mA Inputs Selects Open, $f_{MAX}$ | — | 14 | mA |
| PD | Power Dissipation per Output Pair[4] | $V_{CCN}$ = $V_{CCQ}$ = Max., $I_{OUT}$ = 0 mA Inputs Selects Open, $f_{MAX}$ | — | 78 | mW |

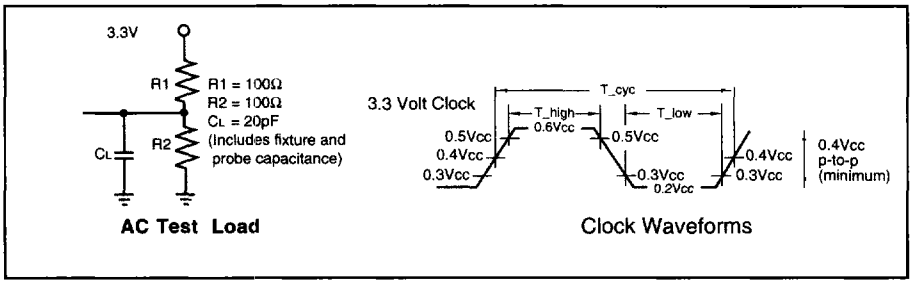
**Notes:**

1. If these inputs, which are normally wired to Vcc, GND, are switched, the function and timing of the outputs may glitch and the PLL may require an additional $t_{LOCK}$ time before all datasheet limits are achieved.
2. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle. Room temperature only.
3. (TBD) Total output current per output pair is approximated by the following expression that includes device current plus load current.
   $I_{CCN}$ = [(4 + 0.11F) + [((835 − 3F)/Z) + (.0022FC)]N1] x 1.1
   Where: F = frequency in MHz; Z = line impedance in ohms
   C = capacitive load in pF; FC = F · C
   N = number of loaded outputs: 0, 1, or 2
4. (TBD) Total power dissipation per output pair can be approximated by the following expression that includes device power dissipation plus power dissipation due to the load circuit:
   PD = [(22 + 0.61F) + [((1550 - 2.7F)/Z) + (0.125FC)]N] x 1.1.
   (See note 3 for variable definition.)
5. TBD.
6. Applies to REF and FB inputs only. Tested initially and after any design or process changes that may affect these parameters.

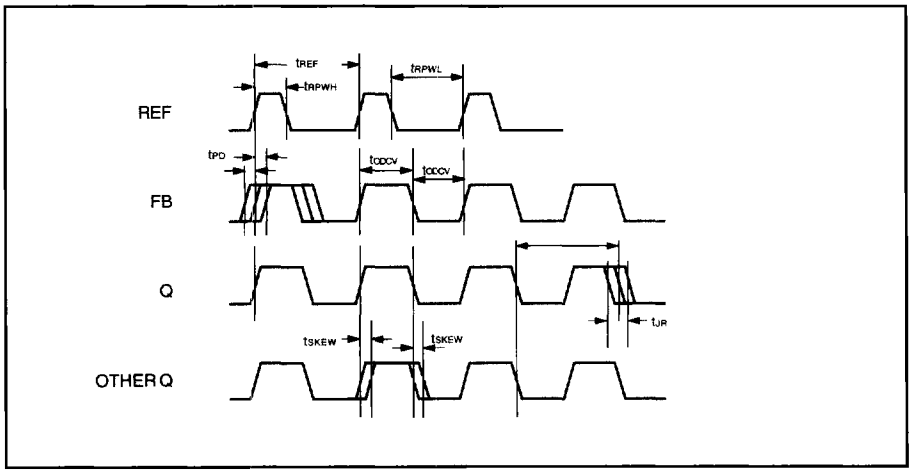
## Capacitance[1,6] ($T_A$ = 25°C, f = 1 MHz, $V_{IN}$ = 0V, $V_{OUT}$ = 0V)

| Parameter | Description | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25C, f = 1 MHz, $V_{CC}$ = 3.3V | 10 | pF |

## AC Test Load and Waveform




## AC Timing Diagram



## Switching Characteristics Over Operating Range[14]

(Commercial: $T_A$ = 0°C to 70°C, $V_{CC}$ = 3.3V ±10%)

| Symbol | Description | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{NOM}$ | Operation Clock Frequency in MHz | FS = LOW | 15 | — | 40 | MHz |
| | | FS = HIGH or Floating | 30 | — | 80 | |
| $t_{RPWH}$ | REF Pulse Width HIGH | | 5.0 | — | — | ns |
| $t_{RPWL}$ | REF Pulse Width LOW | | 5.0 | — | — | ns |
| $t_{SKEW}$ | Zero Output Skew (All Outputs)[7,8] | | — | 0.25 | 0.5 | ns |
| $t_{DEV}$ | Device-to-Device Skew[9,10] | | — | — | 1.0 | ns |
| $t_{PD}$ | Propagation delay, REF Rise to FB Rise | | -0.5 | 0.0 | +0.5 | ns |
| $t_{CYC}$ | Output Duty Cycle, Target Spec @ 66MHz | | 45 | 50 | 55 | % |
| Srate | Slew Rate[11,12] | | 1 | 1.5 | 4 | V/ns |
| $t_{LOCK}$ | PLL Lock Time[13] | | — | — | 0.5 | ms |
| $t_{JR}$ | Cycle-to-Cycle Output Jitter | Peak to Peak[10] | — | — | 200 | ps |
| | | RMS[10] | — | — | 25 | ps |

**Notes:**

7. Skew is defined as the time between the earliest and the latest output transition among all outputs with AC Test Load.
8. $t_{SKEW}$ is defined as the skew between outputs.
9. $t_{DEV}$ is the output-to-output skew between any two outputs on separate devices operating under the same conditions ($V_{CC}$, ambient temperature, air flow, etc.).
10. Tested initially and after any design or process changes that may affect these parameters.
11. Specified with outputs loaded without 20pF in AC Test Load.
12. Slew Rate (SRATE) measured between 0.3Vcc and 0.5Vcc (0.99V and 1.65V).
13. $t_{LOCK}$ is the time that is required before synchronization is achieved. This specification is valid only after Vcc is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until $t_{PD}$ is within specified limits.
14. Test measurement levels for the PI6C9930 are PCI levels (0.4Vcc to 0.4Vcc). Test conditions assume signal transition times of 2ns or less and output loading as shown in the AC Test Loads and Waveforms unless otherwise specified.