HARRIS SEMICONDUCTOR

CA3240

Dual BiMOS Operational Amplifier with MOSFET Inpu/Bipolar Output

March 1993

Features

- Dual Version of CA3140
- Internally Compensated
- MOSFET Input Stage
  - Very High Input Impedance (Z_{IN}) 1.5TΩ Typ
  - Very Low Input Current (I_I) 10pA Typ. at ±15V
  - Wide Common-Mode Input Voltage Range (V_{ICR}): Can be Swung 0.5V Below Negative Supply Voltage Rail
- Directly Replaces Industry Type 741 in Most Applications

Applications

- Ground Referenced Single Amplifiers in Automobile and Portable Instrumentation
- Sample and Hold Amplifiers
- Long Duration Timers/Multivibrators (Microseconds-Minutes-Hours)
- Photocurrent Instrumentation
- Intrusion Alarm System
- Comparators
- Instrumentation Amplifiers
- Active Filters
- Function Generators
- Power Supplies

Description

The CA3240A and CA3240 are dual versions of the popular CA3140 series integrated circuit operational amplifiers. They combine the advantages of MOS and bipolar transistors on the same monolithic chip. The gate-protected MOSFET (PMOS) input transistors provide high input impedance and a wide common-mode input voltage range (typically to 0.5V below the negative supply rail). The bipolar output transistors allow a wide output voltage swing and provide a high output current capability.

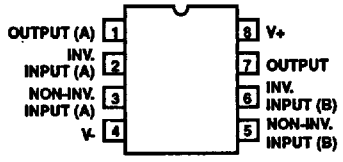
The CA3240A and CA3240 are compatible with the industry standard 1458 operational amplifiers in similar packages.The offset null feature is available only when these types are supplied in the 14 lead dual-in-line plastic package (E1 suffix).

Ordering Information

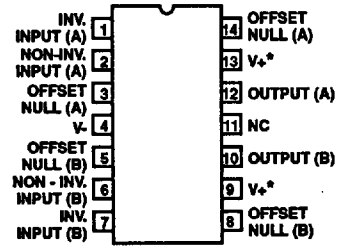
PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3240AE	-40°C to +85°C	8 Lead Plastic DIP
CA3240AE1	-40°C to +85°C	14 Lead Plastic DIP
CA3240E	-40°C to +85°C	8 Lead Plastic DIP
CA3240E1	-40°C to +85°C	14 Lead Plastic DIP

Pinouts

CA3240, CA3240A
(PDIP)
TOP VIEW

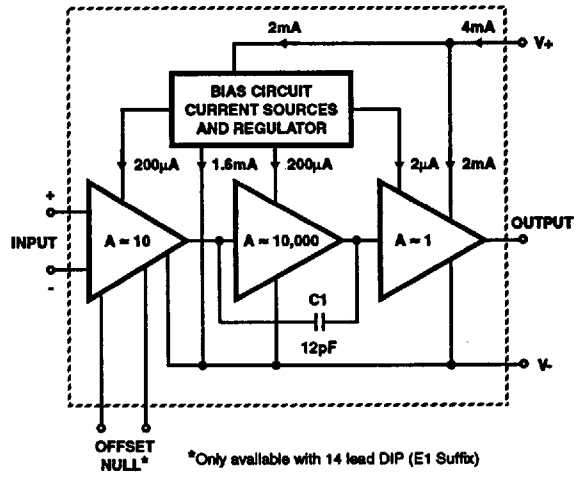


CA3240, CA3240A
(PDIP)
TOP VIEW



* Pins 9 and 13 internally connected through approximately 3Ω

Block Diagram



*Only available with 14 lead DIP (E1 Suffix)

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 1050.2

Specifications CA3240, CA3240A

Absolute Maximum Ratings

Supply Voltage (between V+ and V-) 36V
Differential Input Voltage 8V
Input Voltage ..... (V+ +8V) to (V- -0.5V)
Input Current 1mA
Output Short Circuit Duration (Note 1) ..... Indefinite
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range ..... $-40°C \leq T_A \leq +85°C$
Storage Temperature Range ..... $-65°C \leq T_A \leq +150°C$
Operating Voltage Range ..... 4V to 36V or ±2V to ±18V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

For Equipment Design, V+ = 15V, V- = -15V, T_A = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	LIMITS						UNITS
		CA3240A			CA3240			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	-	2	5	-	5	15	mV
Input Offset Current	I_{IO}	-	0.5	20	-	0.5	30	pA
Input Current	I_I	-	10	40	-	10	50	pA
Large-Signal Voltage Gain (See Figures 2, 17)	A_{OL} (Note 2)	20	100	-	20	100	-	kV/V
		86	100	-	86	100	-	dB
Common-Mode Rejection Ratio (See Figure 7)	CMRR	-	32	320	-	32	320	µV/V
		70	90	-	70	90	-	dB
Common-Mode Input Voltage Range (See Figure 14)	V_{ICR}	-15	-15.5 to +12.5	12	-15	-15.5 to +12.5	11	V
Power Supply Rejection Ratio (See Figure 9)	$\Delta V_{IO}/\Delta V\pm$	-	100	150	-	100	150	µV/V
	PSRR	76	80	-	76	80	-	dB
Maximum Output Voltage (Note 3) (See Figures 14, 20)	V_{OM+}	12	13	-	12	13	-	V
	V_{OM-}	-14	-14.4	-	-14	-14.4	-	V
Maximum Output Voltage (Note 4)	V_{OM-}	0.4	0.13	-	0.4	0.13	-	V
Supply Current (See Figure 5) For Both Amps.	I+	-	8	12	-	8	12	mA
Total Device Dissipation	P_D	-	240	360	-	240	360	mW

NOTES:

1. Short circuit may be applied to ground or to either supply. Temperatures and/or supply voltages must be limited to keep dissipation within maximum rating.
2. At V_O = 26Vp-p, +12V, -14V and R_L = 2kΩ.
3. At R_L = 2kΩ.
4. At V+ = 5V, V- = GND, I_{SINK} = 200µA.

Electrical Specifications For Equipment Design, V+ = +15V, V- = -15V, T_A = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	TYPICAL VALUES		UNITS
			CA3240A	CA3240	
Input Offset Voltage Adjustment Resistor (E1 Package Only)		Typical Value of Resistor Between Terms. 4 and 3(5) or Between 4 and 14(8) to Adjust Maximum V_{IO}	18	4.7	kΩ
Input Resistance	R_I		1.5	1.5	TΩ
Input Capacitance	C_I		4	4	pF
Output Resistance	R_O		60	60	Ω
Equivalent Wideband Input Noise Voltage (See Figure 19)	e_N	BW = 140kHz, R_S = 1MΩ	48	48	μV
Equivalent Input Noise Voltage (See Figure 8)	e_N	f = 1kHz, R_S = 100Ω	40	40	$nV/\sqrt{Hz}$
		f = 10kHz, R_S = 100Ω	12	12	$nV/\sqrt{Hz}$
Short-Circuit Current to Opposite Supply	I_{OM}+	Source	40	40	mA
	I_{OM}-	Sink	11	11	mA
Gain Bandwidth Product (See Figures 3 and 17)	f_T		4.5	4.5	MHz
Slew Rate (See Figure 4)	SR		9	9	V/μs
Transient Response:					
Rise Time	t_R	R_L = 2kΩ, C_L = 100pF	0.08	0.08	μs
Overshoot (See Figure 18)	OS	R_L = 2kΩ, C_L = 100pF	10	10	%
Settling Time at 10 Vp-p (See Figure 15)					
1mV	t_S	R_L = 2kΩ, C_L = 100pF, Voltage Follower	4.5	4.5	μs
10mV	t_S	R_L = 2kΩ, C_L = 100pF, Voltage Follower	1.4	1.4	μs
Crosstalk		f = 1kHz	120	120	dB

Electrical Specifications For Equipment Design at V+ = 15V, V- = -15V, T_A = -40 to +85°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TYPICAL VALUES		UNITS
		CA3240A	CA3240	
Input Offset Voltage	$\|V_{IO}\|$	3	10	mV
Input Offset Current (Note 3)	$\|I_{IO}\|$	32	32	pA
Input Current (Note 3)	I_I	640	640	pA
Large Signal Voltage Gain (See Figures 2, 17)	A_{OL} (Note 1)	63	63	kV/V
		96	96	dB
Common Mode Rejection Ratio (See Figure 7)	CMRR	32	32	µV/V
		90	90	dB
Common Mode Input Voltage Range (See Figure 14)	V_{ICR}	-15 to +12.3	-15 to +12.3	V
Power Supply Rejection Ratio (See Figure 9)	$\Delta V_{IO}/\Delta V\pm$	150	150	µV/V
	PSRR	76	76	dB
Maximum Output Voltage (Note 2) (See Figures 14 and 20)	$V_{OM}+$	12.4	12.4	V
	$V_{OM}-$	-14.2	-14.2	V
Supply Current (See Figure 5) For Both Amps	I+	8.4	8.4	mA
Total Device Dissipation	P_D	252	252	mW
Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	15	15	µV/°C

NOTES:

1. At V_O = 26Vp-p, +12V, -14V and R_L = 2kΩ.
2. At R_L = 2kΩ.
3. At T_A = +85°C.

Electrical Specifications For Design Guidance at V+ = 5V, V- = 0V, T_A = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TYPICAL VALUES		UNITS
		CA3240A	CA3240	
Input Offset Voltage	$\|V_{IO}\|$	2	5	mV
Input Offset Current	$\|I_{IO}\|$	0.1	0.1	pA
Input Current	I_I	2	2	pA
Input Resistance	R_{IN}	1	1	TΩ
Large Signal Voltage Gain (See Figures 2 and 17)	A_{OL}	100	100	kV/V
		100	100	dB
Common-Mode Rejection Ratio	CMRR	32	32	µV/V
		90	90	dB
Common-Mode Input Voltage Range (See Figure 14)	V_{ICR}	-0.5	-0.5	V
		2.6	2.6	V
Power Supply Rejection Ratio	PSRR	31.6	31.6	µV/V
		90	90	dB
Maximum Output Voltage (See Figures 14 and 20)	V_{OM}+	3	3	V
	V_{OM}-	0.3	0.3	V
Maximum Output Current				
Source	I_{OM}+	20	20	mA
Sink	I_{OM}-	1	1	mA
Slew Rate (See Figure 4)	SR	7	7	V/µs
Gain Bandwidth Product (See Figure 3)	f_T	4.5	4.5	MHz
Supply Current (See Figure 5)	I+	4	4	mA
Device Dissipation	P_D	20	20	mW

Schematic Diagram

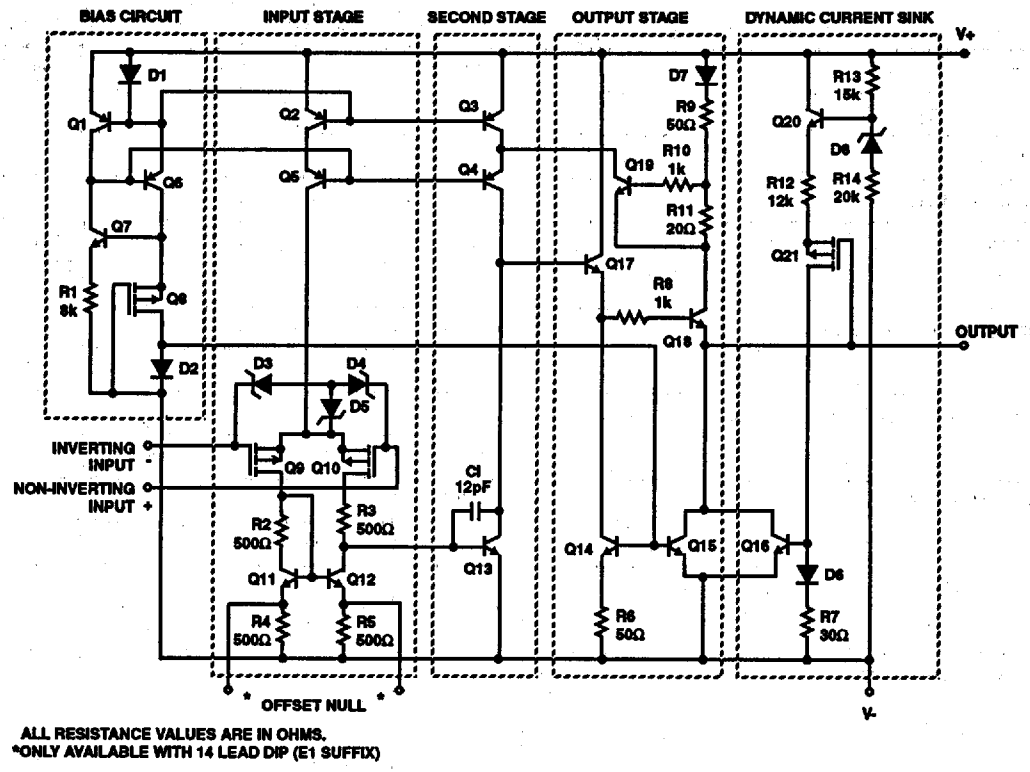


FIGURE 1. SCHEMATIC DIAGRAM OF ONE-HALF CA3240 SERIES.

Circuit Description

The schematic diagram of one amplifier section of the CA3240 is shown in Figure 1. It consists of a differential amplifier stage using PMOS transistors Q9 and Q10 with gate-to-source protection against static discharge damage provided by zener diodes D3, D4, and D5. Constant current bias is applied to the differential amplifier from transistors Q2 and Q5 connected as a constant current source. This assures a high common-mode rejection ratio. The output of the differential amplifier is coupled to the base of gain stage transistor Q13 by means of an n-p-n current mirror that supplies the required differential-to-single-ended conversion. Provision for offset null for types in the 14 lead plastic package (E1 suffix) is provided through the use of this current mirror.

The gain stage transistor Q13 has a high impedance active load (Q3 and Q4) to provide maximum open-loop gain. The collector of Q13 directly drives the base of the compound emitter-follower output stage. Pulldown for the output stage is provided by two independent circuits: (1) constant-current-connected transistors Q14 and Q15 and (2) dynamic current-sink transistor Q16 and its associated circuitry. *The level of pulldown current is constant at about 1mA for Q15 and varies from 0 to 18mA for Q16 depending on the magnitude of the voltage between the output terminal and V+.* The dynamic current sink becomes active whenever the output terminal is more negative than V+ by about 15V. When this condition exists, transistors Q21 and Q16 are turned on causing Q16 to sink current from the output terminal to V-. This current always flows when the output is in the linear region, either from the load resistor or from the emitter of Q18 if no load resistor is present. The purpose of this dynamic sink is to permit the output to go within 0.2V (V_{CE} (sat)) of V- with a 2kΩ load to ground. *When the load is returned to V+, it may be necessary to supplement the 1mA of current from Q15 in order to turn on the dynamic current sink (Q16).* This may be accomplished by placing a resistor (Approx. 2kΩ) between the output and V-.

Typical Performance Curves

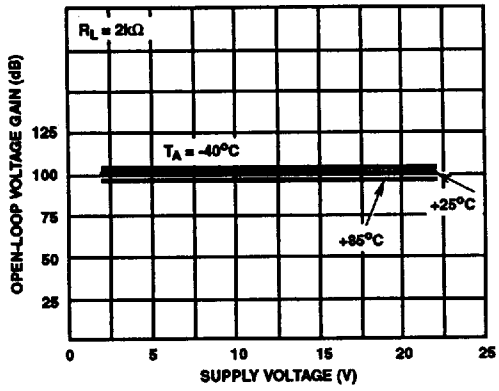


FIGURE 2. OPEN LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE

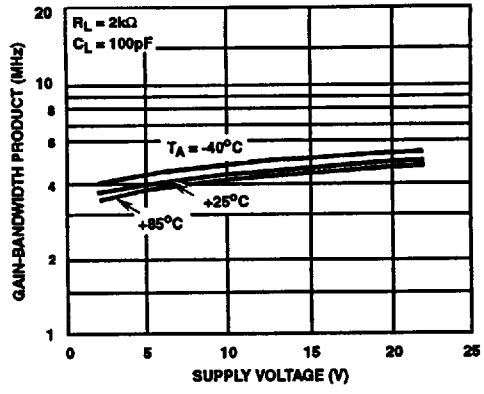


FIGURE 3. GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

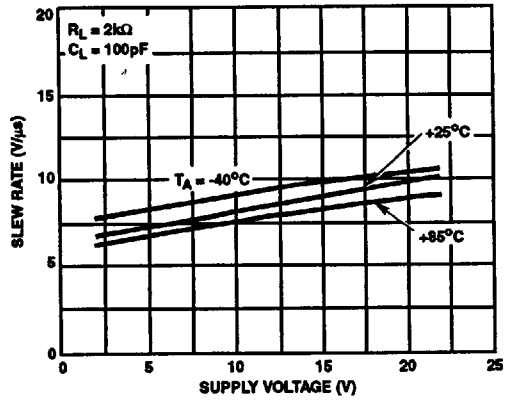


FIGURE 4. SLEW RATE vs SUPPLY VOLTAGE

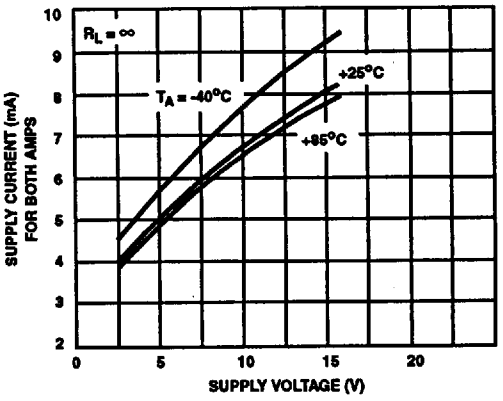


FIGURE 5. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

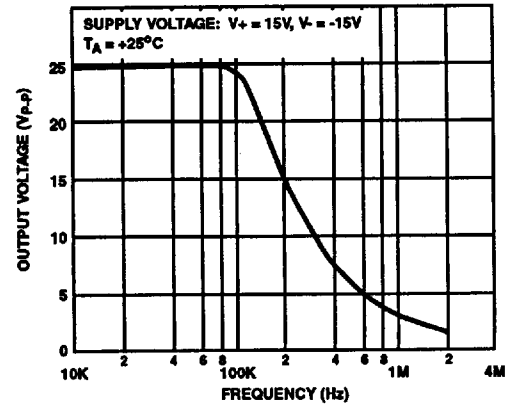


FIGURE 6. MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY

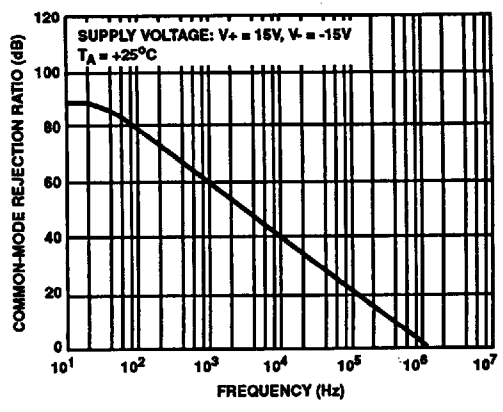


FIGURE 7. COMMON MODE REJECTION RATIO vs FREQUENCY

Typical Performance Curves (Continued)

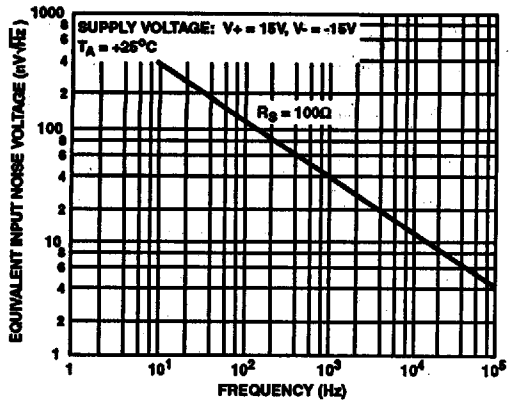


FIGURE 8. EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

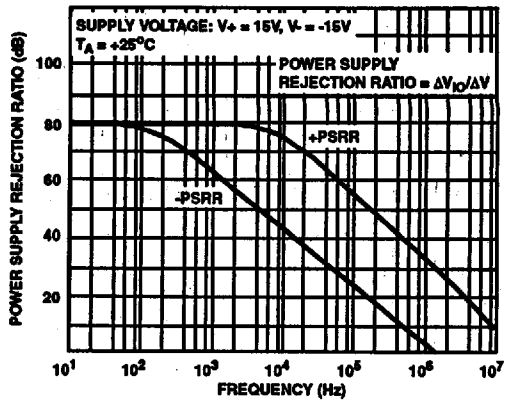


FIGURE 9. POWER SUPPLY REJECTION RATIO vs FREQUENCY

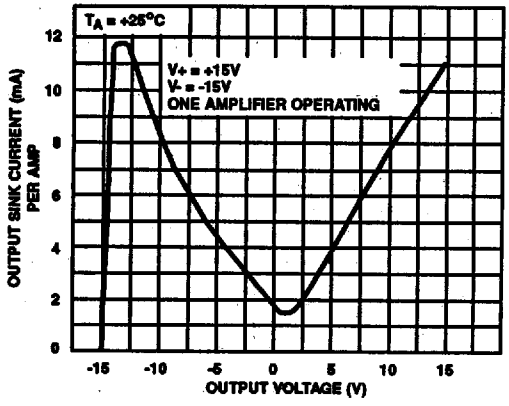


FIGURE 10. OUTPUT SINK CURRENT vs OUTPUT VOLTAGE

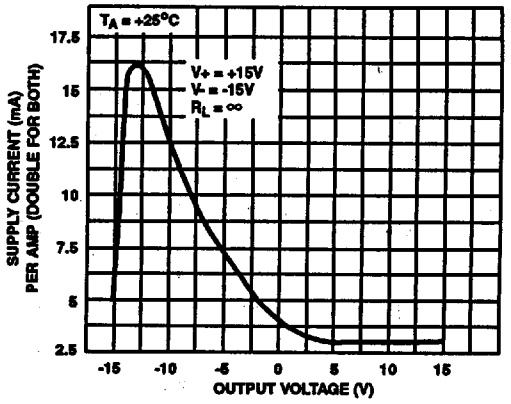


FIGURE 11. SUPPLY CURRENT vs OUTPUT VOLTAGE

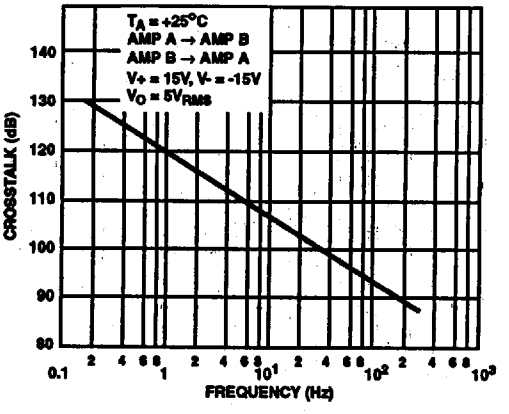


FIGURE 12. CROSSTALK vs FREQUENCY

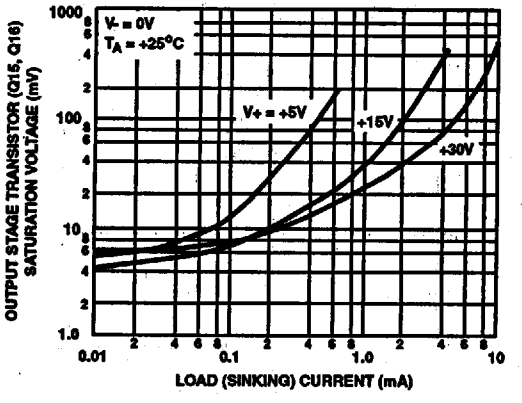


FIGURE 13. VOLTAGE ACROSS OUTPUT TRANSISTORS Q15 AND Q16 vs LOAD CURRENT

Typical Performance Curves (Continued)

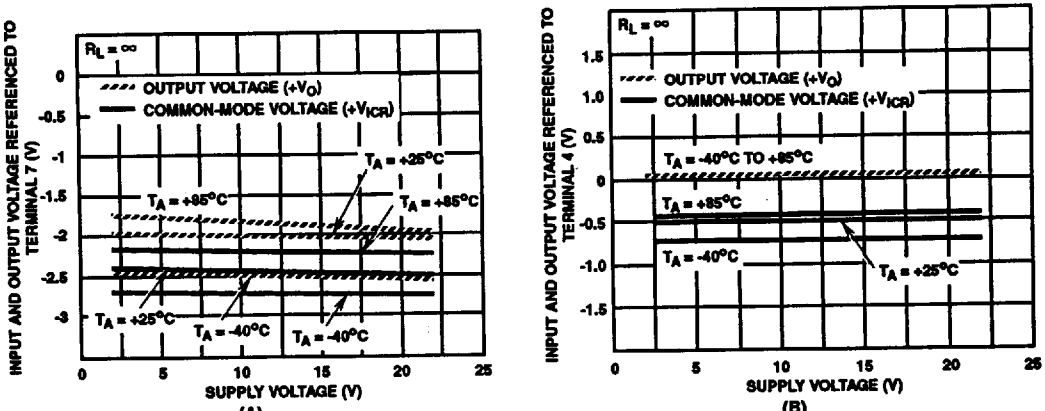
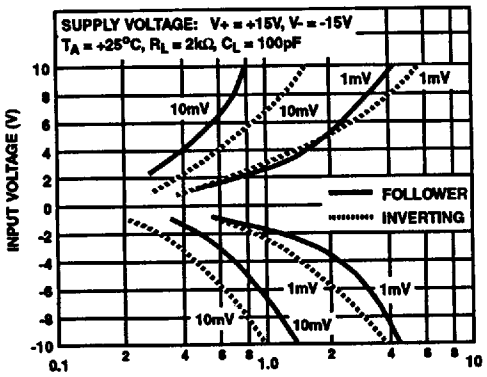
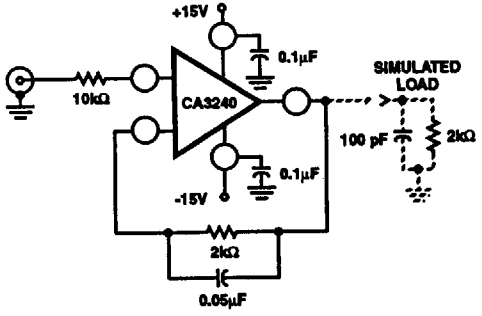


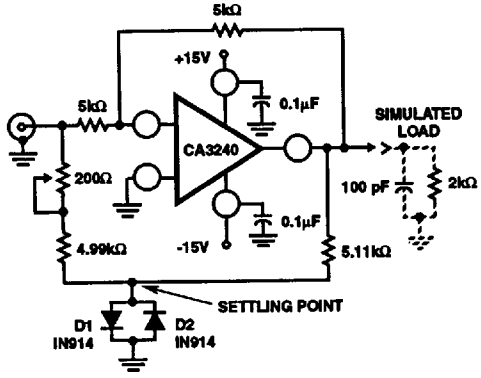
FIGURE 14. OUTPUT-VOLTAGE-SWING CAPABILITY AND COMMON MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE AND TEMPERATURE



(A) SETTLING TIME (μs)



(B) TEST CIRCUIT (FOLLOWER)



(C) TEST CIRCUIT (INVERTING)

FIGURE 15. INPUT VOLTAGE vs SETTLING TIME

Typical Performance Curves (Continued)

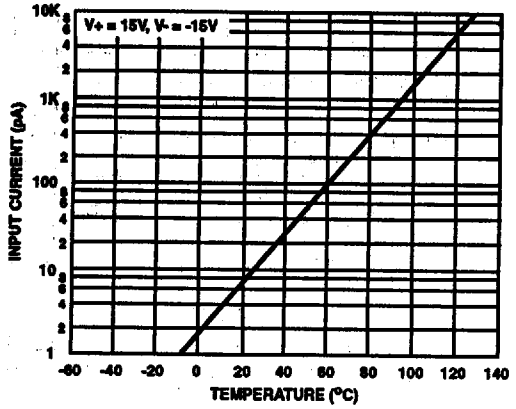


FIGURE 16. INPUT CURRENT vs AMBIENT TEMPERATURE

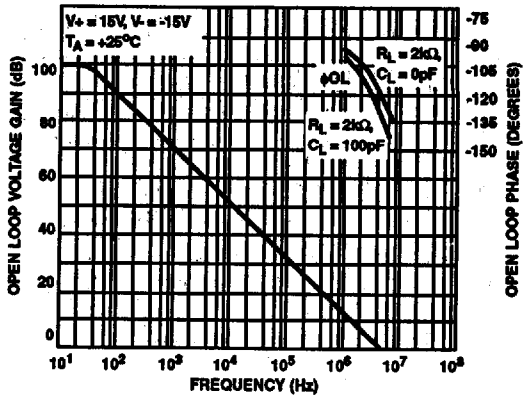
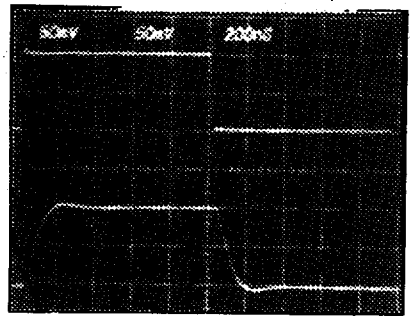


FIGURE 17. OPEN LOOP VOLTAGE GAIN AND PHASE vs FREQUENCY

Top Trace: Input
(50mV/Div.; 200ns/Div.)

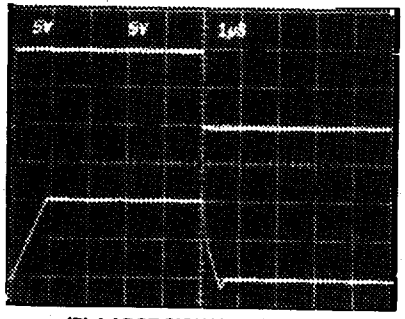
Bottom Trace: Output
(50mV/Div.; 200ns/Div.)



(A) SMALL SIGNAL RESPONSE

Top Trace: Input
(5V/Div.; 1µs/Div.)

Bottom Trace: Output
(5V/Div.; 1µs/Div.)



(B) LARGE SIGNAL RESPONSE

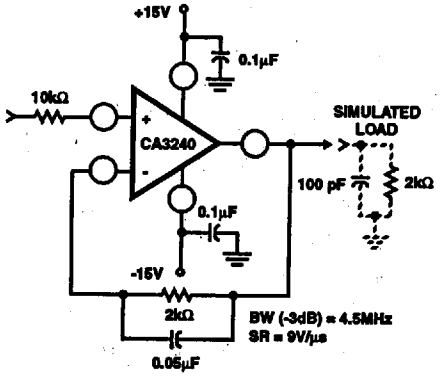


FIGURE 18. SPLIT-SUPPLY VOLTAGE FOLLOWER TEST CIRCUIT AND ASSOCIATED WAVEFORMS

Typical Performance Curves (Continued)

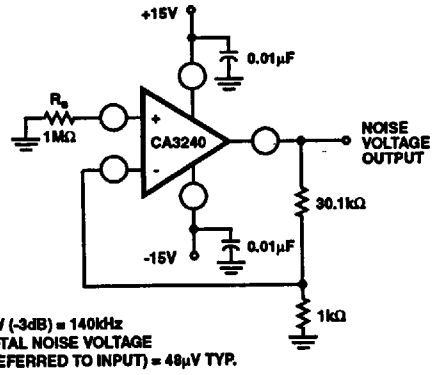


FIGURE 19. TEST CIRCUIT AMPLIFIER (30 dB GAIN) USED FOR WIDEBAND NOISE MEASUREMENT

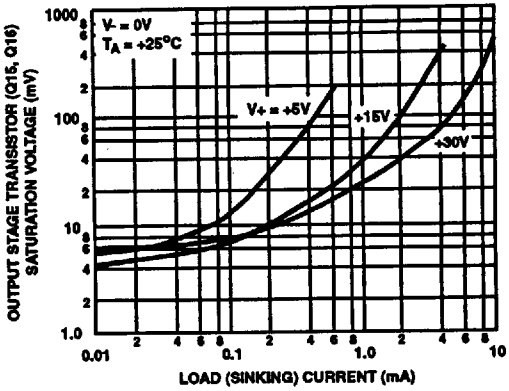


FIGURE 20. VOLTAGE ACROSS OUTPUT TRANSISTORS Q15 AND Q16 AS A FUNCTION OF LOAD CURRENT

Applications Considerations

Output Circuit Considerations

Figure 20 shows output current-sinking capabilities of the CA3240 at various supply voltages. Output voltage swing to the negative supply rail permits this device to operate both power transistors and thyristors directly without the need for level-shifting circuitry usually associated with the 741 series of operational amplifiers.

Figure 21 shows some typical configurations. Note that a series resistor, R_L, is used in both cases to limit the drive available to the driven device. Moreover, it is recommended that a series diode and shunt diode be used at the thyristor input to prevent large negative transient surges that can appear at the gate of thyristors, from damaging the integrated circuit.

Input Circuit Considerations

As indicated by the typical V_{ICR}, this device will accept inputs as low as 0.5V below V-. However, a series current-limiting resistor is recommended to limit the maximum input terminal current to less than 1mA to prevent damage to the input protection circuitry.

Moreover, some current-limiting resistance should be provided between the inverting input and the output when the CA3240 is used as a unity-gain voltage follower. This resistance prevents the possibility of extremely large input-signal transients from forcing a signal through the input-protection network and directly driving the internal constant-current source which could result in positive feedback via the output terminal. A 3.9kΩ resistor is sufficient.

The typical input current is in the order of 10pA when the inputs are centered at nominal device dissipation. As the output supplies load current, device dissipation will increase, rasing the chip temperature and resulting in increased input current. Figure 22 shows typical input-terminal current versus ambient temperature for the CA3240.

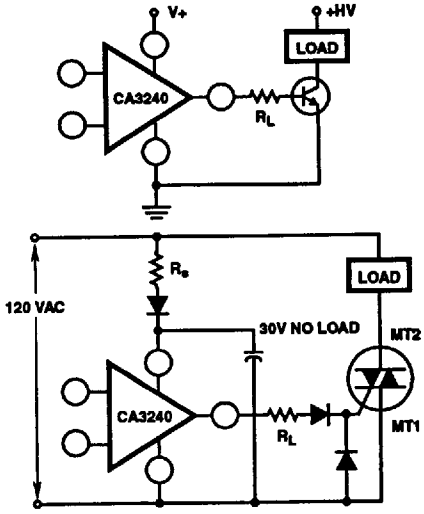


FIGURE 21. METHODS OF UTILIZING THE $V_{CE(SAT)}$ SINKING CURRENT CAPABILITY OF THE CA3240 SERIES

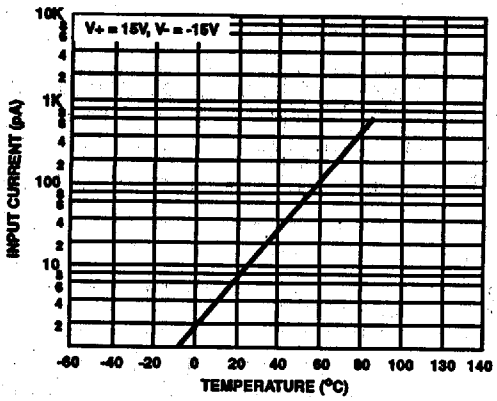


FIGURE 22. INPUT CURRENT vs AMBIENT TEMPERATURE

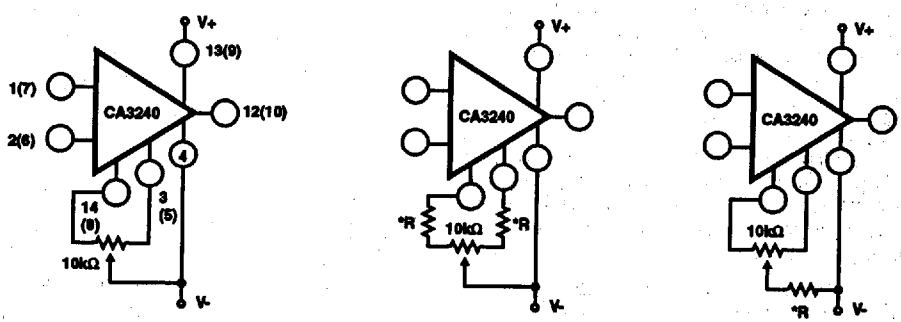
It is well known that MOSFET devices can exhibit slight changes in characteristics (for example, small changes in input offset voltage) due to the application of large differential input voltages that are sustained over long periods at elevated temperatures.

Both applied voltage and temperature accelerate these changes. The process is reversible and offset voltage shifts of the opposite polarity reverse the offset. In typical linear applications, where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage.

Offset-Voltage Nulling

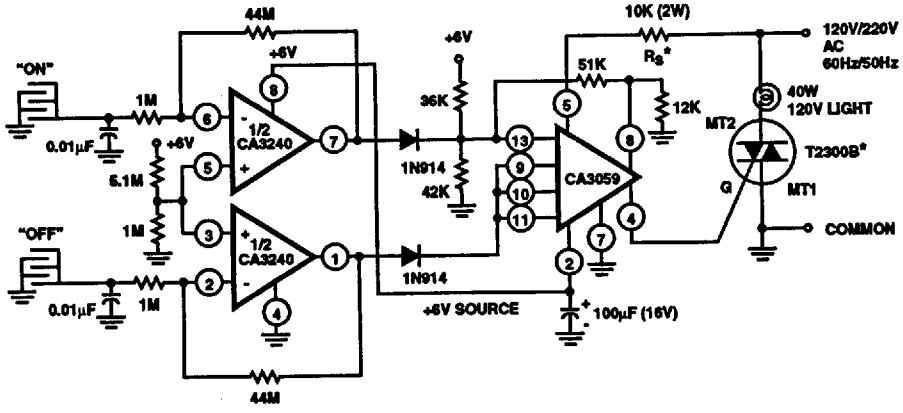
The input-offset voltage of the CA3240AE1 and CA3240E1 can be nulled by connecting a 10kΩ potentiometer between Terminals 3 and 14 or 5 and 8 and returning its wiper arm to Terminal 4, see Figure 23A. This technique, however, gives more adjustment range than required and therefore, a considerable portion of the potentiometer rotation is not fully utilized. Typical values of series resistors that may be placed at either end of the potentiometer, see Figure 23B, to optimize its utilization range are given in the table "Electrical Specifications for Equipment Design" shown on third page of this data sheet.

An alternate system is shown in Figure 23C. This circuit uses only one additional resistor of approximately the value shown in the table. For potentiometers, in which the resistance does not drop to zero ohms at either end of rotation, a value of resistance 10% lower than the values shown in the table should be used.



*See Electrical Specifications Table on third page of this data sheet for value of R.

FIGURE 23. THREE OFFSET-VOLTAGE NULLING METHODS, (CA3240AE1, CA3240E1 ONLY.)



* AT 220V OPERATION, TRIAC SHOULD BE T2300D, R_S = 18K, 5W

FIGURE 24. ON/OFF TOUCH SWITCH

Typical Applications

On/Off Touch Switch

The on/off touch switch shown in Figure 24 uses the CA3240E to sense small currents flowing between two contact points on a touch plate consisting of a PC board metallization "grid". When the "on" plate is touched, current flows between the two halves of the grid causing a positive shift in the output voltage (Terminal 7) of the CA3240E. These positive transitions are fed into the CA3059, which is used as a latching circuit and zero-crossing triac driver. When a positive pulse occurs at Terminal 7 of the CA3240E, the triac is turned on and held on by the CA3059 and its associated positive feedback circuitry (51kΩ resistor and 36kΩ/42kΩ voltage divider). When the positive pulse occurs at Terminal 1 (CA3240E), the triac is turned off and held off in a similar manner. Note that power for the CA3240E is supplied by the CA3059 internal power supply.

The advantage of using the CA3240E in this circuit is that it can sense the small currents associated with skin conduction while allowing sufficiently high circuit impedance to provide protection against electrical shock.

Dual Level Detector (Window Comparator)

Figure 25 illustrates a simple dual liquid level detector using the CA3240E as the sensing amplifier. This circuit operates on the principle that most liquids contain enough ions in solution to sustain a small amount of current flow between two electrodes submersed in the liquid. The current, induced by an 0.5V potential applied between two halves of a PC board grid, is converted to a voltage level by the CA3240E in a circuit similar to that of the on/off touch switch shown in Figure 24. The changes in voltage for both the upper and lower level sensors are processed by the CA3140 to activate an LED whenever the liquid level is above the upper sensor or below the lower sensor.

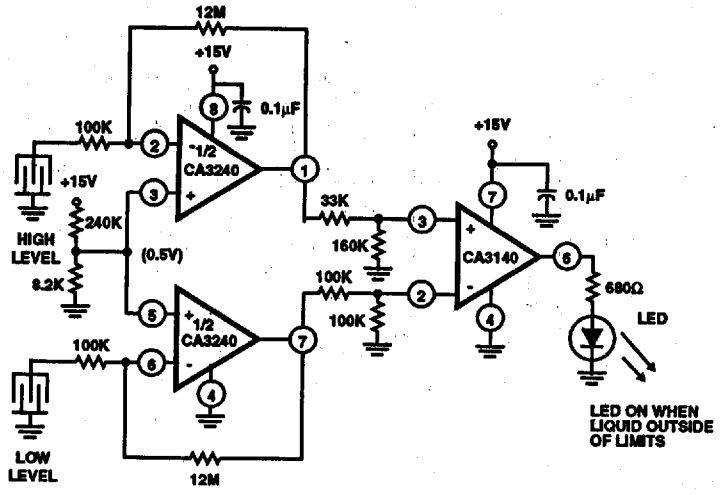


FIGURE 25. DUAL LEVEL DETECTOR

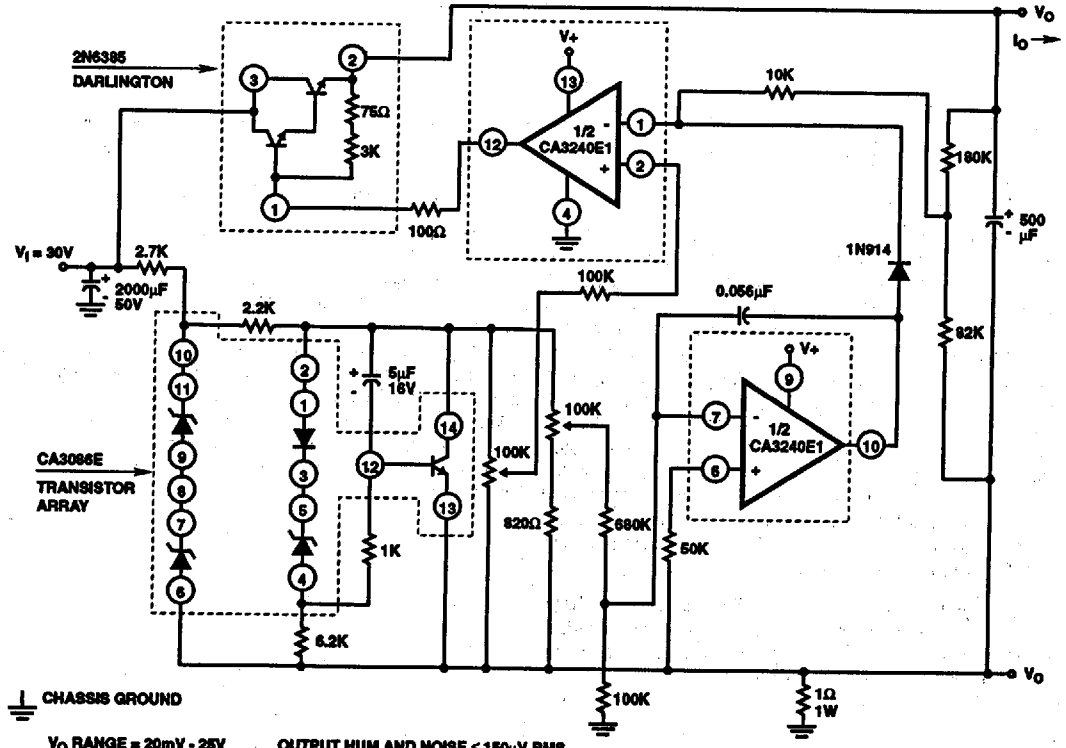


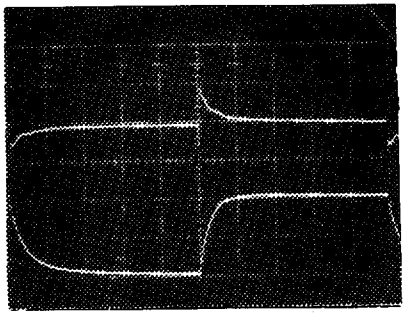
FIGURE 26. CONSTANT-VOLTAGE/CONSTANT-CURRENT POWER SUPPLY

Constant-Voltage/Constant-Current Power Supply

The constant-voltage/constant-current power supply shown in Figure 26 uses the CA3240E1 as a voltage-error and current-sensing amplifier. The CA3240E1 is ideal for this application because its input common-mode voltage range includes ground, allowing the supply to adjust from 20mV to 25V without requiring a negative supply voltage. Also, the ground reference capability of the CA3240E1 allows it to sense the voltage across the 1Ω current-sensing resistor in the negative output lead of the power supply. The CA3086 transistor array functions as a reference for both constant-voltage and constant-current limiting. The 2N6385 power Darlington is used as the pass element and may be required to dissipate as much as 40W. Figure 27 shows the transient response of the supply during a 100mA to 1A load transition.

Precision Differential Amplifier

Figure 28 shows the CA3240E in the classical precision differential amplifier circuit. The CA3240E is ideally suited for biomedical applications because of its extremely high input impedance. To insure patient safety, an extremely high electrode series resistance is required to limit any current that might result in patient discomfort in the event of a fault condition. In this case, 10MΩ resistors have been used to limit the current to less than 2μA without affecting the performance of the circuit. Figure 29 shows a typical electrocardiogram waveform obtained with this circuit.



Top Trace: Output Voltage
(500mV/Div. and 5μs/Div.)

Bottom Trace: Collector Of Load Switching Transistor
Load = 100mA to 1A, (5V/Div. and 5μs/Div.)

FIGURE 27. TRANSIENT RESPONSE

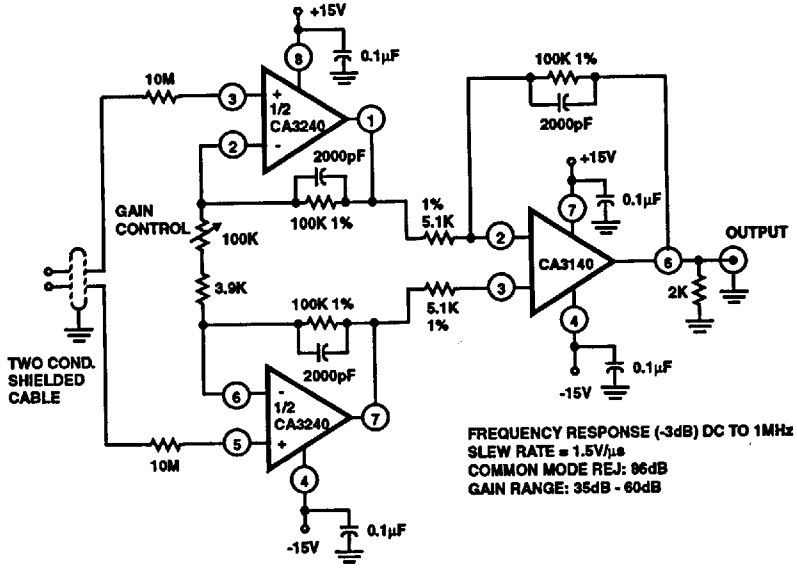
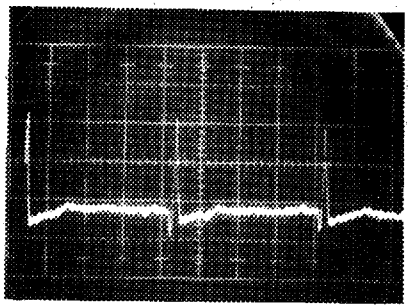


FIGURE 28. PRECISION DIFFERENTIAL AMPLIFIER



Vertical: 1.0mV/Div
(Amplifier Gain = 100X)
(Scope Sensitivity = 0.1V/Div.)

Horizontal: > 0.2 Sec/Div. (Uncal)

FIGURE 29. TYPICAL ELECTROCARDIOGRAM WAVEFORM

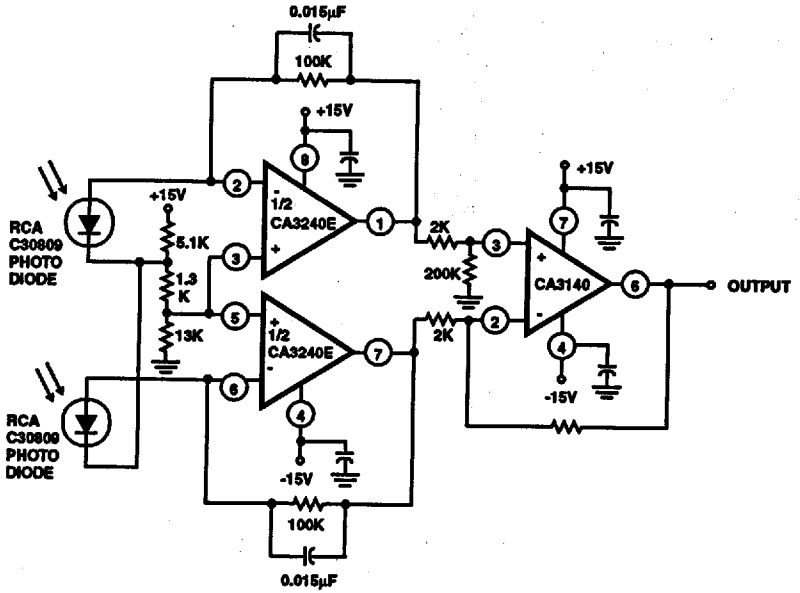


FIGURE 30. DIFFERENTIAL LIGHT DETECTOR

Differential Light Detector

In the circuit shown in Figure 30, the CA3240E converts the current from two photo diodes to voltage, and applies 1V of reverse bias to the diodes. The voltages from the CA3240E outputs are subtracted in the second stage (CA3140) so that only the difference is amplified. In this manner, the circuit can be used over a wide range of ambient light conditions without circuit component adjustment. Also, when used with a light source, the circuit will not be sensitive to changes in light level as the source ages.