

December 1996

Fast CMOS Bus Interface Registers

Features

- Advanced 0.8 micron CMOS Technology
- These Devices are Pin Compatible with Bipolar FAST™ Series at a Higher Speed and Lower Power Consumption
- 25Ω Series Resistor on All Outputs (CD74FCT2821T, CD74FCT2823T Only)
- TTL Input and Output Levels
- Low Ground Bounce Outputs
- Extremely Low Static Power
- Hysteresis on All Inputs

Description

The CD74FCT821T and CD74FCT2821T are 10-bit wide registers designed with ten D-type flip-flops with a buffered common clock and buffered three-state outputs. The CD74FCT823T and CD74FCT2823T are 9-bit wide registers designed with Clock Enable and Clear. The CD74FCT825T is an 8-bit wide register with all CD74FCT823T controls plus multiple enables. When output enable (OE) is LOW, the outputs are enabled. When OE is HIGH, the outputs are in the high impedance state. Input data meeting the setup and hold time requirements of the D inputs is transferred to the Y outputs on the LOW-to-HIGH transition of the clock input.

The CD74FCT2821T and CD74FCT2823T devices have a built-in 25Ω series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

Ordering Information

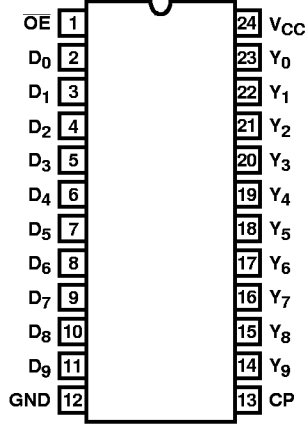
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT821ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT821ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT821BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT821BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT821CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT821CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT823ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT823ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT823BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT823BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT823CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT823CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT825ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT825ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT825BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT825BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT825CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT825CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2821ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2821ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2821BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2821BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2823ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2823ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2823BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2823BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2823CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2823CTQM	-40 to 85	24 Ld QSOP	M24.15-P

NOTE: QSOP is commonly known as SSOP.

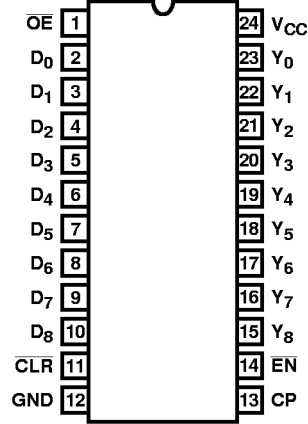
When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinouts

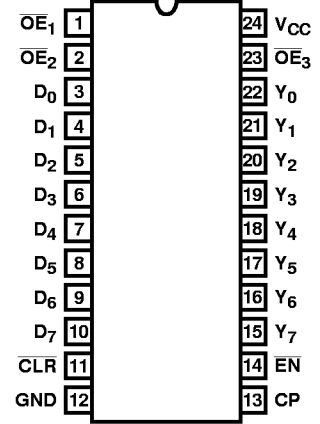
CD74FCT821T, CD74FCT2821T
(QSOP, SOIC)
TOP VIEW



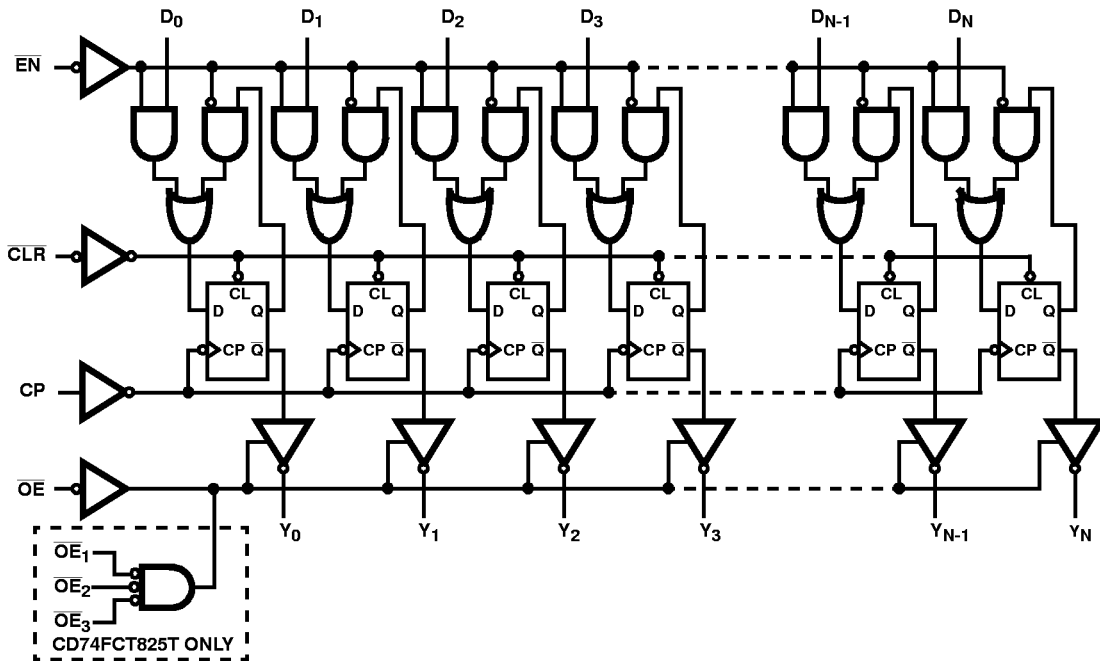
CD74FCT823, CD74FCT2823T
(QSOP, SOIC)
TOP VIEW



CD74FCT825T
(QSOP, SOIC)
TOP VIEW



Functional Block Diagram



CD74FCT821T, CD74FCT823T, CD74FCT825T, CD74FCT2821T, CD74FCT2823T

TRUTH TABLE (NOTE 1)

FUNCTION	INPUTS					OUTPUTS	INTERNAL
	CLR	EN	OE	CP	D _N	Y _N	Q _N
High-Z	H	L	H	↑	L	Z	L
	H	L	H	↑	H	Z	H
Clear	L	X	H	X	X	Z	L
	L	X	L	X	X	L	L
Hold	H	H	H	X	X	Z	NC
	H	H	L	X	X	NC	NC
Load	H	L	H	↑	L	Z	L
	H	L	H	↑	H	Z	H
	H	L	L	↑	L	L	L
	H	L	L	↑	H	H	H

NOTE:

1. H = High Voltage Level
 L = Low Voltage Level
 X = Don't Care
 Z = High Impedance
 NC = No Change
 ↑ = LOW-to-HIGH transition

Pin Descriptions

PIN NAME	DESCRIPTION
\overline{OE}	Output Enable Input (Active LOW)
CP	Clock Pulse for the register. Enters data on LOW-to-HIGH transition
D _N	Data Inputs
Y _N	Three-State Outputs
\overline{CLR}	Clear Input (Active LOW) (823/825/2823 Only)
EN	Clock Enable Input (Active LOW)
GND	Ground
V _{CC}	Power

CD74FCT821T, CD74FCT823T, CD74FCT825T, CD74FCT2821T, CD74FCT2823T

Absolute Maximum Ratings

DC Input Voltage -0.5V to 7.0V
 DC Output Current 120mA

Operating Conditions

Operating Temperature Range -40°C to 85°C
 Supply Voltage to Ground Potential
 Inputs and V_{CC} Only -0.5V to 7.0V
 Supply Voltage to Ground Potential
 Outputs and D/O Only -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W)
 SOIC Package 75
 QSOP Package 100
 Maximum Junction Temperature 150°C
 Maximum Storage Temperature Range -65°C to 150°C
 Maximum Lead Temperature (Soldering 10s) 300°C
 (Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETERS	SYMBOL	(NOTE 3)		MIN	(NOTE 4)	MAX	UNITS
		TEST CONDITIONS			TYP		
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T _A = -40°C to 85°C, V _{CC} = 5.0V ± 5%							
Output HIGH Voltage	V _{OH}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V _{OL}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OL} = 48mA	-	0.3	0.50	V
Output LOW Voltage	V _{OL}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OL} = 12mA (25Ω series)	-	0.3	0.50	V
Input HIGH Voltage	V _{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V _{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I _{IH}	V _{CC} = Max	V _{IN} = V _{CC}	-	-	1	μA
Input LOW Current	I _{IL}	V _{CC} = Max	V _{IN} = GND	-	-	-1	μA
High Impedance Output Current	I _{OZH} , I _{OZL}	V _{CC} = Max	V _{OUT} = 2.7V			1	μA
			V _{OUT} = 0.5V			-1	μA
Clamp Diode Voltage	V _{IK}	V _{CC} = Min, I _{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I _{OS}	V _{CC} = Max (Note 5), V _{OUT} = GND		-60	-120	-	mA
Power Down Disable	I _{OFF}	V _{CC} = GND, V _{OUT} = 4.5V		-	-	100	μA
Input Hysteresis	V _H			-	200	-	mV
CAPACITANCE T _A = 25°C, f = 1MHz							
Input Capacitance (Note 6)	C _{IN}	V _{IN} = 0V		-	6	10	pF
Output Capacitance (Note 6)	C _{OUT}	V _{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I _{CC}	V _{CC} = Max	V _{IN} = GND or V _{CC}	-	0.1	500	μA
Supply Current per Input at TTL HIGH	ΔI _{CC}	V _{CC} = Max	V _{IN} = 3.4V (Note 7)	-	0.5	2.0	mA
Supply Current per Input per MHz (Note 8)	I _{CCD}	V _{CC} = Max, Outputs Open OE = EN = GND One Input Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	-	0.15	0.25	mA/ MHz

CD74FCT821T, CD74FCT823T, CD74FCT825T, CD74FCT2821T, CD74FCT2823T

Electrical Specifications (Continued)

PARAMETERS	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4)	MAX	UNITS
					TYP		
Total Power Supply Current (Note 10)	I _{CC}	V _{CC} = Max, Outputs Open f _{CP} = 10MHz, 50% Duty Cycle OE = EN = GND f _I = 5MHz One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND	-	1.5	3.5 (Note 9)	mA
			V _{IN} = 3.4V V _{IN} = GND	-	2.0	5.5 (Note 9)	mA
		V _{CC} = Max, Outputs Open f _{CP} = 10MHz, 50% Duty Cycle OE = EN = GND Eight Bits Toggling f _I = 2.5MHz 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	-	3.8	7.3 (Note 9)	mA
			V _{IN} = 3.4V V _{IN} = GND	-	6.0	16.3 (Note 9)	mA

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	AT		BT		CT (NOTE 14)		UNIT
			(NOTE 12) MIN	MAX	(NOTE 12) MIN	MAX	(NOTE 12) MIN	MAX	
CD74FCT821T, CD74FCT2821T									
Propagation Delay CP to Y _N (OE = LOW)	t _{PLH} , t _{PHL}	C _L = 50pF R _L = 500Ω	1.5	10.0	1.5	7.5	1.5	6.0	ns
		C _L = 300pF (Note 13) R _L = 500Ω	1.5	20.0	1.5	15.0	1.5	12.5	ns
Setup Time HIGH or LOW, D _N to CP	t _{SU}	C _L = 50pF R _L = 500Ω	4.0	-	3.0	-	3.0	-	ns
Hold Time HIGH or LOW, D _N to CP	t _H		2.0	-	1.5	-	1.5	-	ns
Setup Time HIGH or LOW, EN to CP	t _{SU}		4.0	-	3.0	-	3.0	-	ns
Hold Time HIGH or LOW, EN to CP	t _H		2.0	-	0	-	0	-	ns
Propagation Delay CLR to Y _N	t _{PHL}		1.5	14.0	1.5	9.0	1.5	8.0	ns
Recovery Time, CLR to CP (Note 13)	t _{REM}		6.0	-	6.0	-	6.0	-	ns
Clock Pulse Width HIGH or LOW (Note 13)	t _W		7.0	-	5.0	-	6.0	-	ns
CLR Pulse Width LOW (Note 13)	t _W		6.0	-	6.0	-	6.0	-	ns
Output Enable Time OE to Y _N	t _{PZH}	C _L = 50pF R _L = 500Ω	1.5	11.5	1.5	8.0	1.5	7.0	ns
	t _{PZL}	C _L = 300pF (Note 13) R _L = 500Ω	1.5	23.0	1.5	15.0	1.5	12.5	ns
Output Disable Time OE to Y _N	t _{PHZ}	C _L = 50pF R _L = 500Ω	1.5	7.0	1.5	6.5	1.5	6.2	ns
	t _{PLZ}	C _L = 300pF (Note 13) R _L = 500Ω	1.5	8.0	1.5	7.5	1.5	6.5	ns
CD74FCT823T, CD74FCT2823T, CD74FCT825T									
Propagation Delay CP to Y _N (OE = LOW)	t _{PLH} , t _{PHL}	C _L = 50pF R _L = 500Ω	1.5	10.0	1.5	7.5	1.5	6.0	ns
		C _L = 300pF (Note 13) R _L = 500Ω	1.5	20.0	1.5	15.0	1.5	12.5	ns

CD74FCT821T, CD74FCT823T, CD74FCT825T, CD74FCT2821T, CD74FCT2823T

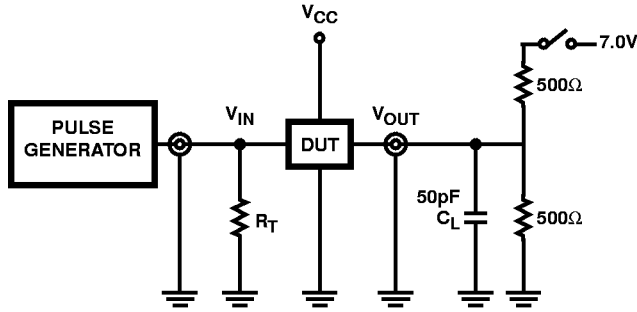
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	AT		BT		CT (NOTE 14)		UNIT
			(NOTE 12) MIN	MAX	(NOTE 12) MIN	MAX	(NOTE 12) MIN	MAX	
Setup Time HIGH or LOW, D _N to CP	t _{SU}	C _L = 50pF R _L = 500Ω	4.0	-	3.0	-	3.0	-	ns
Hold Time HIGH or LOW, D _N to CP	t _H		2.0	-	1.5	-	1.5	-	ns
Setup Time HIGH or LOW, $\overline{E_N}$ to CP	t _{SU}		4.0	-	3.0	-	3.0	-	ns
Hold Time HIGH or LOW, $\overline{E_N}$ to CP	t _H		2.0	-	0	-	0	-	ns
Propagation Delay CLR to Y _N	t _{PHL}		1.5	13.0	1.5	9.0	1.5	8.0	ns
Recovery Time, \overline{CLR} to CP (Note 13)	t _{REM}		6.0	-	6.0	-	6.0	-	ns
Clock Pulse Width HIGH or LOW (Note 13)	t _W		7.0	-	5.0	-	6.0	-	ns
CLR Pulse Width LOW (Note 13)	t _W		6.0	-	6.0	-	6.0	-	ns
Output Enable Time OE to Y _N	t _{PZH}	C _L = 50pF R _L = 500Ω	1.5	11.5	1.5	8.0	1.5	7.0	ns
	t _{PZL}	C _L = 300pF (Note 13) R _L = 500Ω	1.5	23.0	1.5	15.0	1.5	12.5	ns
Output Disable Time \overline{OE} to Y _N	t _{PHZ}	C _L = 50pF R _L = 500Ω	1.5	7.0	1.5	6.5	1.5	6.2	ns
	t _{PLZ}	C _L = 300pF (Note 13) R _L = 500Ω	1.5	8.0	1.5	7.5	1.5	6.5	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Characteristics for the applicable device type.
4. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is determined by device characterization but is not production tested.
7. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
9. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
10. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input (V_{in} = 3.4V)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_I = Input Frequency
 N_I = Number of Inputs at f_I
 All currents are in milliamps and all frequencies are in megahertz.
11. See test circuit and wave forms.
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. This parameter is guaranteed but not production tested.
14. The CD74FCT2821CT type is not available.

Test Circuits and Waveforms



SWITCH POSITION	
TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
$t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}$	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.
 R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

15. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $Z_{OUT} \leq 50\Omega$;
 $t_f, t_r \leq 2.5\text{ns}$.

FIGURE 1. TEST CIRCUIT

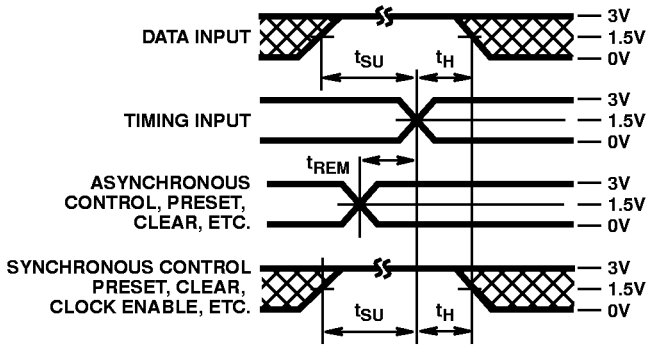


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

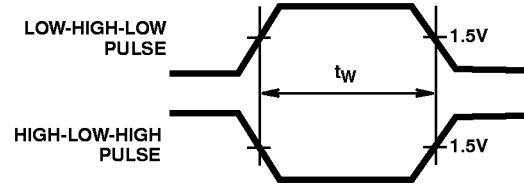


FIGURE 3. PULSE WIDTH

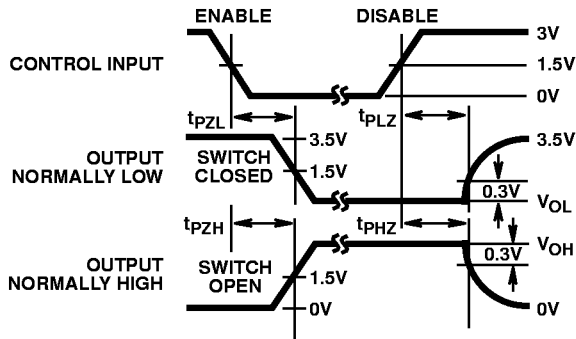


FIGURE 4. ENABLE AND DISABLE TIMING

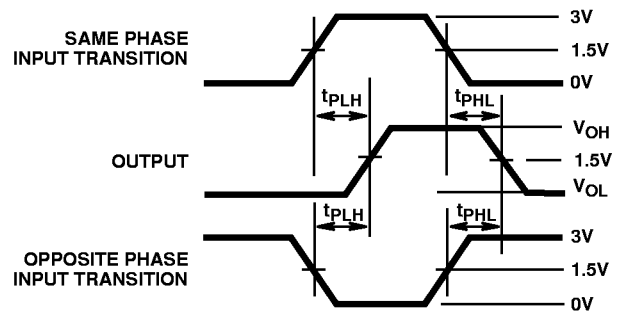
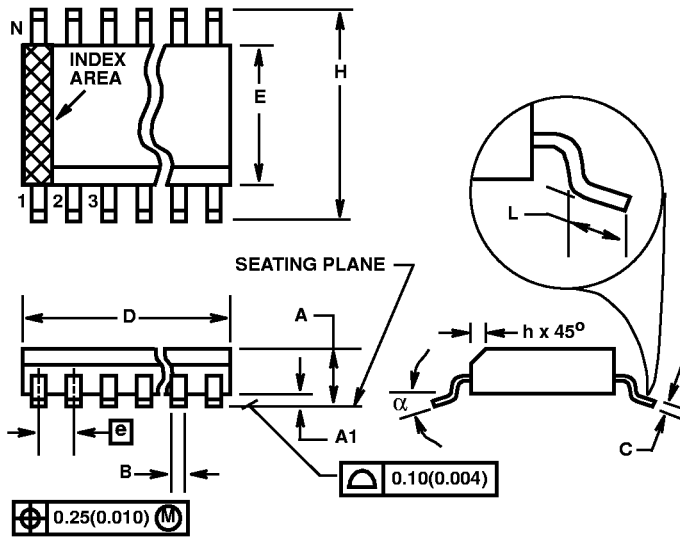


FIGURE 5. PROPAGATION DELAY

Small Outline Plastic Packages (SOIC)



NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs.
2. Dimension "E" does not include interlead flash or protrusions.
3. "L" is the length of terminal for soldering to a substrate.
4. "N" is the number of terminal positions.
5. Terminal numbers are shown for reference only.
6. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

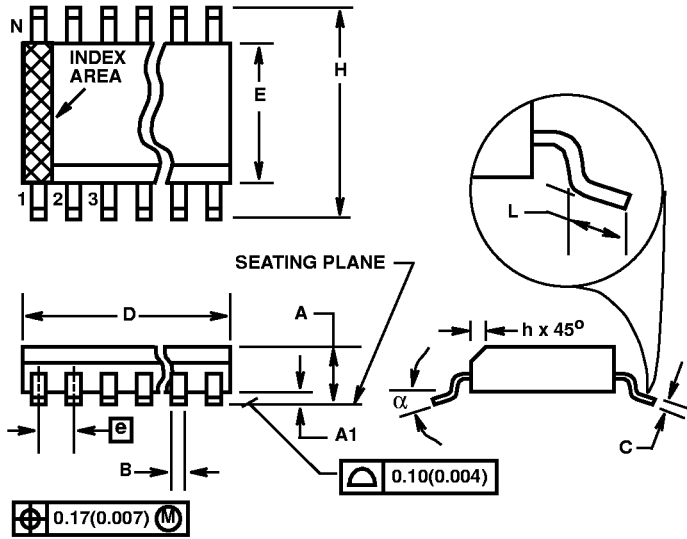
M24.3-P

24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.092	0.105	2.34	2.67	-
A1	0.004	0.012	0.102	0.302	-
B	0.013	0.020	0.330	0.508	-
C	0.009	0.011	0.229	0.279	-
D	0.598	0.614	15.19	15.60	1
E	0.291	0.299	7.39	7.59	2
e	0.050 BSC		1.27 BSC		-
H	0.401	0.411	10.18	10.44	-
h	0.010	0.029	0.254	0.737	-
L	0.016	0.050	0.41	1.27	3
N	24		24		4
α	0°	8°	0°	8°	-

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Shrink Small Outline Plastic Packages (SSOP/QSOP)



M24.15-P
24 LEAD SHRINK NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.007	0.011	0.178	0.279	-
B	0.008	0.012	0.203	0.305	-
C	0.007	0.010	0.178	0.254	-
D	0.337	0.344	8.56	8.74	1
E	0.149	0.157	3.78	3.99	2
e	0.025 BSC		0.635 BSC		-
H	0.228	0.244	5.79	6.20	-
h	0.015		0.38		-
L	0.016	0.050	0.41	1.27	3
N	24		24		4
α	0°	8°	0°	8°	-

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs.
2. Dimension "E" does not include interlead flash or protrusions.
3. "L" is the length of terminal for soldering to a substrate.
4. "N" is the number of terminal positions.
5. Terminal numbers are shown for reference only.
6. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

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