3 Channel 14- & 16-Bit Tracking Synchro/Resolver-to-Digital Converters





Models: SDC-14610, SDC-14615



The SDC-14610/15 Series are small low cost three channel Synchro- or Resolver-to-Digital (S/R-D) converters. The three channels are independent tracking types but share digital output pins and a common reference

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THREE CHANNEL 14- AND 16-BIT TRACKING S/R-D CONVERTERS SDC-14610/15 DATA SHEET

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Revision	Date	Pages	Description
Rev N	8/2017	All	Updated to new format, S option removed.

1 P	REFACE	1
1.1	Text Usage	1
1.2	Special Handling and Cautions	1
1.3	Trademarks	1
1.4	What is included in this manual?	1
1.5	Technical Support	2
2 C	OVERVIEW	3
2.1	Features	3
3 D	DETAILED ARCHITECTURE	8
3.1	Theory of Operation	8
3.2	Transfer Function and Bode Plot	8
~ ~		
3.3	General Setup Considerations	
3.3 3.4	General Setup Considerations Inhibit and Enable Timing	10 10
3.3 3.4 3.5	General Setup Considerations Inhibit and Enable Timing BIT , Built-In-Test (T option)	10 10 11
3.3 3.4 3.5 3.6	General Setup Considerations Inhibit and Enable Timing BIT , Built-In-Test (T option) No False 180° Hangup	10 10 11 11
3.3 3.4 3.5 3.6 3.7	General Setup Considerations Inhibit and Enable Timing BIT , Built-In-Test (T option) No False 180° Hangup Pinout	10 10 11 11 11

Figure 1.	SDC-14610/15 Synchro/Resolver-to-Digital Converter	4
Figure 2.	SDC-14610/15 Block Diagram	4
Figure 3.	Bode Plots	9
Figure 4.	Inhibit Timing	10
Figure 5.	Enable Timing	11
Figure 6.	SDC-14610/15 Mechanical Outline	13

Table 1. DSC-14610/15 Specification Table	5
Table 2. Pinouts (36 Pin)	12
Table 3. Standard DDC Processing for Hybrid and Monolithic Hermetic Products	15

1 PREFACE

This data sheet uses typographical conventions to assist the reader in understanding the content. This section will define the text formatting used in the rest of the data sheet.

1.1 Text Usage

- **BOLD**-indicates important information.
- Courier New-indicates code examples.
- <...> indicates user-entered text or commands.

1.2 Special Handling and Cautions

The DSC-14610/15 uses state-of-the-art components, and proper care should be used to ensure that the device will not be damaged by Electrical Static Discharge (ESD), physical shock, or improper power surges and that precautions are taken to avoid electrocution.



Warnings: Turn off power to the computer hardware and unplug from wall.

NEVER insert or remove card with power turned on.

Ensure that standard ESD precautions are followed. As a minimum, one hand should be grounded to the power supply in order to equalize the static potential.

Do not store disks in environments exposed to excessive heat, magnetic fields or radiation.

1.3 Trademarks

All trademarks are the property of their respective owners.

1.4 What is included in this manual?

This data sheet contains a complete description of hardware installation and use.

1.5 Technical Support

In the event that problems arise beyond the scope of this manual, you can contact DDC by the following:

US Toll Free Technical Support: 1-800-DDC-5757, ext. 7771

Outside of the US Technical Support: 1-631-567-5600, ext. 7771

Fax: 1-631-567-5758 to the attention of SYNCHRO Applications

DDC Website: www.ddc-web.com/ContactUs/TechSupport.aspx

Please note that the latest revisions of Software and Documentation are available for download at DDC's Web Site, <u>www.ddc-web.com</u>.

2 OVERVIEW

The SDC-14610/15 Series are small low cost three channel Synchro- or Resolver-to-Digital (S/R-D) converters. The SDC-14610 Series are fixed at 14 bits, the SDC-14615 at 16 bits. The three channels are independent tracking types but share digital output pins and a common reference.

The Velocity Output (VEL) from the SDC-14610/15 Series, which can be used to replace a tachometer, is a 4V signal referenced to ground with a linearity of 1% of output voltage.

A BIT output is optional and is a logic line that indicates LOS (Loss Of Signal) or excessive converter error. Due to pin limitations this option will exclude the velocity output. (See option "T".)

SDC-14610/15 Series converters are available with operating temperature ranges of 0°C to +70°C and -55°C to +125°C, and MIL-PRF-38534 processing is available.

2.1 Features

- Fixed 14- or 16-Bit resolution
- Small size 36-Pin DDIP package
- Three independent converters
- Low cost per channel
- Velocity output eliminates tachometers
- Optional BIT output (LOS)
- High reliabaility single chip monolithic
- -55°C to +125°C operating temperature range
- MIL-PRF-38534 processing available



Figure 1. SDC-14610/15 Synchro/Resolver-to-Digital Converter





PARAMETER	VALUE		UNITS
RESOLUTION	14	16	Bits
ACCURACY	4 +1 LSB	2 or 4 +1 LSB	Min
REPEATABILITY	1 m	ax	LSB
DIFFERENTIAL LINEARITY	1 m	ax	LSB
REFERNCE INPUT			
Туре	Common to all channels, Differential		
	2 & 11.8V Units	90V Unit	
Voltage Range	2 – 35	10 – 130	Vrms
Frequency	360 – 5000	see note 1	Hz
Input Impedance			
Single Ended	60k	270k min	Ω
Differential	120k	540k min	Ω
Common-Mode Range	50	200, 300 transient	Vpeak
SIGNAL INPUT CHARACTERISTICS	EACH CHANNEL		
90V Synchro Input (L-L)			
Zin line-to-line	123k		Ω
Zin line-to-ground	80k		Ω
Common-Mode Voltage	180 max		V
11.8V Synchro Input (L-L)			
Zin line-to-line	52	52k	
Zin line-to-ground	34k		Ω
Common-Mode Voltage	30 n	30 max	
11.8V Resolver Input (L-L)			
Zin line-to-line	140	140k	
Zin line-to-ground	70k		Ω
Common-Mode Voltage	30 max		V
2V Direct Input (L-L)			
Voltage Range	2 nom, 2	2 nom, 2.3 max	
Max Voltage No Damage	25 cont, 100	25 cont, 100pk transient	
Input Impedance	20 M // 1	0pF min	Ω
DIGITAL INPUT/OUTPUT			
Logic Type	TTL/CMOS compatibl	е	
Inputs	Logic 0 = 0.8V max		
	Logic $1 = 2.0$ V min		

Table 1. DSC-14610/15 Specification Table					
These specs apply over the rated power supply, temperature, and reference frequency ranges; 10% signal amplitude variation, and 10% harmonic distortion. (Values are for each channel unless stated otherwise.					
PARAMETER	PARAMETER VALUE				UNITS
DIGITAL INPUT/OUTPUT (con't)					
	Loading	(per channel) = 10 µA		
	max P.U. current source to +5V // 5pF max				
	CMOS transient protected				
Inhibit (INH.) (common)	EACH C	EACH CHANNEL			
	Logic 0 ir	nhibits; Data	stable withir	n 0.5µs	
Enables Bits 1 to 8 (EM.)	Logic 0 e	nables; Data	a stable with	in 150ns	
Enables Bits 9 to 14 (16) (EL)	Logic 1 =	High Impen	dance		
	Data Hig	h Z within 10	0ns		
DIGITAL OUTPUT	СОММО	N TO ALL C	HANNELS		
Parallel Data [1 – 14 (16)]	8 parallel positive l	8 parallel lines; 2 bytes natural binary angle, positive logic			bits
Built-In-Test (BIT.) (optional)	Logic 0 = BIT condition \pm LSBs of error with a filter of 500µs or LOS				
	EACH CHANNEL				
	50				pF
Drive Capability	Logic 0;	1 TTL loads;	-0.4mA at 2	.8V min	TTL
	Logic 0; 100mV max driving			TTL	
	Logic 1; +5V supply minus 100mV min driving			CMOS	
DYNAMIC CHARATERISTICS	DEVICE TYPE				
Each Channel	60Hz 400Hz)Hz		
Input Frequency	47	47-5k		360-5k	
Bandwidth (Closed Loop)	1	5	103		Hz
Ка	830		53k		1/s²
A1	0.17		1.33		1/s
A2	5k		40k		1/s
А	29		230		1/s
В	14.5 115		1/s		
Resolution	14	16	14	16	bits
Tracking Rate					
Typical	1.25	0.31	10	2.5	rps
Minimum	1	0.25	8	2	rps
Acceleration (1LSB lag)	18	4.5	1160	290	deg/s²
Setting Time (179° step max)	1100 2500 140 320		320	msec	

Table 1. DSC-14610/15 Specification Table These specs apply over the rated power supply, temperature, and reference frequency ranges; 10% signal amplitude variation, and 10% harmonic distortion. (Values are for each channel unless stated otherwise.)				
PARAMETER VALUE UNI				
VELOCITY CHARACTERISTICS	EACH CHANNEL			
Polarity	Positive for increasing angle			
Voltage Range (Full Scale)	4.5 typ	4 min	±V	
Scale Factor	10 typ	20 max	±%	
Scale Factor TC	100 typ	200 max	ppm/°C	
Reversal Error	1 typ	2 max	±%	
Linearity	0.5 typ	1 max	±%	
Zero Offset	5 typ	10 max	mV	
Zero Offset TC	15 typ	30 max	μV/°C	
Load		20 max	kΩ	
Noise	1 typ	2 max	(Vp/V)%	
POWER SUPPLIES	TOTAL DE	EVICE		
Nominal Voltage	+5	-5	V	
Voltage Range	5	10	±%	
Max Volt, w/o Damage	+7	-7	V	
Current (each supply)	36 typ, 51	mA		
TEMPERATURE RANGE				
Operating				
-30x	0 to +70			
-10x		°C		
Storage		°C		
Junction-to-case	55		°C/W	
JC Thermal Rise	+9 (note 2)		°C	
Junction Temperature max	140		°C	
PHYSICAL CHARACTERISTICS				
Size	1.70 x 0.78 x 0.21		in	
		43.2 x 19.8 x 5.3	mm	
Weight		0.66	oz	
	1.87			
 Table 1 Notes: 1. 47 - 5k for 90V, 60Hz; 360 - 5k for 90V, 400Hz. 2. Applied to operating.temperature. 				

3 DETAILED ARCHITECTURE

3.1 Theory of Operation

The SDC-14610/15 Series of converters are based upon a single chip CMOS custom monolithic. They are implemented using the latest IC technology which merges precision analog circuitry with digital logic to form a complete high performance tracking resolver-to-digital converter.

Figure 2 is the Functional Block Diagram of the SDC-14610/15 Series. The converter operates with \pm 5VDC power supplies. Analog signals are referenced to analog ground, which is at ground potential. The converter is made up of three main sections; an input front-end, a converter, and a digital interface. The converter front-end differs for synchro, resolver and direct inputs. An electronic Scott-T is used for synchro inputs, a resolver conditioner for resolver inputs and a sine and cosine voltage follower for direct inputs. These amplifiers feed the high accuracy Control Transformer (CT). Its other input is the 14-bit digital angle f. Its output is an analog error angle, or difference angle, between the two inputs. The CT performs the ratiometric trigonometric computation of SINqCOSf - COSqSINf = SIN(q - f) using amplifiers, switches, logic and capacitors in precision ratios.

The converter accuracy is limited by the precision of the computing elements in the CT. In these converters, ratioed capacitors are used in the CT instead of more conventional precision ratioed resistors. Capacitors used as computing elements with op-amps need to be sampled to eliminate voltage drifting. Therefore, the circuits are sampled at a high rate to eliminate this drifting and at the same time to cancel out the op-amp offsets.

The error processing is performed using the industry standard technique for type II tracking R/D converters. The DC error is integrated yielding a velocity voltage which, in turn, drives a voltage controlled oscillator (VCO). This VCO is an incremental integrator (constant voltage input to position rate output) which, together with the velocity integrator, forms a type II servo feedback loop. A lead in the frequency response is introduced to stabilize the loop and another lag at higher frequency is introduced to reduce the gain and ripple at the carrier frequency and above.

3.2 Transfer Function and Bode Plot

The dynamic performance of the converter can be determined from its functional block diagram and its Bode plots (open and closed loop); these are shown in Figure 3.

The open loop transfer function is as follows:

Open Loop Transfer Function = $\frac{A^2 \left(\frac{S}{B} + 1\right)}{1 + 1}$

$$\frac{1}{S^2 \left(\frac{S}{10B} + 1\right)}$$



The components of gain coefficient are error gradient, integrator gain, and VCO gain. These can be broken down as follows:

- Error Gradient = 0.011 volts per LSB (CT + Error Amp + Demod)
- Integrator Gain = $\frac{1}{R_i C_i}$ volts per second per volt
- VCO Gain = $\frac{1}{1.25 \text{ R}_{V} \text{ C}_{V}}$ LSBs per second per volt



Figure 3. Bode Plots

3.3 General Setup Considerations

The following recommendations should be considered when connecting the SDC-14610/15 Series converters:

- 1. Power supplies are ± 5 VDC. For lowest noise performance it is recommended that a 0.1 μ F or larger cap be connected from each supply to ground near the converter package.
- 2. Direct inputs are referenced to AGND.
- 3. Connect pin 5 (GND) to pin 6 (AGND) close to the hybrid.

3.4 Inhibit and Enable Timing

The Inhibit (INH) signal is used to freeze the digital output angle in the transparent output data latch while data is being transferred. Application of an Inhibit signal does not interfere with the continuous tracking of the converter. As shown in Figure 4, angular output data is valid 500 nanoseconds maximum after the application of the low-going inhibit pulse.

Output angle data is enabled onto the tri-state data bus in six bytes. The Enable MSB (<u>EM.</u>-A, <u>EM.</u>-B, or <u>EM.</u>-C) is used for the most significant 8 bits and Enable LSB (<u>EL.</u>-A, <u>EL.</u>-B, or <u>EL.</u>-C) is used for the least significant bits. As shown in Figure 5, output data is valid 150 nanoseconds maximum after the application of a low-going enable pulse. The tri-state data bus returns to the high impedance state 100

nanoseconds maximum after the rising edge of the enable signal.



Figure 4. Inhibit Timing



Figure 5. Enable Timing

3.5 BIT , Built-In-Test (T option)

This output is a logic line that will flag an internal fault condition, or LOS (Loss-Of-Signal). The internal fault detector monitors the internal error and, when it exceeds ± 100 LSBs, will set the line to a logic 0; this condition will occur during a large-step input and will reset to a logic 1 after the converter settles out. (The error voltage is filtered with a 500 µs filter). BIT, will set for an overvelocity condition because the converter loop can't maintain input/output sync. BIT, will also be set if a total LOS (loss of all signals) occurs.

3.6 No False 180° Hangup

This feature eliminates the "false 180° reading" during instantaneous 180° step changes; this condition most often occurs when the input is "electronically switched" from a digital-to-synchro converter. If the "MSB" (or 180° bit) is "toggled" on and off, a converter without the "false 180° reading" feature may fail to respond.

The condition is artificial, as a "real" synchro or resolver cannot change its output 180° instantaneously. The condition is most often noticed during wraparound verification tests, simulations, or troubleshooting.

3.7 Pinout

Table 2. Pinouts (36 Pin)					
	Description				
Pin	Synchro	Resolver	Direct (note 5)	Pin	Description
1	S1A	S1A	N.C.	19	EMC (Enable MSBs)
2	S2A	S2A	+COSA	20	EL -C (Enable LSBs)
3	S3A	S3A	+SINA	21	VEL C (Velocity Output) (note 1)
4	N.C.	S4A	N.C.	22	Bit 1/Bit 9
5	GN	D (Ground) (no	te 3)	23	Bit 2/Bit 10
6	AGND (Analog Ground) (note 3)	24	Bit 3/Bit 11
7	S1B	S1B	N.C.	25	Bit 4/Bit 12
8	S2B	S2B	+COSB	26	Bit 5/Bit 13
9	S3B	S3B	+SINB	27	Bit 6/Bit 14
10	N.C.	S4B	N.C.	28	Bit 7/Bit 15 (note 2)
11	-5V (Power Supply)		29	Bit 8/Bit 16 (note 2)	
12	+5V (Power Supply)			30	EL -B (Enable LSBs)
13	S1C	S1C	N.C.	31	EMA (Enable MSBs)
14	S2C	S2C	+COSC	32	VEL B (Velocity Output) (note 1)
15	S3C	S3C	+SINC	33	. INH. (Inhibit)
16	N.C.	S4C	N.C.	34	EL -A (Enable LSBs)
17	-REF (-Refernce Input)		35	EMA (Enable MSBs)	
18	+REF (+Refernce Input)			36	VEL A (Velocity Output) (note 1)

Table 2 notes:

1. Replaced with BIT - T option

2. SDC-14615 Series only

3. Connect pin 5 (GND) to pin 6 (AGND) close to the hybrid

4. (MSB = Bit 1) (LSB = Bit 14 or 16 depending on resolution set)

5. Digital = 2V Resolver Direct



Notes:

1. Dimensions are in inches (millimeters).

2. Lead identification numbers are for reference only.

3. Lead clusters shall be centered withing ±0.01 of outline dimensions. Lead spacing dimensions. Lead spacing dimensions apply only at seating plane.

4. Pin material meets solderability requirements to MIL-STD-202E, Method 208C.

5. Case is electrically floating.

Figure 6. SDC-14610/15 Mechanical Outline

4 ORDERING INFORMATION



Notes:

- 1. Standard DDC Processing with burn-in and full temperature test see Table 3.
- 2. MIL-PRF-38534 product grading is designated with the following dash numbers:
 - Class H is a-11X, 13X, 14X, 15X, 41X, 43X, 44X, 45X Class G is a -21X, 23X, 24X, 25X, 51X, 53X, 54X, 55X Class D is a -31X, 33X, 34X, 35X, 81X, 83X, 84X, 85X
- 3. These products contain tin-lead solder finish as applicable to solder dip requirements. Contact factory for custom Flat-Pack requests.
- 4. Contact factory for 1 minute custom part requirements.

Table 3. Standard DDC Processing for Hybrid and Monolithic Hermetic Products				
TEST	MIL-STD-883			
TEST	Method(s)	Condition(s)		
Inspection	2009, 2010, 2017, and 2032	—		
Seal	1014	A and C		
Temperature Cycle	1010	С		
Constant Acceleration	2001	3000g		
Burn-in	1015 (note 1), 1030 (note 2)	Table 1		

Notes:

1. For process requirements "B" (refer to ordering information), devices may be non-compliant with MIL-STD-883, Test Method 1015, Paragraph 3.2. Contact factory for details.

2. When applicable.

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Data Device Corporation (DDC) is a world leader in the design and manufacture of high-reliability Connectivity, Power and Control solutions (Data Networking; Power Distribution, Control and Conversion; Motor Control and Motion Feedback) for aerospace, defense, space, and industrial applications. With awards for quality, delivery and support, DDC has served these industries as a trusted resource for more than 50 years... providing proven solutions optimized for efficiency, reliability, and performance. Data Device Corporation brands include DDC, Beta Transformer Technology Corporation, National Hybrid Inc., North Hills Signal Processing Corporation, Pascall Electronics Ltd., and XCEL Power Systems Ltd. DDC is headquartered in Bohemia, NY and has manufacturing operations in New York, California, Mexico, and the United Kingdom.

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Certifications -

Data Device Corporation is ISO 9001:2008, AS 9100 Rev C, EN 9100, and JIS Q9100 certified. DDC has been granted certification by the Defense Logistics Agency, Land & Maritime (DLA) for manufacturing Class D, G, H, and K hybrid products in accordance with MIL-PRF-38534. Industry documents used to support DDC's certifications and Quality system are MIL-STD-883, ANSI/NCSL Z540-1, IPC-A-610, MIL-STD-202, JESD-22, and J-STD-020.

Beta Transformer Technology Corporation (BTTC) and its subsidiaries are ISO 9001:2008 and AS 9100 Rev C certified. BTTC has been granted certification as a qualified source of transformers by the Defense Logistics Agency, Land & Maritime (DLA) and is listed on the QPL for products MIL-PRF 21038/27-01 through -31 Product Levels C, M and T.

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Environment

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