VITESSE

VSC7939
Data Sheet

SONET/SDH 3.125Gb/s Laser Diode Driver with Automatic Power Control

FEATURES

- Power Supply: +3.3V, +5V or –5.2V
- AC- or DC-Coupled to Laser Diode
- Programmable Modulation Current: 5mA to 60mA
- Programmable Bias Current: 2mA to 100mA
- Enable /Disable Control
- Typical Rise/Fall Times of 60ps
- Automatic Optical Average Power Control
- Modulation and Bias Current Monitors

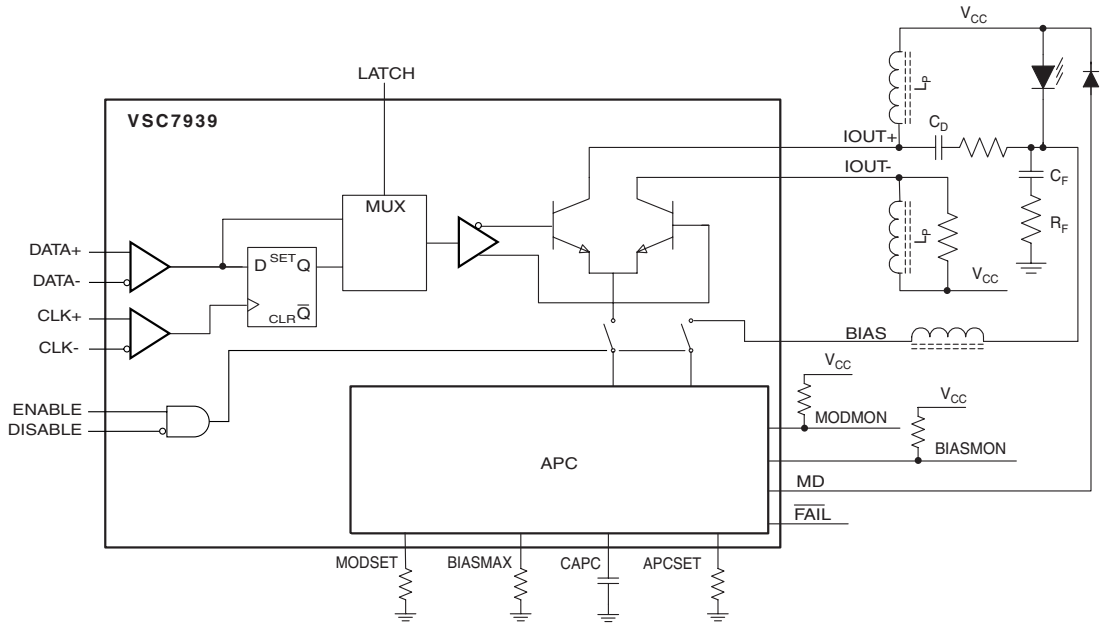
APPLICATIONS

- SONET/SDH at 155Mb/s, 622Mb/s, 1.244Gb/s, 2.488Gb/s, 3.125Gb/s
- Full-Speed Fibre Channel (1.062Gb/s, 2.124Gb/s)
- OC-48, OC-12, OC-3 Modules
- SFF/SFP Modules
- CWDM Modules
- DWDM Modules

GENERAL DESCRIPTION

The VSC7939 is a single +3.3V, +5V or –5.2V supply laser diode driver for SONET/SDH applications up to 3.125Gb/s. External resistors set a wide range of bias and modulation currents for driving the laser. Data and clock inputs accept differential PECL signals. The Automatic Power Control (APC) loop maintains a constant average optical power over temperature and lifetime. The dominant pole of the APC loop can be controlled with an external capacitor. Other features include enable/disable control, short-circuit protection for the modulation and bias inputs, short rise and fall times, and failure-monitor output to indicate when the APC loop is unable to maintain the desired average optical power. The VSC7939 is available in a 32-pin MLF or 32-pin TQFP package. The device is also available in lead(Pb)-free packages, VSC7939XRP and VSC7939XYE.

VSC7939 Block Diagram



REVISION HISTORY

This section describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

Revision 4.2

Revision 4.2 of this data sheet was published in January 2007. The following is a summary of the changes implemented in the data sheet:

- The VSC7939-W device was removed, because it is no longer available.
- The VSC7939XRP and VSC7939XYE lead(Pb)-free packages were added. For more information, see "Ordering Information," page 17.

Revision 4.1

Revision 4.1 of this data sheet was published in November 2002. The following is a summary of the changes implemented in the data sheet:

- 5.2 V power supply references were added.
- Equations 8, 9, 10, and 11 were revised.
- The duty cycle crossing point range parameter was added to the AC specifications.
- Power supply voltage parameters for positive and negative supply operations were added to the recommended operating conditions.
- The package drawing was updated to include dimensions for the exposed pad.

Revision 4.0

Revision 4.0 of this data sheet was published in April 2002. This was the first production-level publication of the document.

SPECIFICATIONS

Typical values are for T_A = +25°C and V_{CC} = +3.3V operation, unless otherwise noted.

Table 1. DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Condition
I_{CC}	Power Supply Current		45	55	mA	R_{MODSET} = 7.3kΩ, $R_{BIASMAX}$ = 4.8kΩ, I_{BIAS} and I_{MOD} excluded, V_{CC} = +3.3V, unlatched
			60	65	mA	R_{MODSET} = 7.3kΩ, $R_{BIASMAX}$ = 4.8kΩ, I_{BIAS} and I_{MOD} excluded, V_{CC} = +5V, unlatched
I_{CC_MAX}	Maximum Power Supply Current		265		mA	I_{MOD} = 60mA, I_{BIAS} = 100mA included, V_{CC} = +5.25V, +85°C, latched.
I_{BIAS}	Bias Current Range	2		100	mA	Voltage at BIAS pin = (V_{CC} - 1.6)
I_{BIAS_OFF}	Bias Off Current			200	µA	ENABLE = LOW or DISABLE = HIGH(1)
S_{BIAS}	Bias Current Stability		230		ppm/°C	APC open loop. I_{BIAS} = 100mA
			900			APC open loop. I_{BIAS} = 2mA
$BIAS_{AA}$	Bias Current Absolute Accuracy	-15		+15	%	Refers to part-to-part variation
VR_{MD}	Monitor Diode Reverse Bias Voltage	1.5			V	VR_{MD} = V_{CC} - V_{MD}
I_{MD}	Monitor Diode Reverse Current Range	18		1000	µA	APC closed loop
S_{MD_BIAS}	Monitor Diode Bias Setpoint Stability	-480	-50	+480	ppm/°C	I_{MD} = 1mA(2)
			90			I_{MD} = 18µA(2)
MD_{AA}	Monitor Diode Bias Absolute Accuracy	-15		+15	%	Refers to part-to-part variation
I_{MOD}	Modulation Current Range	5		60	mA	
I_{MOD_OFF}	Modulation Off Current			200	µA	ENABLE = LOW or DISABLE = HIGH(1)
MOD_{AA}	Modulation Current Absolute Accuracy	-15		+15	%	See Note 2
S_{MOD}	Modulation Current Stability	-800	-50	+480	ppm/°C	I_{MOD} = 60mA
			250			I_{MOD} = 5mA
A_{BIAS}	BIASMON to I_{BIAS} Gain		37		A/A	$I_{BIAS}/I_{BIASMON}$
A_{MOD}	MODMON to I_{MOD} Gain		27		A/A	I_{MOD}/I_{MODMON}

1. *Both IBIAS and IMOD will turn off if MODSET or BIASMAX is grounded.*
2. *Assumes laser diode to monitor diode transfer function does not change with temperature.*

.

Table 2. AC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Condition
t_{SU}	Input Latch Setup Time	100			ps	LATCH = HIGH
t_H	Input Latch Hold Time	100			ps	LATCH = HIGH
t_{DEN}	Enable/Start-up Delay		250		ns	APC open loop
t_R, t_F	Output Rise and Fall Time		60	80	ps	20% to 80%, I_{MOD} = 60mA, V_{CC} = +3.3V, +5V
PWD	Pulse Width Distortion(1, 2)		10	50	ps	
DC_{RANGE}	Duty Cycle Crossing Point Range	45		55	%	
CID_{MAX}	Maximum Consecutive Identical Digits	80			bits	
t_J	Jitter Generation		7	20	ps_{p-p}	0-1 pattern
J_{TOT}	Total Jitter		20	40	ps_{p-p}	$PRBS^{23}$-1 pattern, I_{MOD} = 60mA

1. *Measured with 622Mb/s 0-1 pattern, LATCH = HIGH.*
2. *PWD = (wider pulse - narrower pulse) / 2.*

Table 3. PECL and TTL/CMOS Inputs/Outputs

Symbol	Parameter	Min	Typ	Max	Units	Condition
V_{ID}	Differential Input Voltage	100		1600	mV_{p-p}	(DATA+)-(DATA-)
V_{ICM}	Common-Mode Input Voltage	V_{CC} -1.49	V_{CC} -1.32	V_{CC} -V_{ID}/4	V	PECL-compatible
I_{IN}	Clock and Data Input Current	-1		15	µA	
V_{IH}	TTL Input High Voltage (ENABLE, DISABLE, LATCH)	2.0			V	
V_{IL}	TTL Input LOW Voltage (ENABLE, DISABLE, LATCH)			0.8	V	
V_{OH}	TTL Output HIGH Voltage ($\overline{FAIL}$)	2.4	V_{CC} - 0.3	V_{CC}	V	Sourcing 50µA
V_{OL}	TTL Output LOW Voltage ($\overline{FAIL}$)			0.44	V	Sinking 100µA

Table 4. ENABLE/DISABLE Truth Table

ENABLE	DISABLE	Output Currents
Floating	Floating	Off
Floating	HIGH	Off
Floating	LOW	On
HIGH	Floating	Off
HIGH	HIGH	Off
HIGH	LOW	On
LOW	Floating	Off
LOW	HIGH	Off
LOW	LOW	Off

Table 5. LATCH Truth Table

LATCH	Mode
Floating	Clocked
HIGH	Clocked
LOW	Bypass

Table 6. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Condition
$V_{CC} - V_{EE}$	Power Supply Voltage	+3.135		+5.5	V	
V_{CC}	Power Supply Voltage for Positive Supply Operation		+3.3		V	V_{EE} = GND
V_{CC}	Power Supply Voltage for Positive Supply Operation		+5.0		V	V_{EE} = GND
V_{EE}	Power Supply Voltage for Negative Supply Operation		-5.2		V	V_{CC} = GND
T_A	Ambient Temperature Range	-40		+85	°C	

Table 7. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Condition
$V_{CC} - V_{EE}$	Power Supply Voltage	-0.5	+7	V	
	Current into BIAS	-20	+150	mA	
	Current into MD	-5	+5	mA	
	Current into $\overline{FAIL}$	-10	+30	mA	
	Voltage at DATA+, DATA-, CLK+, CLK-, ENABLE, DISABLE, LATCH	-0.5	V_{CC} + 0.5	V	
	Voltage at MODSET, BIASMAX, APCSET, MD, $\overline{FAIL}$	-0.5	+3.0	V	
	Voltage at OUT+, OUT-	-0.5	V_{CC} + 1.5	V	
	Voltage at BIAS	-0.5	V_{CC} + 0.5	V	
V_{ESD}	ESD Voltage (human body model)	-350	+350	V	
T_J	Operating Junction Temperature	-55	+150	°C	
T_S	Storage Temperature	-65	+165	°C	

Stresses listed under Absolute Maximum Ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

FUNCTIONAL DESCRIPTION

The VSC7939 is a high-speed laser driver with Automatic Power Control and is designed to operate up to 3.125Gb/s with a +3.3V,+5V, or –5.2V supply. The data and clock inputs support PECL inputs as well as other inputs that meet the common-mode voltage and differential voltage swing specifications. The differential pair output stage is capable of sinking up to 60mA from the laser with typical rise and fall times of 60ps. This output may be DC-coupled for 5V operation. To allow for larger output swings during +3.3V operation, the VSC7939 is designed to be AC-coupled to the laser cathode with a pull-up inductor for DC-biasing. This configuration isolates laser forward voltage from the output circuitry and allows the output at OUT+ to swing above and below the supply voltage V_{CC}. The key features of the VSC7939 are Automatic Power Control (APC), low power supply current, and fast rise and fall times. The VSC7940 is a pin-compatible modified version of the VSC7939 capable of 100mA output currents.

Automatic Power Control

To ensure constant average optical power, the device offers APC. A photodiode mounted in the laser package provides optical feedback to compensate for changes in average laser output power due to changes that affect laser performance such as temperature and laser lifetime. The laser bias current is adjusted by the APC loop according to the reference current set at APCSET by an external resistor. An external capacitor at CAPC controls the time constant for the APC feedback loop. The recommended value for CAPC is 0.1µF. This value reduces pattern-dependent jitter associated with the APC feedback loop and guarantees stability. If the APC loop cannot adjust the bias current to track the desired monitor current, $\overline{\text{FAIL}}$ is set LOW.

The device may be operated with or without APC. To utilize APC, a capacitor must be connected at CAPC (0.1µF) and a resistor must be connected at APCSET to set the average optical power. For open-loop operation (no APC), a 100kΩ resistor should be connected between APCSET and GND. CAPC has no effect on open-loop operation. In both modes of operation, resistors to GND should be placed at BIASMAX and MODSET to set the bias and modulation currents.

The APCSET, BIASMAX, and MODSET inputs utilize a bandgap voltage of 1.17V to set the current flow. For example, to set the internal APC current to 500mA:

$$\text{RAPCSET} = 1.17\text{V} / 500\text{mA} = 2.43\text{k}\Omega \quad \textbf{(EQ 1)}$$

Both BIASMAX and MODSET multiply this current internally so that it is compared to the actual values. BIASMAX is multiplied by 222, and MODSET is multiplied by 174. For example, to set the maximum bias to 50mA, select:

$$R_{BIASMAX} = 1.17\text{V} / (50\text{mA}/222) = 5.19\text{k}\Omega \quad \textbf{(EQ 2)}$$

To set the maximum modulation to 60mA, select:

$$R_{MODSET} = 1.17\text{V} / (60\text{mA}/174) = 3.39\text{k}\Omega \quad \textbf{(EQ 3)}$$

Data Retiming

The VSC7939 provides inputs for differential PECL clock signals for data retiming to minimize jitter at high speeds. To incorporate this function, LATCH should be connected to V_{CC}. If this function is unused, CLK+ should be connected to V_{CC}, CLK- should be left unconnected, and LATCH should be connected to GND.

Short-Circuit Protection

If either BIASMAX or MODSET is shorted to ground, both the bias and modulation currents are turned off.

Modulation and Bias Current Monitors

The VSC7939 provides monitoring of the modulation and bias currents using BIASMON and MODMON. These pins sink a current proportional to the actual modulation and bias currents. MODMON sinks approximately $1/27^{th}$ of the amount of modulation current and BIASMON sinks approximately $1/37^{th}$ of the amount of the bias current. These pins should be tied through a pull-up resistor to V_{CC}. The resistors must be chosen so that the voltage at MODMON is greater than V_{CC} - 1.0V and the voltage at BIASMON is greater than V_{CC} -1.6V.

Enable/Disable

Two pins are provided to allow either ENABLE or DISABLE control. If ENABLE is used, connect DISABLE to ground. If DISABLE is used, leave ENABLE floating. Both modulation and bias currents are turned off when ENABLE is LOW or DISABLE is HIGH. Typically, ENABLE or DISABLE turns off the laser within 10ns to 20ns and turns on the laser in about 200ns.

Controlling Modulation Current

The output modulation current may be determined from the following equation:

$$I_{MOD} = P_{p-p} / \eta = 2 \bullet P_{AVE} \bullet (r_e-1) / (r_e+1) / \eta \quad \textbf{(EQ 4)}$$

where, P_{p-p} is peak-to-peak optical power, P_{AVE} is average power, r_e is extinction ratio, and η is laser slope efficiency.

A resistor at MODSET controls the output bias current. The graph of I_{MODSET} vs. R_{MODSET} in "Typical Operating Characteristics," page 9 describes the relationship between the resistor at MODSET and the output modulation current at +25°C. After determining the desired output modulation current, use the graph to determine the appropriate resistor value at MODSET. Alternatively, the following equation may be used to calculate the set resistor:

$$R_{MODSET} = 1.17V / (\text{Modulation Current} / 174) \quad \textbf{(EQ 5)}$$

For example, to set the modulation to 60mA, select R_{MODSET} = 1.17V / (60mA / 174) = 3.39kΩ

Controlling Bias Current

A resistor at BIASMAX should be used to control the output bias current. The graph of $I_{BIASMAX}$ vs. $R_{BIASMAX}$ in "Typical Operating Characteristics," page 9 describes the relationship between the resistor at BIASMAX and the output bias current at +25°C If the APC is not used, the appropriate resistor value at BIASMAX is determined by first selecting the desired output bias current and then using the graph to determine the appropriate resistor value at BIASMAX. When using APC, BIASMAX sets the maximum allowed bias current. After determining the maximum end-of-life bias current at +85°C for the laser, refer to the graph of $I_{BIASMAX}$ vs. $R_{BIASMAX}$ in "Typical Operating Characteristics," page 9 to select the appropriate resistor value. Alternatively, the following equation may be used to calculate the set resistor:

$$R_{BIASMAX} = 1.17V / (\text{BiasCurrent} / 222) \quad \textbf{(EQ 6)}$$

For example, to set the maximum bias current to 50mA, select:

$$R_{BIASMAX} = 1.17V / (50mA / 222) = 5.19k\Omega \quad \textbf{(EQ 7)}$$

Laser Diode Interface

An RC shunt network should be placed at the laser output interface. The sum of the resistor placed at the output and the laser diode resistance should be 25Ω. For example, if the laser diode has a resistance of 5Ω, a 20Ω resistor should be placed in series with the laser. For optimal performance, a bypass capacitor should be placed close to the laser anode.

A "snubber network" consisting of a capacitor C_F and resistor R_F should be placed at the laser output to minimize reflections from the laser (see "VSC7939 Block Diagram," page 1). Suggested values for these components are 80Ω and 2pF, respectively; however, these values should be adjusted until an optical output waveform is obtained.

Reducing Pattern-Dependent Jitter

Three design values significantly affect pattern-dependent jitter: the APC capacitor (C_{APC}), the pull-up inductor at the output (L_P), and the AC-coupling capacitor at the output (C_D). As previously stated, the recommended value for the capacitor C_{APC} is 0.1µF. This results in a 10kHz loop bandwidth which makes the pattern-dependent jitter from the APC loop negligible.

For 2.5Gb/s data rates, the recommended value for C_D is 0.056µF. The time constant at the output is dominated by L_P. The variation in the peak voltage should be less that 12% of the average voltage over the maximum consecutive identical digit (CID) period. The following equation approximates this time constant for a CID period (t) of 100UI = 40ns:

$$L_P = -t / \ln(1-12\%) = 7.8t = L_P / 25\Omega \quad \textbf{(EQ 8)}$$

Therefore, the inductor L_P should be a 7.8µH SMD ferrite bead inductor for this case.

Input/Output Considerations

Although the VSC7939 is PECL-compatible, it is not required to drive the device. The inputs must only meet the common-mode voltage and differential voltage swing specifications.

Power Consumption

The following equation provides the device supply current (I_{CC}) in terms of quiescent current (I_Q), modulation current (I_{MOD}), and bias current (I_{BIAS}):

$$I_{CC} = I_Q + 1.9 \bullet I_{MOD} + 1.4 \bullet I_{BIAS} \quad \textbf{(EQ 9)}$$

For +3.3V operation, I_Q is 40mA.

This equation may be used to determine the estimated power dissipation:

$$P_{DIS} = V_{CC} \bullet I_Q \quad \textbf{(EQ 10)}$$

For example, if the device is operated at +3.3V with a 30mA modulation current and a 10mA bias current, the supply current will be:

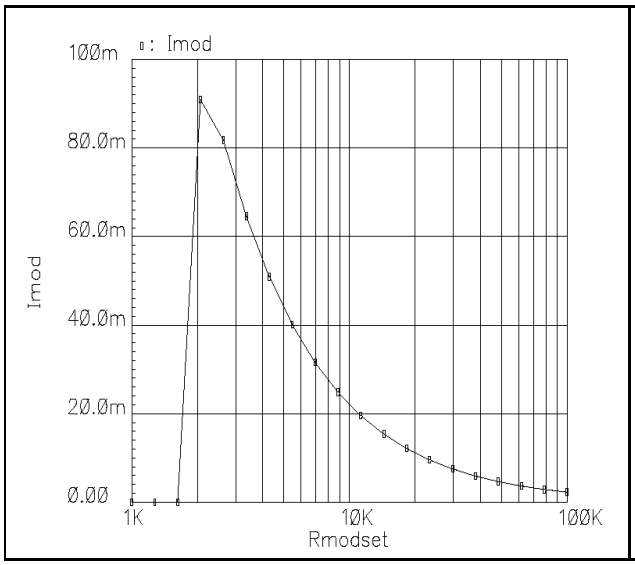
$$I_{CC} = 40mA + 1.9 \bullet 30mA + 1.4 \bullet 10mA = 111mA \quad \textbf{(EQ 11)}$$

This corresponds to a power dissipation of +3.3V • 111mA = 366mW.

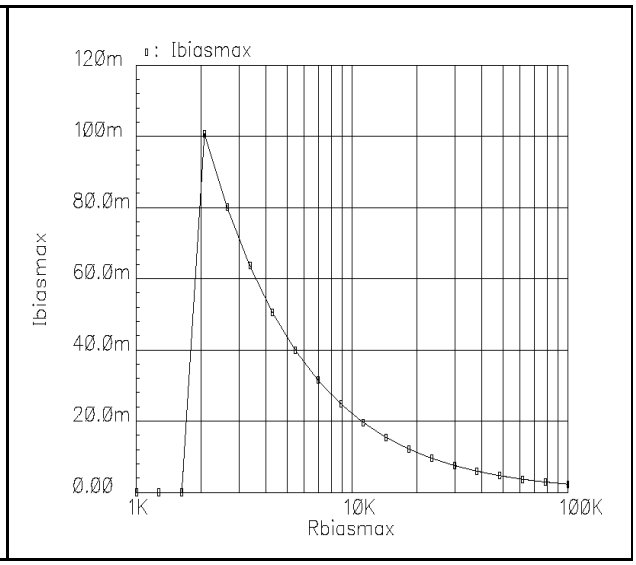
TYPICAL OPERATING CHARACTERISTICS

T_A = +25°C and V_{CC} = +3.3V.

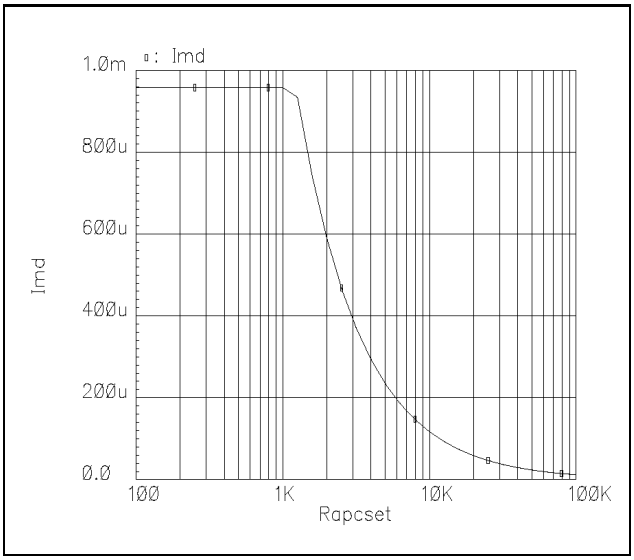
I_{MODSET} vs. R_{MODSET}



$I_{BIASMAX}$ vs. $R_{BIASMAX}$



I_{MD} vs. R_{APCSET}



APPLICATIONS INFORMATION

The following is a typical design example for the VSC7939, assuming +3.3V operation with APC.

Select a Laser

Table 8 provides specifications for a typical communication-grade laser capable of operating at 2.5Gb/s.

Table 8. Typical Laser Characteristics

Symbol	Parameter	Value	Unit
λ	Wavelength	1310	nm
P_{AVE}	Average Optical Output Power	6	mW
I_{th}	Threshold Current	6	mA
ρ_{MON}	Laser to Monitor Transfer	0.04	mA/mW
η	Laser Slope Efficiency	0.4	mW/mA
T_C	Operating Temperature Range	-40 to +85	°C

Select Resistor for APCSET

The monitor diode current is estimated by:

$$I_{MD} = P_{AVE} \bullet \rho_{MON} = 6mW \bullet 0.04mA/mW = 0.24mA \quad \textbf{(EQ 12)}$$

The I_{MD} vs. R_{APCSET} in "Typical Operating Characteristics," page 9 shows the resistor at APCSET should be 5kΩ.

Select Resistor for MODSET

To ensure some minimum extinction ratio over temperature and lifetime, assume an optimal extinction ratio (r_e) of 20 (13dB) at +25°C. The modulation current may be calculated from the following equation:

$$I_{MOD} = P_{p\text{-}p} / \eta = 2 \bullet P_{AVE} \bullet (r_e\text{-}1) / (r_e+1) / \eta = 2 \bullet 6mW \bullet (20 - 1) / (20 + 1) / 0.4mW/mA = 27.1mA \quad \textbf{(EQ 13)}$$

The graph of I_{MODSET} vs. R_{MODSET} in "Typical Operating Characteristics," page 9 shows the resistor for MODSET should be 8.5kΩ.

Select Resistor for BIASMAX

The maximum threshold current at +85°C and end of life must be determined. A graph of a typical laser's I_{th} versus T_C reveals a maximum threshold current of 30mA at +85°C. Therefore, the maximum bias can be approximated by:

$$I_{BIASMAX} = I_{TH\_MAX} + I_{MOD} / 2 = 30mA + 27.1mA / 2 = 43.6mA \quad \textbf{(EQ 14)}$$

The graph of $I_{BIASMAX}$ vs. $R_{BIASMAX}$ in "Typical Operating Characteristics," page 9 shows the resistor for BIASMAX should be 5kΩ.

Select Resistors for MODMON and BIASMON

Assuming the modulation and bias currents never exceed 120mA, the following equations provide values for the resistor at MODMON, R_{MODMON} and the resistor at BIASMON, $R_{BIASMON}$:

$$R_{MODMON} = 1V \bullet 27/120mA = 225\Omega \quad \textbf{(EQ 15)}$$

$$R_{BIASMON} = 1.6V \bullet 37/120mA = 493\Omega \quad \textbf{(EQ 16)}$$

A voltage of 4.8V at MODMON would indicate a modulation current of:

$$I_{MOD} = (5.0V - 4.8V) \bullet 27/225mA = 24mA \quad \textbf{(EQ 17)}$$

PCB Layout Guidelines

Use high frequency PCB layout techniques with solid ground planes to minimize crosstalk and EMI. Keep high speed traces as short as possible for signal integrity. The output traces to the laser diode must be short to minimize inductance. Short output traces provide best performance.

PIN DESCRIPTIONS

The VSC7939 device has 32 pins, which are described in this section.

Pin Diagram

The following illustration shows the pin diagram for the VSC7939RP and VSC7939XRP devices.

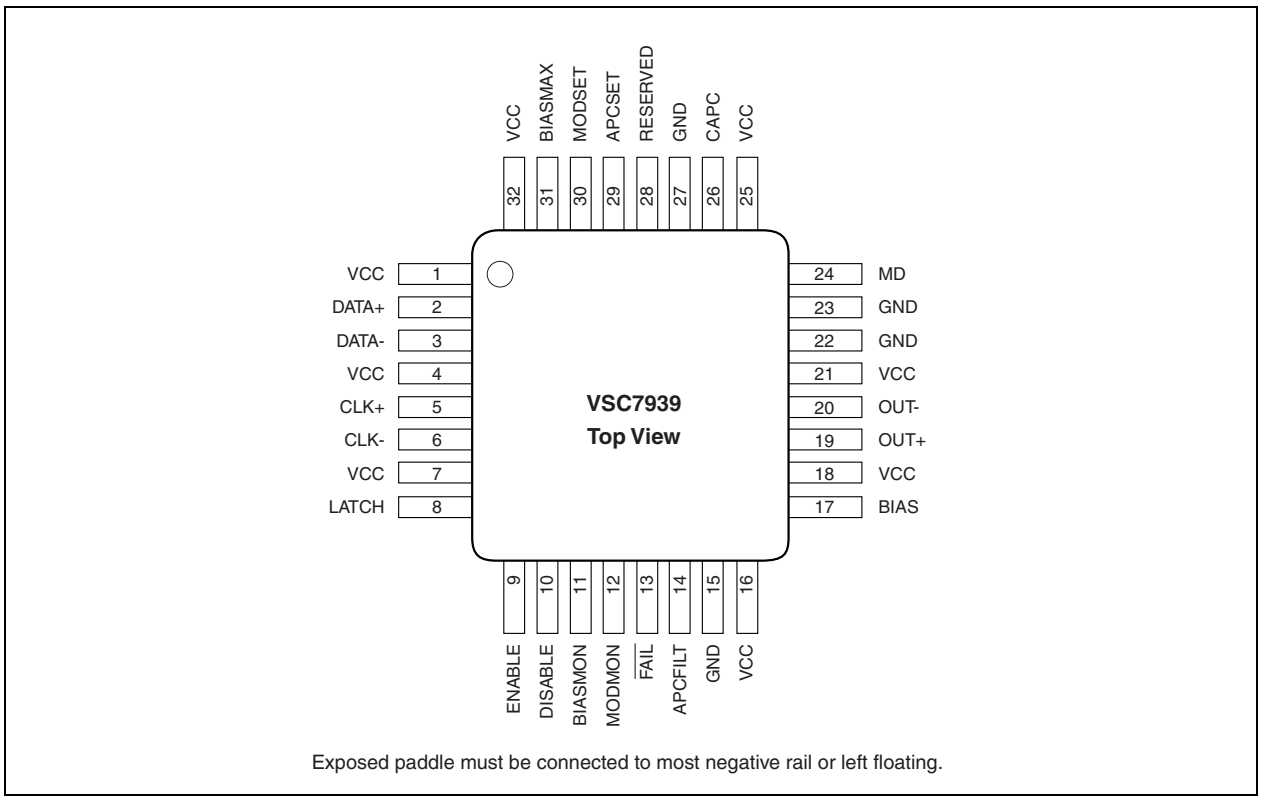


Figure 1. Pin Diagram for 32-Pin TQFP (RP and XRP)

Pin Diagram

The following illustration shows the pin diagram for the VSC7939YE and VSC7939XYE devices.

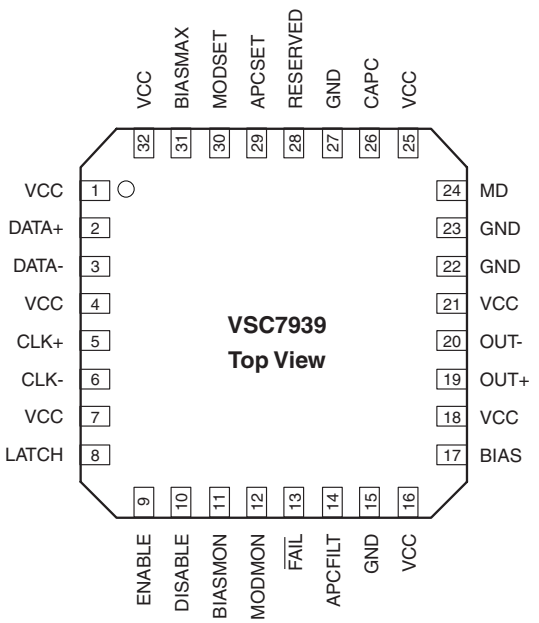


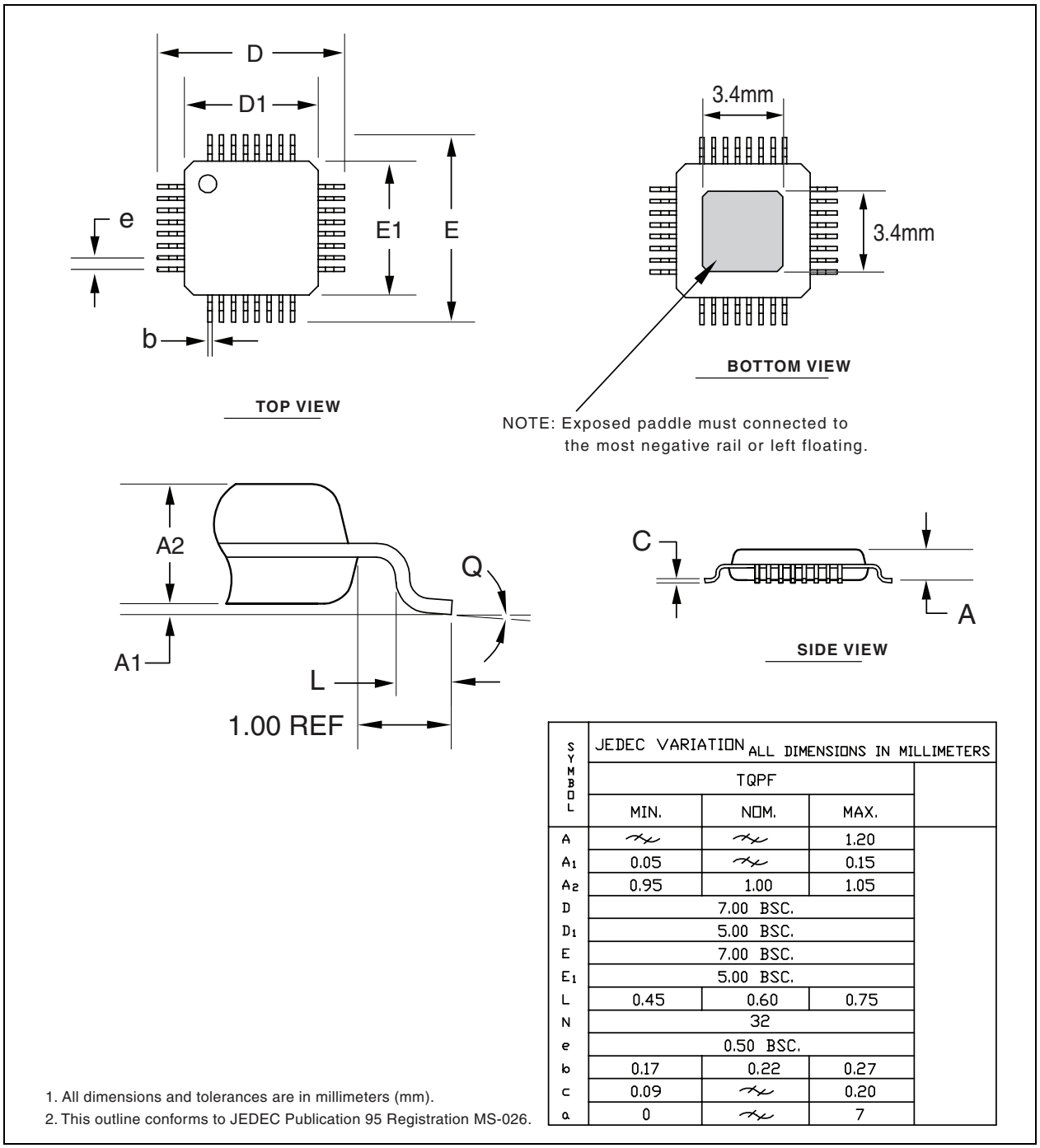
Figure 2. Pin Diagram 32-Pin MLF (YE and XYE)

Pin Identifications

This section contains the pin descriptions for the VSC7939 device.

Table 9: Pin Identifications

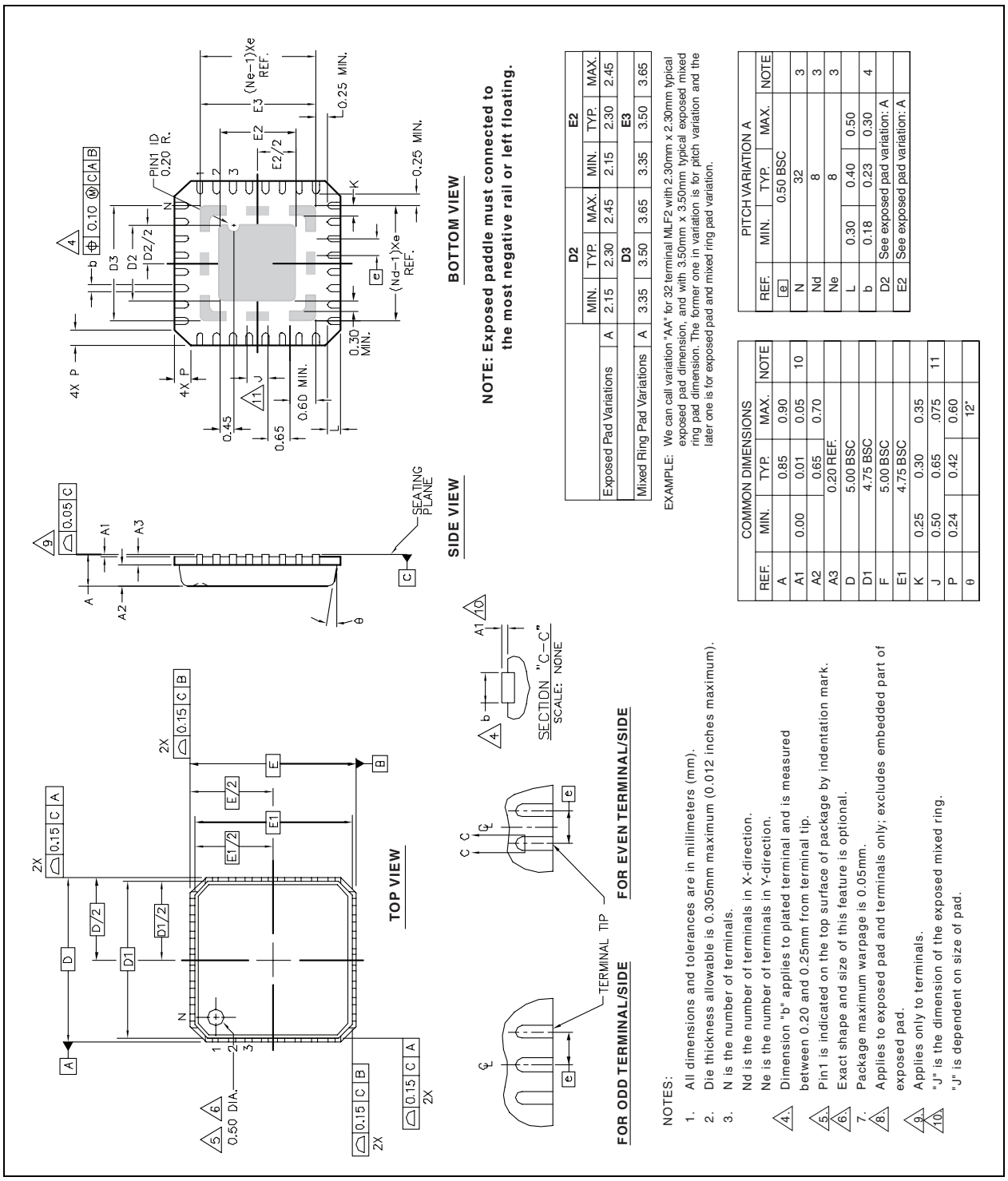
Pin Name	Pin Number	Description
GND	15, 22, 23, 27	Ground
V_{CC}	1, 4, 7, 16, 18, 21, 25, 32	+3.3V or +5V Power Supply
DATA+	2	Positive Data Input (PECL)
DATA-	3	Negative Data Input (PECL)
CLK+	5	Positive Clock Input (PECL). Connect to V_{CC} if LATCH function is not used.
CLK-	6	Negative Clock Input (PECL). Leave unconnected if LATCH function is not used.
LATCH	8	Latch Input (TTL/CMOS). Connect to V_{CC} or leave floating for data retiming and GND for direct data.
ENABLE	9	Enable Input (TTL/CMOS). If used, connect DISABLE to GND. Connect to V_{CC} or leave floating for normal operation, and GND to disable laser bias and modulation currents.
DISABLE	10	Disable Input (TTL/CMOS). If used, leave ENABLE pin floating. Connect to GND or V_{CC} for normal operation, or leave floating to disable laser bias and modulation currents.
BIASMON	11	Bias Current Monitor. Sink current source that is proportional to the laser bias current.
MODMON	12	Modulation Current Monitor. Sink current source that is proportional to the laser modulation current.
$\overline{FAIL}$	13	Output (TTL/CMOS). When LOW, indicates APC failure.
APCFILT	14	No effect on device operation.
BIAS	17	Laser Bias Current Output
OUT+	19	Positive Modulation Current Output. I_{MOD} flows when input data is HIGH.
OUT-	20	Negative Modulation Current Output. I_{MOD} flows when input data is LOW.
MD	24	Monitor Diode Input. Connect to monitor photodiode anode.
CAPC	26	Capacitor to GND sets dominant pole of the APC feedback loop.
RESERVED	28	Do not connect.
APCSET	29	Connect resistor to GND to set desired average optical power. If APC is not used, connect 100kΩ resistor to GND.
MODSET	30	Connect resistor to GND to set desired modulation current.
BIASMAX	31	Connect resistor to GND to set maximum bias current. The APC function can subtract from this value but cannot add to it.



SYMBOL	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
	TQPF			
	MIN.	NOM.	MAX.	
A			1.20	
A_1	0.05		0.15	
A_2	0.95	1.00	1.05	
D		7.00 BSC.		
D_1		5.00 BSC.		
E		7.00 BSC.		
E_1		5.00 BSC.		
L	0.45	0.60	0.75	
N		32		
e		0.50 BSC.		
b	0.17	0.22	0.27	
c	0.09		0.20	
α	0		7	

1. All dimensions and tolerances are in millimeters (mm).
2. This outline conforms to JEDEC Publication 95 Registration MS-026.

Figure 3. Package Drawing for 32-Pin TQFP (RP and XRP)



		D2			E2		
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
Exposed Pad Variations	A	2.15	2.30	2.45	2.15	2.30	2.45
		D3			E3		
Mixed Ring Pad Variations	A	3.35	3.50	3.65	3.35	3.50	3.65

EXAMPLE: We can call variation "AA" for 32 terminal MLF2 with 2.30mm x 2.30mm typical exposed pad dimension, and with 3.50mm x 3.50mm typical exposed mixed ring pad dimension. The former one in variation is for pitch variation and the later one is for exposed pad and mixed ring pad variation.

COMMON DIMENSIONS				
REF.	MIN.	TYP.	MAX.	NOTE
A		0.85	0.90	
A1	0.00	0.01	0.05	10
A2		0.65	0.70	
A3		0.20 REF.		
D		5.00 BSC		
D1		4.75 BSC		
F		5.00 BSC		
E1		4.75 BSC		
K	0.25	0.30	0.35	
J	0.50	0.65	.075	11
P	0.24	0.42	0.60	
θ			12°	

PITCH VARIATION A				
REF.	MIN.	TYP.	MAX.	NOTE
[e]		0.50 BSC		
N		32		3
Nd		8		3
Ne		8		3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4
D2	See exposed pad variation: A			
E2	See exposed pad variation: A			

NOTES:
1. All dimensions and tolerances are in millimeters (mm).
2. Die thickness allowable is 0.305mm maximum (0.012 inches maximum).
3. N is the number of terminals.
   Nd is the number of terminals in X-direction.
   Ne is the number of terminals in Y-direction.
4. Dimension "b" applies to plated terminal and is measured between 0.20 and 0.25mm from terminal tip.
5. Pin1 is indicated on the top surface of package by indentation mark.
6. Exact shape and size of this feature is optional.
7. Package maximum warpage is 0.05mm.
8. Applies to exposed pad and terminals only; excludes embedded part of exposed pad.
9. Applies only to terminals.
10. "J" is the dimension of the exposed mixed ring.
    "J" is dependent on size of pad.

Figure 4. Package Drawing for 32-Pin MLF (YE and XYE)

ORDERING INFORMATION

Lead(Pb)-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

VSC7939 SONET/SDH 3.125Gb/s Laser Diode Driver with Automatic Power Control

Part Number	Description
VSC7939RP	32-Pin TQFP, 5mm x 5mm Body
VSC7939XRP	Lead(Pb)-free, 32-Pin TQFP, 5mm x 5mm Body
VSC7939YE	32-Pin leadless MLF, 5mm x 5mm Body
VSC7939XYE	Lead(Pb)-free, 32-Pin leadless MLF, 5mm x 5mm Body

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