



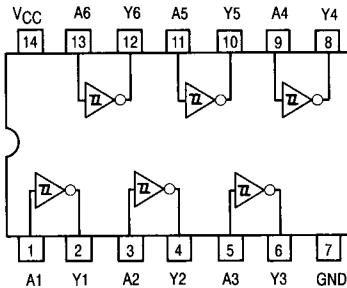
# Hex Schmitt-Trigger Inverter Gate

ELECTRICALLY TESTED PER:  
MIL-M-38510/31302

The 54LS14 contains logic gates which accept standard TTL input signals and provide standard TTL output levels. It is capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. Additionally, it has greater noise margin than conventional inverters.

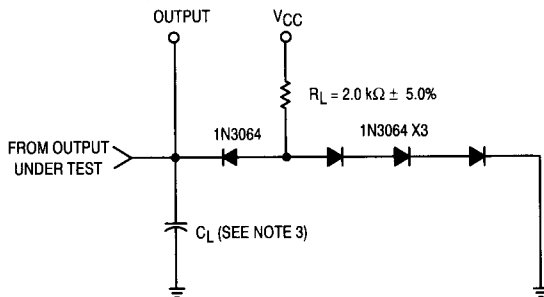
Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

### LOGIC DIAGRAM

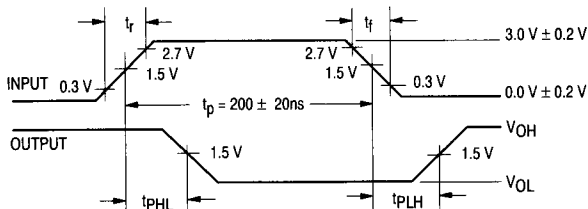


### AC TEST CIRCUIT

(LOAD FOR OUTPUT UNDER TEST)



### WAVEFORMS



## Military 54LS14



### AVAILABLE AS:

- 1) JAN: JM38510/31302BXA
- 2) SMD: N/A
- 3) 883: 54LS14/BXAJC

X = CASE OUTLINE AS FOLLOWS:  
PACKAGE: CERDIP: C  
CERFLAT: D  
LCC: 2

THE LETTER "M" APPEARS  
BEFORE THE / ON LCC.

### PIN ASSIGNMENTS

FUNCT.	DIL 632-08	FLATS 717-04	LCC 756A-02	BURN-IN (COND. A)
A1	1	1	2	GND
Y1	2	2	3	VCC
A2	3	3	4	GND
Y2	4	4	6	VCC
A3	5	5	8	GND
Y3	6	6	9	VCC
GND	7	7	10	GND
Y4	8	8	12	VCC
A4	9	9	13	GND
Y5	10	10	14	VCC
A5	11	11	16	GND
Y6	12	12	18	VCC
A6	13	13	19	GND
VCC	14	14	20	VCC

### BURN-IN CONDITIONS:

VCC = 5.0 V MIN/6.0 V MAX

### NOTES:

1. Pulse generator has the following characteristics:  $t_r \leq 15$  ns,  $t_f \leq 6.0$  ns,  $PRR \leq 1.0$  MHz and  $Z_{OUT} = 50 \Omega$ .
2. Terminal conditions (pins not designated may be high  $\geq 1.4$  V, low  $\leq 1.0$  V, or open).
3.  $C_L = 50$  pF  $\pm 10\%$ , including scope probe, and jig capacitance.
4.  $R_L = 2.0$  k $\Omega \pm 5.0\%$ .
5. Voltage measurements are to be made with respect to network ground terminal.

## 54LS14

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
VOH1	Logical "1" Output Voltage	2.5		2.5		2.5		V	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -0.4 mA, V <sub>IL</sub> = 0.5 V.
VOL1	Logical "0" Output Voltage		0.4		0.4		0.4	V	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 4.0 mA, V <sub>IH</sub> = 1.9 V.
VOH2	Logical "1" Output Voltage	2.5		2.5		2.5		V	V <sub>CC</sub> = 5.0 V, I <sub>OH</sub> = -0.4 V, V <sub>IL</sub> = (See Note 2).
VOL2	Logical "0" Output Voltage		0.4		0.4		0.4	V	V <sub>CC</sub> = 5.0 V, I <sub>OL</sub> = 4.0 mA, V <sub>IN</sub> = (See Note 3).
VIC	Input Clamping Voltage		-1.5					V	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA.
I <sub>IH1</sub>	Logical "1" Input Current		20		20		20	μA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.7 V.
I <sub>IH2</sub>	Logical "1" Input Current		100		100		100	μA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V.
I <sub>IL</sub>	Logical "0" Input Current	-0.12	-0.36	-0.12	-0.36	-0.12	-0.36	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.4 V.
I <sub>OS</sub>	Output Short Circuit Current	-15	-100	-15	-100	-15	-100	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0 V, V <sub>OUT</sub> = 0 V.
I <sub>CCH</sub>	Power Supply Current		16		16		16	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0 V.
I <sub>CCL</sub>	Power Supply Current		21		21		21	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V.
V <sub>IH</sub>	Logical "1" Input Voltage	1.9		1.9		1.9		V	V <sub>CC</sub> = 4.5 V.
V <sub>IL</sub>	Logical "0" Input Voltage		0.5		0.5		0.5	V	V <sub>CC</sub> = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V <sub>CC</sub> = 5.0 V, V <sub>INL</sub> = 0.5 V, and V <sub>INH</sub> = 2.5 V.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t <sub>PHL</sub>	Propagation Delay /Data-Output	5.0	32	5.0	52	5.0	52	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ.
t <sub>PHL</sub>	Output High-Low	—	22	—	47	—	47	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2.0 kΩ.
t <sub>PLH</sub>	Propagation Delay /Data-Output	5.0	32	5.0	52	5.0	52	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ.
t <sub>PLH</sub>	Output Low-High	—	22	—	47	—	47	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2.0 kΩ.

## NOTES:

1. The limits specified for C<sub>L</sub> = 15 pF are guaranteed but not tested.
2. Momentary 0.5 V, then 1.4 V without overshoot during test.
3. Momentary 1.9 V, then 1.0 V (all inputs) without undershoot during test.