Am28F010

131,072 x 8-Bit CMOS Flash E^{2}PROM

**Advanced
Micro
Devices**

DISTINCTIVE CHARACTERISTICS

- **Flasherase™ Electrical Bulk Chip-Erase**
  — One Second Typical Chip-Erase

- **Compatible with JEDEC Standard Byte Wide 32-pin EEPROM Pinouts**
  — 32-pin DIP
  — 32-pin PLCC

- **Flashrite™ Programming**
  — 10μS Typical Byte-Program
  — Less than 2 Second Typical Chip Program

- **Program and Erase Voltage**
  12.0V ±5% V$_{PP}$

- **Advanced CMOS Technology**
  — EPROM Compatible Process
  — Extensive Manufacturing Experience

- **Low Power Consumption**
  — 30mA Maximum Active Current
  — 100 μA Maximum Standby Current

- **Command Register Architecture for Microprocessor/Micro-controller Compatible Write Interface**

- **10,000 Program/Erase Cycles**

- **Provides On-Board Functionality for In-System-Write**

- **High Performance**
  — 120nS Maximum Access Time

- **On Board Address and Data Latches**

- **5V±10% Single Power Supply**

BLOCK DIAGRAM
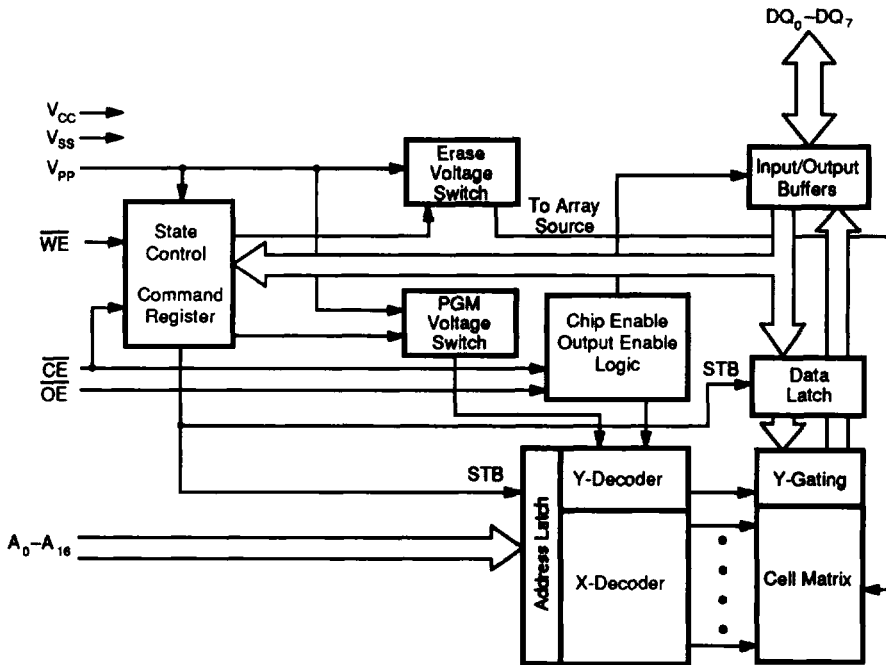
11559-001A

GENERAL DESCRIPTION

This device is an alternative to the full-featured EEPROM.

The 28F010 is targeted for in-system alterable code- or data-storage applications where full-feature EEPROM functionality is either not required or not cost effective. The Am28F010 CMOS Flash memory provides the highest performance and most cost-effective alternative for high density rewritable non-volatile memory. Flash memory adds electrical chip-erase and reprogramming to AMD's EPROM technology. The entire memory content may be Flash erased and reprogrammed in a PROM programmer or test socket, on board during subassembly test, in-system during final test or after sale. In-system electrical erasure increases the memory's flexibility, while providing time and cost savings.
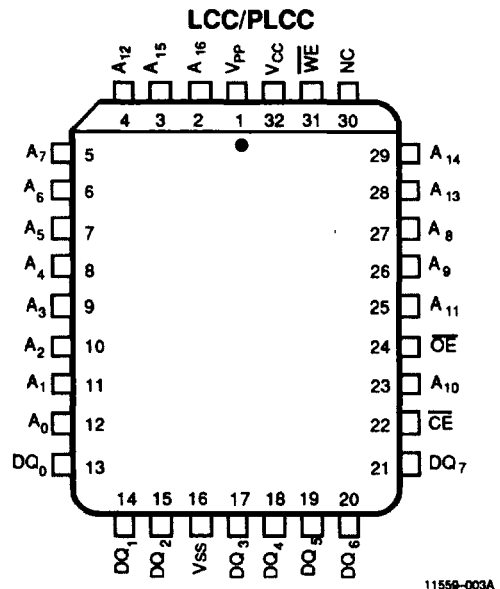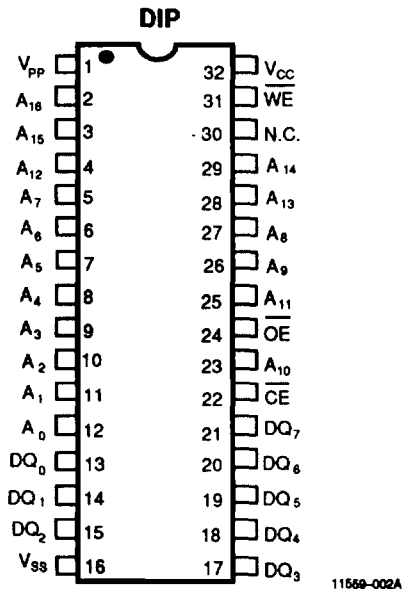
The device may be packaged in plastic DIP or PLCC and is ideal for use in auto-insertion manufacturing systems. The entire memory array may be erased and reprogrammed on-board using AMD's

Flasherase™ and Flashrite™ programming algorithms respectively.
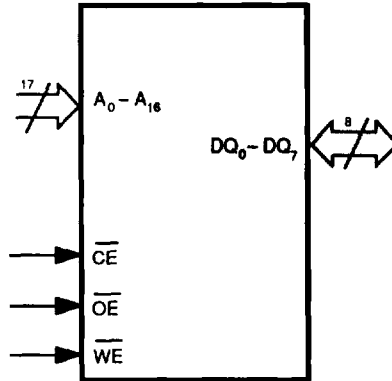
Typical Applications

Flash memory is ideal for storing code or data-tables in embedded control applications where periodic updates or data down-loading is required. Code updates may occur throughout the entire life of a system. Beginning with prototyping, code updates may also be necessary during subassembly or even in after-sale service. Electrical chip erasure eliminates the 15 to 20 minute ultraviolet erase and streamlines code updates. In addition both DIP or PLCC Flash devices may be soldered to the circuit board during subassembly. Test codes may be programmed into the device on board. Prior to shipment final code is downloaded to the device. Thus, Flash technology eliminates unnecessary handling and less reliable socketed connections, saves board space, and adds increased manufacturing flexibility. After-sale code updates are performed locally via an edge-connector, or remotely over a serial communication link.

CONNECTION DIAGRAMS

DIP

V_{PP}	1	32	V_{CC}
A_{16}	2	31	$\overline{WE}$
A_{15}	3	30	N.C.
A_{12}	4	29	A_{14}
A_7	5	28	A_{13}
A_6	6	27	A_8
A_5	7	26	A_9
A_4	8	25	A_{11}
A_3	9	24	$\overline{OE}$
A_2	10	23	A_{10}
A_1	11	22	$\overline{CE}$
A_0	12	21	DQ_7
DQ_0	13	20	DQ_6
DQ_1	14	19	DQ_5
DQ_2	15	18	DQ_4
V_{SS}	16	17	DQ_3

11559-002A

LCC/PLCC

11559-003A

LOGIC SYMBOL

11559-004A

FUNCTIONAL DESCRIPTION

In-circuit electrical erase and reprogramming gives flash memory the flexibility of EEPROM. A command register in the Flash device manages the electrical erasure and reprogramming. The command register architecture allows for fixed power supplies during erasure and programming and does not require high voltage on control pins.

Read Mode

The Flash device functions as a read only memory when high voltage is not applied to the V_{pp} pin. In this mode the external memory control signals produce the standard EPROM read, standby, output disable, and Auto-select modes.

Programming/Read Mode

High voltage on the V_{pp} pin enables the erase and programming functions of the device. The same EPROM read, standby, and output disable functions are available to the system when high voltage is applied to the Vpp pin. All functions associated with altering memory contents (erase, erase-verify, program, and program-verify) are accessed via the command register.

Standard microprocessor write timing is used to write commands into the register. Register contents serve as input to an internal state machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data required for programming or erase operations. Standard microprocessor read timings are used to access array data, access data for erase and program verification, or access the Auto-select modes. As with EEPROM devices, the 28F010 uses a dedicated $\overline{WE}$ control pin for command execution.

The command register is alterable only when high voltage is applied to Vpp. When high voltage is removed, the contents of the register default to the read command. The device then functions as a read only memory. V_{pp} may be controlled with system hardware to provide secure write protect.

Performance

AMD's Flash memories offer access times as fast as 120ns. This high performance allows operation of high-speed microprocessors and microcontrollers without wait-states. The Flash architecture supports separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls in order to eliminate bus contention.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (T_c)   0°C to +70°C
Industrial (I) Devices
Case Temperature (T_c)   −40°C to +85°C
Extended (E) Devices
Case Temperature (T_c)   −55°C to +125°C
Military (M) Devices
Case Temperature (T_c)   −55°C to +125°C

Operating ranges define those limits between which the functionality of the device is guaranteed.