T-46-23-12

Ordering number: EN3753

CMOS LSI

LC3518B, BM, BS, BL, BML, BSL

2048-word × 8-bit CMOS Static RAM

OVERVIEW

LC3518B series devices are silicon-gate CMOS, static RAM ICs configured as 2048 words × 8 bits. They incorporate two chip enables for easy memory expansion, and TTL-compatible, tristate outputs for direct interfacing with a bus.

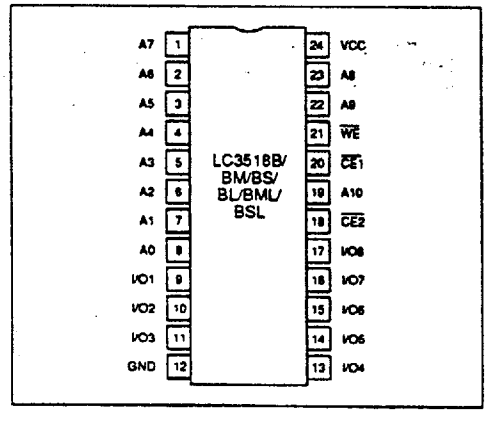
LC3518B series ICs feature a data retention mode and a low standby current, making them ideal for low-power or battery-powered equipment. In particular, the LC3518BL, LC3518BML and LC3518BSL offer a guaranteed maximum standby current of 1 μA at 60 deg. C.

LC3518B series ICs operate from a 5 V supply and are available in 24-pin DIPs, 24-pin MFPs and 24-pin SDIPs.

FEATURES

- 120 ns (LC3518B-12 series) and 150 ns (LC3518B-15 series) maximum address access times
- 0.2 μA at 25 deg. C and 1.0 μA at 60 deg. C (LC3518BL/BML/BSL-12/15), and 5.0 μA at 60 deg. C and 30 μA at 85 deg. C (LC3518B/BM/BS-12/15) maximum standby currents
- 9 mA maximum supply current at f = 1 MHz
- Data retention for V_{CC} = 2.0 to 5.5 V
- Asynchronous operation
- TTL-compatible, tristate input/outputs
- Single 5 V supply
- 24-pin DIP, 24-pin MFP and 24-pin SDIP

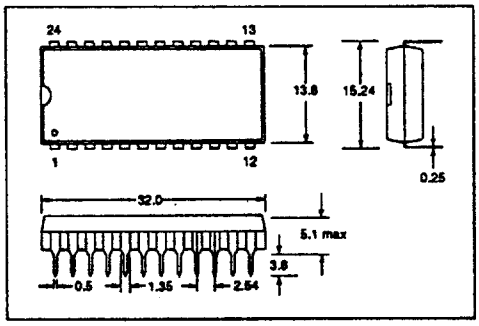
PINOUT



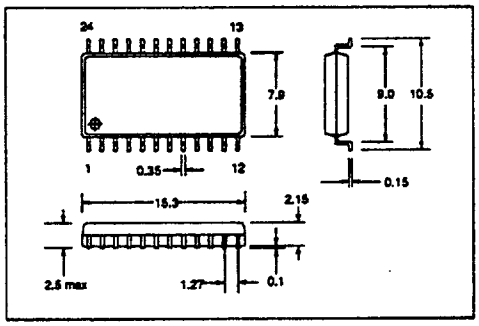
PACKAGE DIMENSIONS

Unit: mm

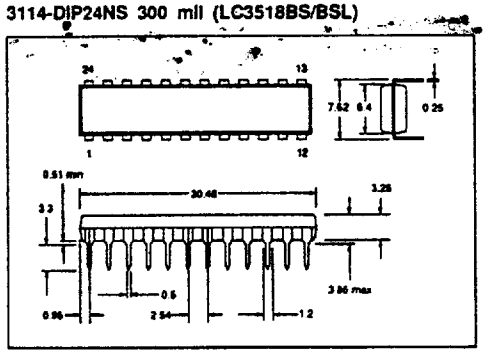
3072-DIP24NS (LC3518B/BL)



3045B-MFP24 (LC3518BM/BML)



3114-DIP24NS 300 mil (LC3518BS/BSL)



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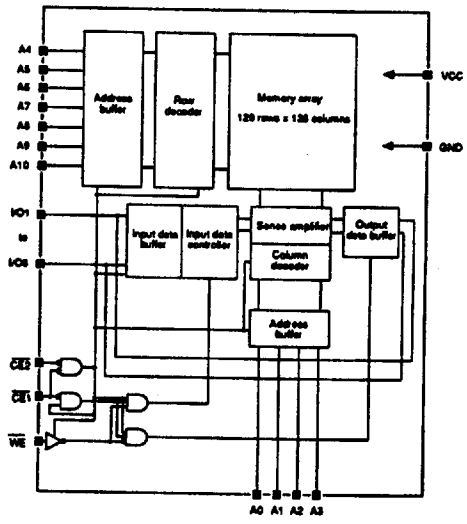
BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	Description
1 to 8, 19, 22, 23	A0 to A10	Address inputs
9 to 11, 13 to 17	I/O1 to I/O8	Data inputs/outputs
12	GND	Ground
18, 20	$\overline{CE2}$, $\overline{CE1}$	Chip enable inputs
21	$\overline{WE}$	Read/write select input
24	VCC	5 V supply

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC} max	7.0	V
Input voltage range	V_{IN}	−0.5 to V_{CC} + 0.5	V
Input/output voltage range	$V_{I/O}$	−0.5 to V_{CC} + 0.5	V
Operating temperature range	T_{opg}	−30 to 85	deg. C
Storage temperature range	T_{stg}	−55 to 125	deg. C

Recommended Operating Conditions

T_a = 25 deg. C

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	5.0	V
Supply voltage range	V_{CC} op	4.5 to 5.5	V

Electrical Characteristics

V_{CC} = 5 V ±10%, T_a = −30 to 85 deg. C unless otherwise noted

Parameter	Symbol	Condition		Rating min	Rating typ	Rating max	Unit
Quiescent supply current	I_{CCA1}	$\overline{CE1}$ = $CE2$ = 0 V, V_{IN} = V_{CC} or GND, I_{VO} = 0 mA		–	2	5	mA
		$\overline{CE1}$ = $CE2$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{VO} = 0 mA		–	5	15	
Average supply current	I_{CCA2}	Minimum cycle time, duty = 100%, I_{VO} = 0 mA		–	–	50	mA
		Cycle time = 1 µs, $\overline{CE1}$ = $CE2$ = 0 V, V_{IN} = V_{CC} or GND, I_{VO} = 0 mA		–	4	9	
Standby supply current	I_{CCS}	$\overline{CE1}$ or $CE2$ = V_{CC} − 0.2 V, V_{IN} = 0 V to V_{CC}. See note 1.	T_a = 60 deg. C	–	–	5.0	µA
			T_a = 85 deg. C	–	–	30	
		$\overline{CE1}$ or $CE2$ = V_{CC} − 0.2 V, V_{IN} = 0 V to V_{CC}. See note 2.	T_a = 25 deg. C	–	–	0.2	
			T_a = 60 deg. C	–	–	1.0	
		$\overline{CE1}$ or $CE2$ = V_{IH}, V_{IN} = 0 V to V_{CC}		–	1.0	3.0	mA
LOW-level input voltage	V_{IL}			−0.3	–	0.8	V
HIGH-level input voltage	V_{IH}			2.2	–	V_{CC} + 0.3	V
LOW-level output voltage	V_{OL}	I_{OL} = 2.0 mA		–	–	0.4	V
HIGH-level output voltage	V_{OH}	I_{OH} = −1.0 mA		2.4	–	–	V
Input capacitance	C_{IN}	V_{IN} = 0 V, f = 1 MHz, T_a = 25 deg. C		–	–	5	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1 MHz, T_a = 25 deg. C		–	–	10	pF
Input leakage current	I_{LI}	V_{IN} = 0 to V_{CC}		−1.0	–	1.0	µA
Input/output leakage current	I_{LO}	$\overline{CE1}$ or $CE2$ = V_{IH}, $V_{I/O}$ = 0 V to V_{CC}		−5.0	–	5.0	µA

Notes

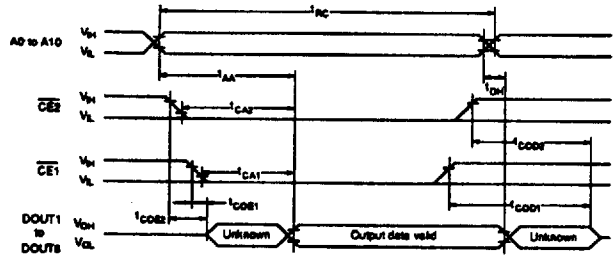
1. LC3518B/BM/BS-12/15
2. LC3518BL/BML/BSL-12/15
3. Typical values are measured at V_{CC} = 5.0 V and T_a = 25 deg. C.

Timing Characteristics

Test conditions

- LOW-level pulse—0.6 V
- HIGH-level pulse—2.4 V
- Input rise and fall times—5 ns
- LOW-level timing reference—V_{IL} = V_{OL} = 0.8 V
- HIGH-level timing reference—V_{IH} = V_{OH} = 2.2 V
- Output load—1 TTL gate + C_L = 100 pF (including jig capacitance)

Read timing

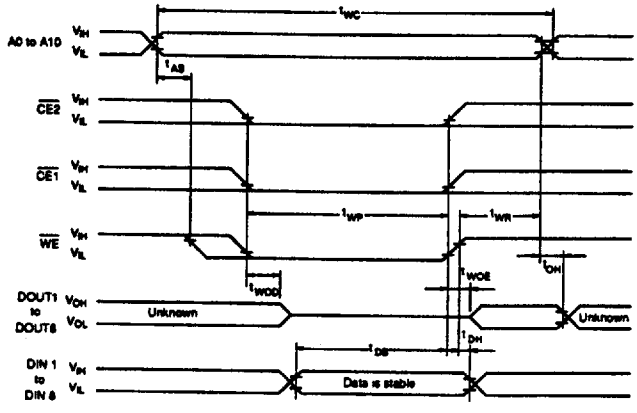


V_{CC} = 5 V ±10%, T_a = −30 to 85 deg. C

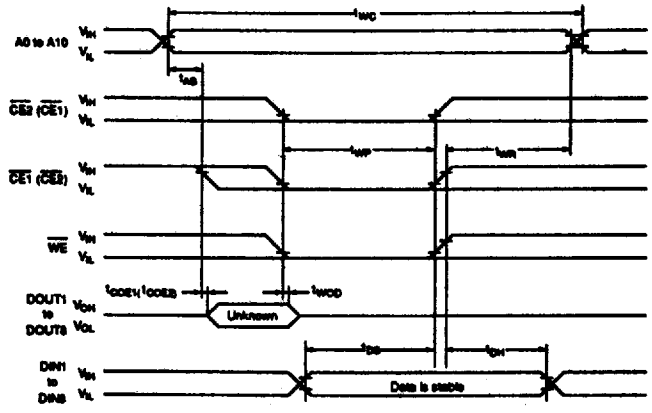
Parameter	Symbol	LC3518B/BM/BS-12, LC3518BL/BML/BSL-12		LC3518B/BM/BS-15, LC3518BL/BML/BSL-15		Unit
		min	max	min	max	
Read cycle time	t_{RC}	120	–	150	–	ns
Address access time	t_{AA}	–	120	–	150	ns
Chip-enable 1 access time	t_{CA1}	–	120	–	150	ns
Chip-enable 2 access time	t_{CA2}	–	120	–	150	ns
Output hold time	t_{OH}	20	–	20	–	ns
Chip-enable 1 propagation delay	t_{COE1}	10	–	10	–	ns
Chip-enable 2 propagation delay	t_{COE2}	10	–	10	–	ns
Chip-disable 1 propagation delay	t_{COD1}	–	40	–	50	ns
Chip-disable 2 propagation delay	t_{COD2}	–	40	–	50	ns

Write timing

- Write cycle 1



- Write cycle 2



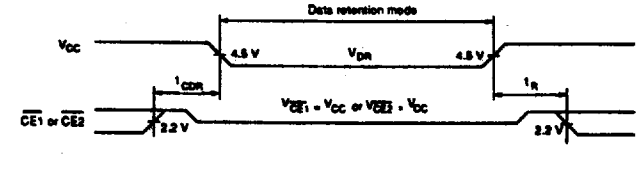
V_{CC} = 5 V ±10%, T_a = −30 to 85 deg. C

Parameter	Symbol	LC3518B/BM/BS-12, LC3518BL/BML/BSL-12		LC3518B/BM/BS-15, LC3518BL/BML/BSL-15		Unit
		min	max	min	max	
Write cycle time	t_{WC}	120	–	150	–	ns
Address setup time	t_{AS}	0	–	0	–	ns
Write pulsewidth	t_{WP}	100	–	120	–	ns
Write recovery time	t_{WR}	0	–	0	–	ns
Data setup time	t_{DS}	60	–	70	–	ns
Data hold time	t_{DH}	0	–	0	–	ns
Write-enable propagation delay	t_{WOE}	5	–	5	–	ns
Write-disable propagation delay	t_{WOD}	–	40	–	50	ns

Notes

1. Hold $\overline{WE}$ HIGH during the read cycle.
2. Do not apply opposite phase signals to DOUT when it is connected to the output bus.
3. t_{WP} is measured when $\overline{CE1}$, $\overline{CE2}$ and $\overline{WE}$ are LOW.
4. t_{WR}, t_{DS} and t_{DH} are measured when $\overline{CE1}$, $\overline{CE2}$ or $\overline{WE}$ is HIGH.
5. DOUT becomes high impedance when either $\overline{CE1}$ or $\overline{CE2}$ is HIGH, or $\overline{WE}$ is LOW.
6. t_{AS} is measured when $\overline{CE1}$, $\overline{CE2}$ and $\overline{WE}$ are LOW.
7. DOUT has the same phase as the data to be written during the write cycle.
8. DOUT is the data read out from the next address.

Data Retention Characteristics



T_a = –30 to 85 deg. C

Parameter	Symbol	Condition		Rating min	Rating typ	Rating max	Unit
Data retention mode supply voltage	V_{DR}	$\overline{CE1}$ or $\overline{CE2}$ = V_{CC}, V_{IN} = 0 V to V_{CC}		2.0	–	5.5	V
Data retention mode supply current	I_{CCDR}	$\overline{CE1}$ or $\overline{CE2}$ = V_{CC}, V_{CC} = 3.0 V, V_{IN} = 0 V to V_{CC}. See note 1.	T_a = 60 deg. C	–	–	4.0	µA
			T_a = 85 deg. C	–	–	20	
		$\overline{CE1}$ or $\overline{CE2}$ = V_{CC}, V_{CC} = 3.0 V, V_{IN} = 0 V to V_{CC}. See note 2.	T_a = 25 deg. C	–	–	0.2	
			T_a = 60 deg. C	–	–	1.0	
Chip-enable setup time	t_{CDR}			0	–	–	ns
Chip-enable hold time	t_R			t_{RC}	–	–	ns

Notes

1. LC3518B/BM/BS-12/15
2. LC3518BL/BML/BSL-12/15

Mode Selection

Mode	$\overline{CE2}$	$\overline{CE1}$	$\overline{WE}$	Input/output	Supply current
Reset cycle	L	L	H	Data output	I_{CCA}
Write cycle	L	L	L	Data input	I_{CCA}
Output disable	X	H	X	High impedance	I_{CCS}
Standby	H	X	X	High impedance	I_{CCS}

Note

X = don't care