

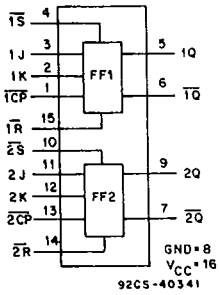
CD54/74HCT112
CD54/74HCT112

HARRIS SEMICOND SECTOR

27E D ■ 4302271 0017551 6 ■ HAS

High-Speed CMOS Logic

T-46-07-07



FUNCTIONAL DIAGRAM

Dual J-K Flip-Flop with Set and Reset

Negative-Edge Trigger

Type Features:

- Hysteresis on clock inputs for improved noise immunity and increased input rise and fall times
- Asynchronous set and reset
- Complementary outputs
- Buffered inputs
- Typical $f_{max} = 60 \text{ MHz}$ @ $V_{CC} = 5 \text{ V}$, $C_L = 15 \text{ pF}$, $T_A = 25^\circ \text{ C}$

Family Features:

- Fanout (Over Temperature Range):
Standard Outputs - 10 LSTTL Loads
Bus Driver Outputs - 15 LSTTL Loads
- Wide Operating Temperature Range:
CD74HC/HCT: -40 to $+85^\circ \text{ C}$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips/Signetics
- CD54HC/CD74HC Types:
2 to 6 V Operation
High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} ,
@ $V_{CC} = 5 \text{ V}$
- CD54HCT/CD74HCT Types:
4.5 to 5.5 V Operation
Direct LSTTL Input Logic Compatibility
 $V_{IL} = 0.8 \text{ V Max.}$, $V_{IH} = 2 \text{ V Min.}$
CMOS Input Compatibility
 $I_i \leq 1 \mu\text{A}$ @ V_{OL} , V_{OH}

The RCA-CD54/74HC112 and CD54/74HCT112 utilize silicon-gate CMOS technology to achieve operating speeds equivalent to LSTTL parts. They exhibit the low power consumption of standard CMOS integrated circuits, together with the ability to drive 10 LSTTL loads.

These flip-flops have independent J, K, Set, Reset, and Clock inputs and Q and \bar{Q} outputs. They change state on the negative-going transition of the clock pulse. Set and Reset are accomplished asynchronously by low-level inputs.

The 54HCT/74HCT logic family is functionally as well as pin-compatible with the standard 54LS/74LS logic family.

The CD54HC112 and CD54HCT112 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC112 and CD74HCT112 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

TRUTH TABLE
(EACH FLIP-FLOP)

INPUTS					OUTPUTS	
\bar{S}	\bar{R}	\bar{CP}	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H		L	L	No Change	
H	H		H	L	H	L
H	H		L	H	L	H
H	H		H	H	Toggle	
H	H	H	X	X	No Change	

* Output states unpredictable if \bar{S} and \bar{R} go High simultaneously after both being low at the same time.

H = High steady state.

L = Low steady state.

X = Irrelevant.

= High-to-Low transition.

CD54/74HCT112
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MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_i < -0.5$ V OR $V_i > V_{CC} + 0.5$ V)	± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$ V)	± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V $< V_o < V_{CC} + 0.5$ V)	± 25 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC}):	± 50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F, H)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+85^\circ\text{C}$
STORAGE TEMPERATURE (T_{STG})	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 \pm 1/32 in. (1.59 \pm 0.79 mm) from case for 10 s max.	$+265^\circ\text{C}$
Unit inserted into a PC board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	$+300^\circ\text{C}$

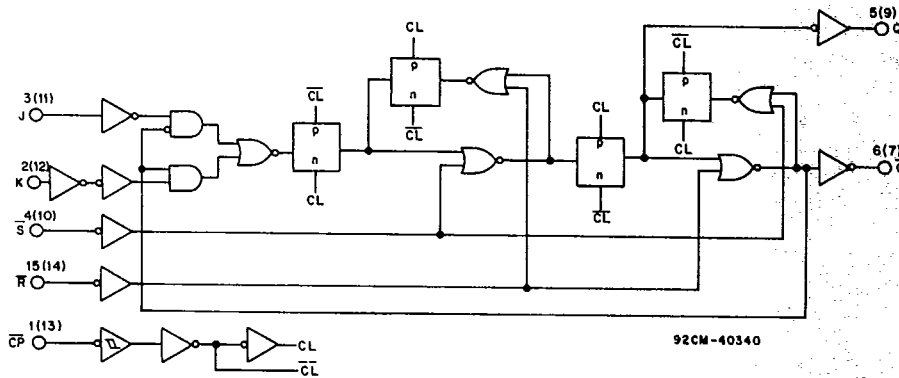


Fig. 1 - Flip-flop logic diagram.

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For $T_A =$ Full Package-Temperature Range) V_{CC} .*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_i, V_o	0	V_{CC}	V
Operating Temperature T_A :			
CD74 Types	-40	+85	$^\circ\text{C}$
CD54 Types	-55	+125	$^\circ\text{C}$
Input Rise and Fall Times, t_r, t_f •			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

* Unless otherwise specified, all voltages are referenced to Ground.
• Applicable for all inputs except clock.

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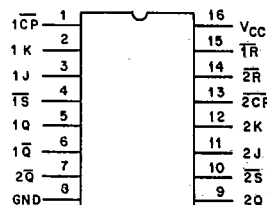
STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CD74HC112, CD54HC112										CD74HCT112, CD54HCT112										UNITS				
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE			54HC TYPE			TEST CONDITIONS			74HCT/54HCT TYPE			74HCT TYPE			54HCT TYPE			
	V _i V	I _o mA	V _{cc} V	+25°C			-40/ +85°C			-55/ +125°C			V _i V	V _{cc} V	+25°C			-40/ +85°C				-55/ +125°C			
				Min	Typ	Max	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max					
High-Level Input Voltage V _{IH}			2	1.5	—	—	1.5	—	1.5	—	—	—	4.5			2	—	—	2	—	2	—	—	V	
			4.5	3.15	—	—	3.15	—	3.15	—	—	—	to			—	—	—	—	—	—	—	—		
			6	4.2	—	—	4.2	—	4.2	—	—	—	5.5			—	—	—	—	—	—	—	—		
Low-Level Input Voltage V _{IL}			2	—	—	0.5	—	0.5	—	0.5	—	—	4.5			—	—	0.8	—	0.8	—	0.8	—	V	
			4.5	—	—	1.35	—	1.35	—	1.35	—	—	to			—	—	—	—	—	—	—	—		
			6	—	—	1.8	—	1.8	—	1.8	—	—	5.5			—	—	—	—	—	—	—	—		
High-Level Output Voltage V _{OH}	V _{IL} or V _{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	—	V _{IL} or V _{IH}	4.5	4.4	—	—	4.4	—	4.4	—	4.4	—	—	V	
CMOS Loads			4.5	4.4	—	—	4.4	—	4.4	—	—														
			6	5.9	—	—	5.9	—	5.9	—	—														
TTL Loads	V _{IL} or V _{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	—	V _{IL} or V _{IH}	4.5	3.98	—	—	3.84	—	3.7	—	—	—	—	V	
Low-Level Output Voltage V _{OL}	V _{IL} or V _{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	—	V _{IL} or V _{IH}	4.5	—	—	0.1	—	0.1	—	0.1	—	0.1	—	V	
CMOS Loads			4.5	—	—	0.1	—	0.1	—	0.1	—														
			6	—	—	0.1	—	0.1	—	0.1	—														
TTL Loads	V _{IL} or V _{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	—	V _{IL} or V _{IH}	4.5	—	—	0.26	—	0.33	—	0.4	—	—	—	V	
			5.2	6	—	—	0.26	—	0.33	—	0.4														
Input Leakage Current I _i	V _{cc} or Gnd		6	—	—	±0.1	—	±1	—	±1	—	Any Voltage Between V _{cc} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	—	±1	—	μA	
Quiescent Device Current I _{cc}	V _{cc} or Gnd	0	6	—	—	4	—	40	—	80	—	V _{cc} or Gnd	5.5	—	—	4	—	40	—	80	—	80	—	μA	
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI _{cc} *												V _{cc} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	—	—	—	μA	

*For dual-supply systems theoretical worst case (V_i = 2.4 V, V_{cc} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS *
1S, 2S	0.5
1K, 2K	0.6
1R, 2R	0.65
1J, 2J, 1CP, 2CP	1



TOP VIEW 92CS-40339

TERMINAL ASSIGNMENT

* Unit Load is ΔI_{cc} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	C _L (pF)	TYPICAL VALUES		UNITS
		HC	HCT	
Propagation Delay \overline{CP} to Q, \overline{Q} t _{PLH} , t _{PHL}	15	14	14	ns
		13	13	ns
		15	14	ns
\overline{CP} Frequency f _{max}	15	60	60	MHz
Power Dissipation Capacitance *	C _{PD}	12	20	pF

* C_{PD} is used to determine the dynamic power consumption, per flip-flop.
 $P_D = C_{PD} V_{CC}^2 f_i + \sum C_L V_{CC}^2 f_o$ where: f_i = input frequency C_L = output load capacitance
 f_o = output frequency V_{CC} = supply voltage

PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	TEST CONDITION V _{CC} V	LIMITS												UNITS
		25°C				-40°C to +85°C				-55°C to +125°C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Pulse Width \overline{CP} t _w	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
	4.5	16	—	16	—	20	—	20	—	24	—	24	—	
	6	14	—	—	—	17	—	—	—	20	—	—	—	
\overline{R} , \overline{S}	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
	4.5	16	—	18	—	20	—	23	—	24	—	27	—	
	6	14	—	—	—	17	—	—	—	20	—	—	—	
Set-up Time J, K to \overline{CP} t _{su}	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
	4.5	16	—	16	—	20	—	20	—	24	—	24	—	
	6	14	—	—	—	17	—	—	—	20	—	—	—	
Hold Time J, K to \overline{CP} t _h	2	0	—	—	—	0	—	—	—	0	—	—	—	ns
	4.5	0	—	3	—	0	—	3	—	0	—	3	—	
	6	0	—	—	—	0	—	—	—	0	—	—	—	
Removal Time \overline{R} to \overline{CP} \overline{S} to \overline{CP} t _{rem}	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
	4.5	16	—	20	—	20	—	25	—	24	—	30	—	
	6	14	—	—	—	17	—	—	—	20	—	—	—	
\overline{CP} Frequency f _{max}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
	4.5	30	—	30	—	25	—	25	—	20	—	20	—	
	6	35	—	—	—	29	—	—	—	23	—	—	—	

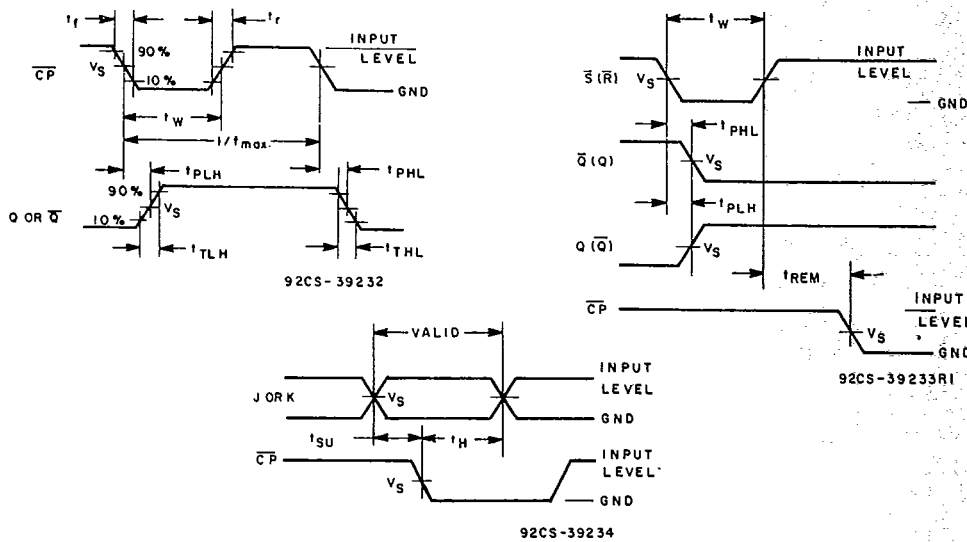
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SWITCHING CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = 6$ ns)

CHARACTERISTIC	TEST CONDITION	LIMITS										UNITS			
		25°C				-40°C to +85°C				-55°C to +125°C					
		HC		HCT		74HC		74HCT		54HC			54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		Min.	Max.	
Propagation Delay \overline{CP} to Q, \overline{Q}	t_{PLH}	2	—	175	—	—	—	220	—	—	—	265	—	—	ns
	t_{PHL}	4.5	—	35	—	35	—	44	—	44	—	53	—	53	
		6	—	30	—	—	—	37	—	—	—	45	—	—	
\overline{S} to Q, \overline{Q}		2	—	155	—	—	—	195	—	—	—	235	—	—	ns
		4.5	—	31	—	32	—	39	—	40	—	47	—	48	
		6	—	26	—	—	—	33	—	—	—	40	—	—	
\overline{R} to Q, \overline{Q}		2	—	180	—	—	—	225	—	—	—	270	—	—	ns
		4.5	—	36	—	37	—	45	—	46	—	54	—	56	
		6	—	31	—	—	—	38	—	—	—	46	—	—	
Output Transition Time	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_i		—	10	—	10	—	10	—	10	—	10	—	10	pF



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_s	50% V_{CC}	1.3 V

Fig. 2 - Transition times, propagation delay times, and setup and hold times.

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