HS-565BRH, HS-565BEH

Radiation Hardened High Speed, Monolithic Digital-to-Analog Converter

FN4607
Rev 4.00
May 7, 2012

The HS-565BRH, HS-565BEH are fast, radiation hardened 12-bit current output, digital-to-analog converters. This part replaces the HS-565ARH, which is no longer available. The monolithic chips include a precision voltage reference, thin-film R-2R ladder, reference control amplifier and twelve high-speed bipolar current switches.

The Intersil Dielectric Isolation process provides latch-up free operation while minimizing stray capacitance and leakage currents, to produce an excellent combination of speed and accuracy. Also, ground currents are minimized to produce a low and constant current through the ground terminal, which reduces error due to code-dependent ground currents.

HS-565BRH, HS-565BEH die are laser trimmed for a maximum integral nonlinearity error of ±0.25 LSB at +25°C. In addition, the low noise buried zener reference is trimmed both for absolute value and minimum temperature coefficient.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-96755. A "hot-link" is provided on our website for downloading.

Features

- Electrically Screened to SMD # 5962-96755
- QML Qualified per MIL-PRF-38535 Requirements
- Total Dose . . . . . 100 krad (Si) (Max)
- DAC and Reference on a Single Chip
- Pin Compatible with AD-565A and HI-565A
- Very High Speed: Settles to 0.50 LSB in 500ns Max
- Monotonicity Guaranteed Over Temperature
- 0.50 LSB Max Nonlinearity Guaranteed Over Temperature
- Low Gain Drift
  (Max., DAC Plus Reference) . . . . . 50ppm/°C
- ±0.75 LSB Accuracy Guaranteed Over Temperature
  (±0.125 LSB Typical at +25°C)

Applications

- High Speed A/D Converters
- Precision Instrumentation
- Signal Reconstruction

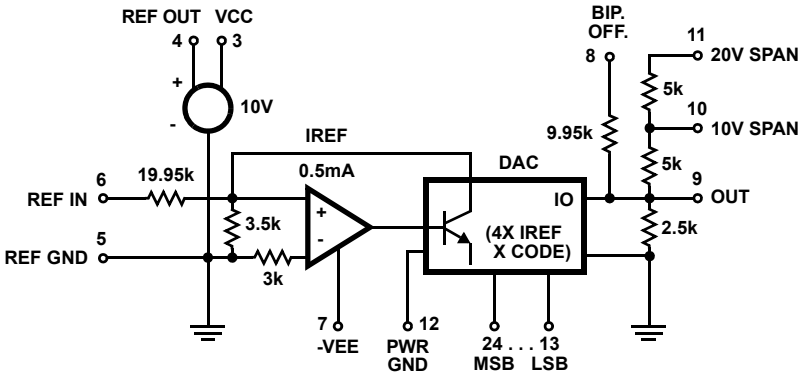
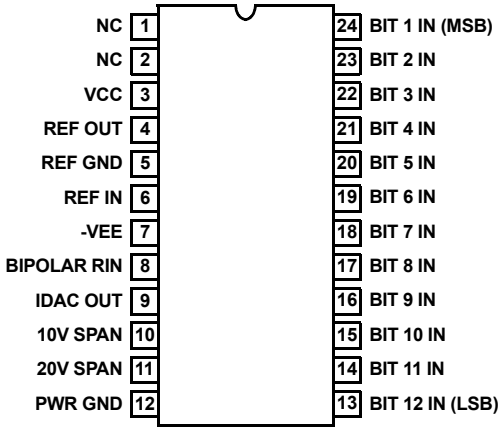


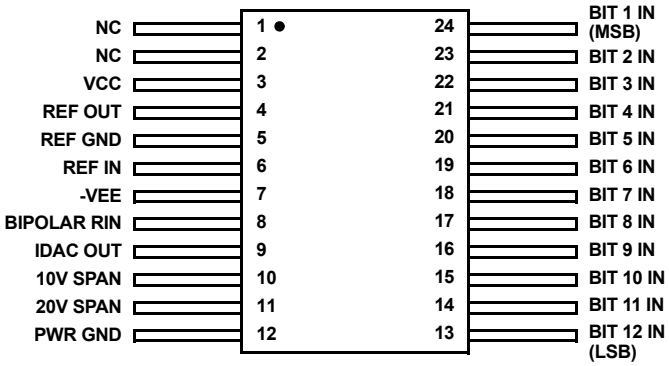
FIGURE 1. FUNCTIONAL DIAGRAM

Pin Configurations

HS1-565BRH, HS1-565BEH
MIL-STD-1835 CDIP2-T24
(SBDIP)
TOP VIEW



HS9-565BRH, HS9-565BEH
MIL-STD-1835 CDFP4-F24
(CERAMIC FLATPACK)
TOP VIEW

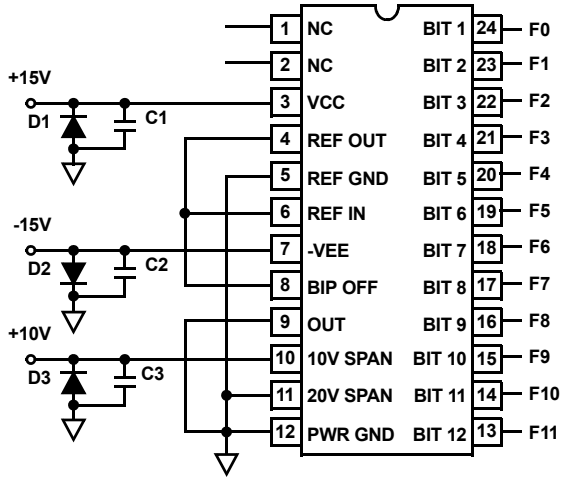


Ordering Information

ORDERING NUMBER	PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
5962R9675502V9A	HS0-565BRH-Q		+25		
5962R9675502VJC	HS1-565BRH-Q	Q 5962R96 75502VJC	-55 to +125	24 Ld SBDIP	D24.6
5962R9675502VXC	HS9-565BRH-Q	Q 5962R96 75502VXC	-55 to +125	24 Ld Flatpack	K24.A
HS9-565BRH/PROTO	HS9-565BRH/PROTO	HS9- 565BRH /PROTO	-55 to +125		
5962R9675503V9A	HS0-565BEH-Q		+25		
5962R9675503VJC	HS1-565BEH-Q	Q 5962R96 75503VJC	-55 to +125	24 Ld SBDIP	D24.6
5962R9675503VXC	HS9-565BEH-Q	Q 5962R96 75503VXC	-55 to +125	24 Ld Flatpack	K24.A

NOTE: These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.

Burn-In Bias Circuit



NOTES:

D1 = D2 = D3 = IN4002 or Equivalent

F0 to F11: VIH = 5.0V ±0.5V

VIL = 0.0V ±0.5V

F0 = 100kHz ±10% (50% Duty Cycle)

F1 = F0/2 F7 = F0/128

F2 = F0/4 F8 = F0/256

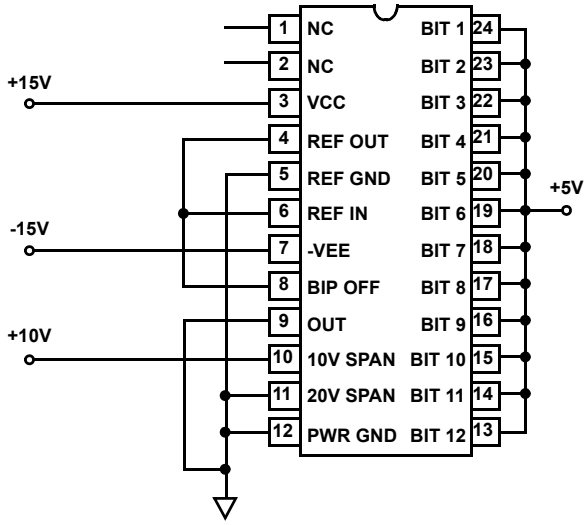
F3 = F0/8 F9 = F0/512

F4 = F0/16 F10 = F0/1024

F5 = F0/32 F11 = F0/2048

F6 = F0/64

Radiation Bias Circuit



NOTE: Power Supply Levels are ±0.5V

Definitions of Specifications

Digital Inputs

The HS-565BRH, HS-565BEH accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight binary, Two's Complement (see note below), or Offset Binary.

DIGITAL INPUT	ANALOG OUTPUT		
MSB...LSB	STRAIGHT BINARY	OFFSET BINARY	TWO'S COMPLEMENT (Note)
000.... 000	Zero	-FS (Full Scale)	Zero
100.... 000	0.50 FS	Zero	-FS
111.... 111	+FS - 1LSB	+FS - 1LSB	Zero - 1LSB
011.... 111	0.50 FS - 1LSB	Zero - 1LSB	+FS - 1LSB

NOTE: Invert MSB with external inverter to obtain Two's Complement Coding

Accuracy

Nonlinearity - Nonlinearity of a D/A converter is an important measure of its accuracy. It describes the deviation from an ideal straight line transfer curve drawn between zero (all bits OFF) and full scale (all bits ON).

Differential Nonlinearity - For a D/A converter, it is the difference between the actual output voltage change and the ideal (1 LSB) voltage change for a one bit change in code. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity; i.e., the output always increases and never decreases for an increasing input.

Settling Time

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale or major carry transition, settling to within 0.50 LSB of final value.

Drift

Gain Drift - The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (TH) and low (TL) temperatures. Gain drift is calculated for both high (TH - +25°C) and low ranges (+25°C - TL) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

Offset Drift - The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (TH) and low (TL) temperatures. Offset drift is calculated for both high (TH - +25°C) and low (+25°C - TL) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst case drift.

Power Supply Sensitivity

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

Compliance

Compliance Voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance Limit implies functional operation only and makes no claims to accuracy.

Glitch

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half scale or the major carry code transition from 011 . . . 1 to 100 . . . 0 or vice versa. For example, if turn ON is greater than turn OFF for 011 . . . 1 to 100 . . . 0, an intermediate state of 000 . . . 0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably.

Applying the HS-565BRH and HS-565BEH

OP AMP Selection

The HS-565BRH, HS-565BEH current output may be converted to voltage using the standard connections shown in Figures 2 and 3. The choice of operational amplifier should be reviewed for each application, since a significant trade-off may be made between speed and accuracy. Remember settling time for the DAC-amplifier combination is:

$$\sqrt{(t_D)^2 + (t_A)^2}$$

where t_D, t_A are settling times for the DAC and amplifier.

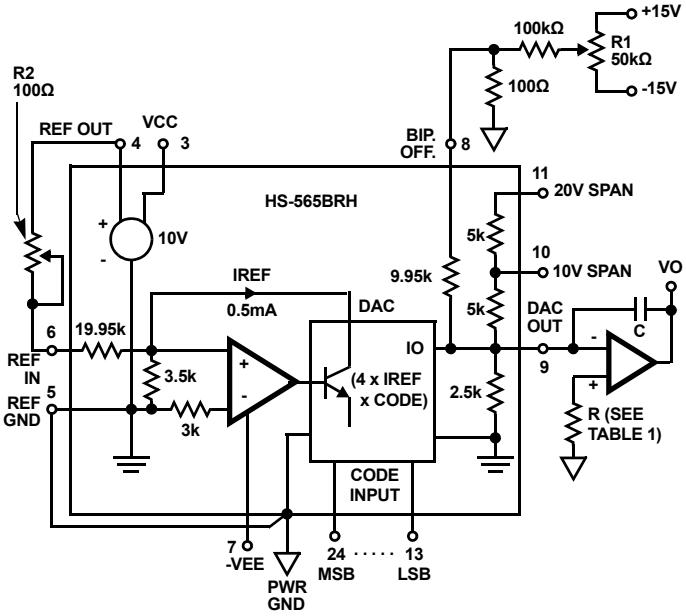


FIGURE 2. UNIPOLAR VOLTAGE OUTPUT

No Trim Operation

The HS-565BRH, HS-565BEH will perform as specified without calibration adjustments. To operate without calibration, substitute 50Ω resistors for the 100Ω trimming potentiometers: In Figure 2 replace R2 with 50Ω; also remove the network on pin 8 and connect 50Ω to ground. For bipolar operation in Figure 3, replace R3 and R4 with 50Ω resistors. Typical unipolar zero will be ±0.50 LSB plus the op amp offset.

The feedback capacitor C must be selected to minimize settling time.

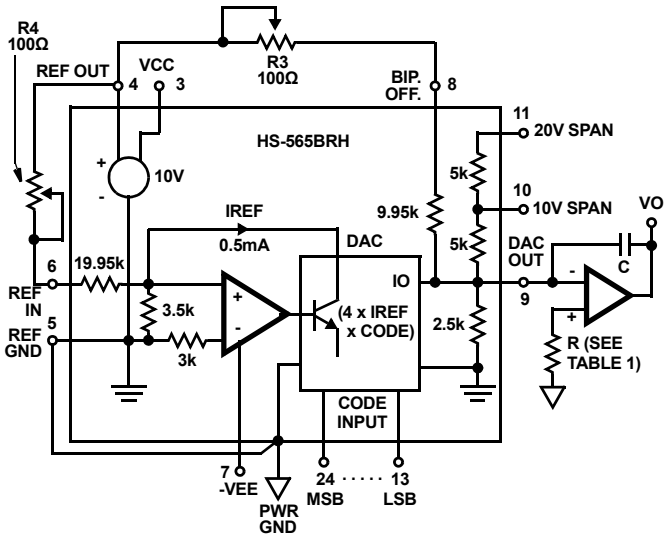


FIGURE 3. BIPOLAR VOLTAGE OUTPUT

Calibration

Calibration provides the maximum accuracy from a converter by adjusting its gain and offset errors to zero. For the HS-565BRH, HS-565BEH, these adjustments are similar whether the current output is used, or whether an external op amp is added to convert this current to a voltage. Refer to Table 1 for the voltage output case, along with Figure 2 or 3.

Calibration is a two step process for each of the five output ranges shown in Table 1. First adjust the negative full scale (zero for unipolar ranges). This is an offset adjust which translates the output characteristic, i.e., affects each code by the same amount.

Next adjust positive FS. This is a gain error adjustment, which rotates the output characteristic about the negative FS value.

For the bipolar ranges, this approach leaves an error at the zero code, whose maximum values is the same as for integral nonlinearity error. In general, only two values of output may be calibrated exactly; all others must tolerate some error. Choosing the extreme end points (plus and minus full scale) minimizes this distributed error for all other codes.

Settling Time

This is a challenging measurement, in which the result depends on the method chosen, the precision and quality of test equipment and the operating configuration of the DAC (test conditions). As a result, the different techniques in use by converter manufacturers can lead to consistently different results. An engineer should understand the advantage and limitations of a given test method before using the specified settling time as a basis for design.

The approach used for several years at Intersil calls for a strobed comparator to sense final perturbations of the DAC output waveform. This gives the LSB a reasonable magnitude (814mV) for the HS-565BRH, HS-565BEH, which provides the comparator with enough overdrive to establish an accurate ±0.50 LSB window about the final settled value. Also, the required test conditions simulate the DACs environment for a common application - use in a successive approximation A/D converter. Considerable experience has shown this to be a reliable and repeatable way to measure settling time.

The usual specification is based on a 10V step, produced by simultaneously switching all bits from off-to-on (tON) or on-to-off (tOFF). The slower of the two cases is specified, as measured from 50% of the digital input transition to the final entry within a window of ±0.50 LSB about the settled value. Four measurements characterize a given type of DAC:

(a) tON, to final value +0.50 LSB

(b) tON, to final value -0.50 LSB

(c) tOFF, to final value +0.50 LSB

(d) OFF, to final value -0.50 LSB

(Cases (b) and (c) may be eliminated unless the overshoot exceeds 0.50 LSB). For example, refer to Figures 4A and 4B for the measurement of case (d).

Procedure

As shown in Figure 4B, settling time equals tX plus the comparator delay (tD = 15ns). To measure tX,

- Adjust the delay on generator number 2 for a tX of several microseconds. This assures that the DAC output has settled to its final wave.
- Switch on the LSB (+5V)
- Adjust the VLSB supply for 50% triggering at COMPARATOR OUT. This is indicated by traces of equal brightness on the oscilloscope display as shown in Figure 4B. Note DVM reading.
- Switch to LSB to Pulse (P)
- Readjust the VLSB supply for 50% triggering as before, and note DVM reading. One LSB equals one tenth the difference in the DVM readings noted above.
- Adjust the VLSB supply to reduce the DVM reading by 5 LSBs (DVM reads 10X, so this sets the comparator to sense the final settled value minus 0.50 LSB). Comparator output disappears.
- Reduce generator number 2 delay until comparator output reappears, and adjust for “equal brightness”.
- Measure tX from scope as shown in Figure 4B. Settling time equals tX + tD, i.e., tX + 15ns.

TABLE 1. OPERATING MODES AND CALIBRATION

MODE	CIRCUIT CONNECTIONS				CALIBRATION		
	OUTPUT RANGE	PIN 10 TO	PIN 11 TO	RESISTOR (R)	APPLY INPUT CODE	ADJUST	TO SET VO
Unipolar (See Figure 2)	0 to +10V	VO	Pin 10	1.43k	All 0’s All 1’s	R1 R2	0V +9.99756V
	0 to +5V	VO	Pin 9	1.1k	All 0’s All 1’s	R1 R2	0V +4.99878V
Bipolar (See Figure 3)	±10V	NC	VO	1.69k	All 0’s All 1’s	R3 R4	-10V +9.99512V
	±5V	VO	Pin 10	1.43k	All 0’s All 1’s	R3 R4	-5V +4.99756V
	±2.5V	VO	Pin 9	1.1k	All 0’s All 1’s	R3 R4	-2.5V +2.49878V

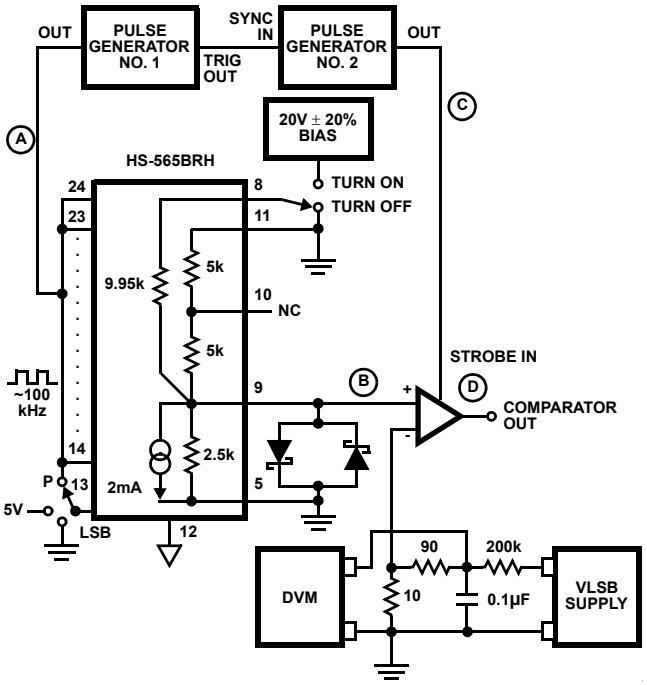


FIGURE 4A.

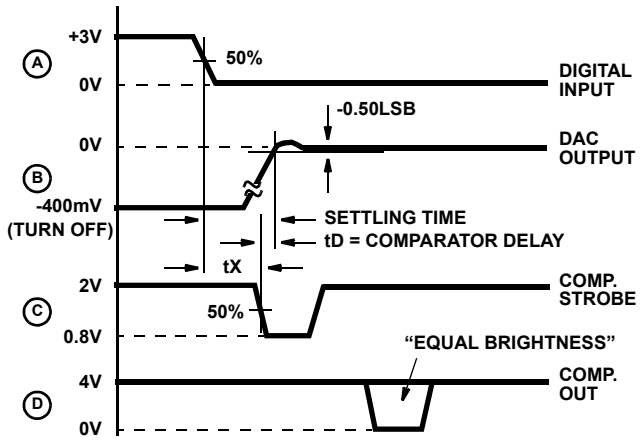


FIGURE 4B.

Other Considerations

Grounds

The HS-565BRH, HS-565BEH has two ground terminals, pin 5 (REF GND) and pin 12 (PWR GND). These should not be tied together near the package unless that point is also the system signal ground to which all returns are connected. (If such a point exists, then separate paths are required to pins 5 and 12).

The current through pin 5 is near zero DC (Note); but pin 12 carries up to 1.75mA of code - dependent current from bits 1, 2, and 3. The general rule is to connect pin 5 directly to the system "quiet" point, usually called signal or analog ground. Connect pin 12 to the local digital or power ground. Then, of course, a single path must connect the analog/signal and digital/power grounds.

NOTE: Current cancellation is a two step process within the HS-565BRH, HS-565BEH in which code dependent variations are eliminated, the resulting DC current is supplied internally. First an auxiliary 9-bit R-2R ladder is driven by the complement of the DACs input code. Together, the main and auxiliary ladders draw a continuous 2.25mA from the internal ground node, regardless of input code. Part of the DC current is supplied by the zener voltage reference, and the remainder is sourced from the positive supply via a current mirror which is laser trimmed for zero current through the external terminal (pin 5).

Layout

Connections to pin 9 (IOUT) on the HS-565BRH, HS-565BEH are most critical for high speed performance. Output capacitance of the DAC is only 20pF, so a small change of additional capacitance may alter the op amp's stability and affect settling time. Connections to pin 9 should be short and few. Component leads should be short on the side connecting to pin 9 (as for feedback capacitor C). See the "Settling Time" section on page 5.

Bypass Capacitors

Power supply bypass capacitors on the op amp will serve the HS-565BRH, HS-565BEH also. If no op amp is used, a 0.01µF ceramic capacitor from each supply terminal to pin 12 is sufficient, since supply current variations are small.

Die Characteristics

DIE DIMENSIONS:

179 mils x 107 mils x 19 mils

INTERFACE MATERIALS:

Glassivation:

Type: AlCu
Thickness: 8kÅ ±1kÅ

Top Metallization:

Type: Al/Copper
Thickness: 16kÅ ±2kÅ

Substrate:

Bipolar DI,

Backside Finish:

Silicon

ASSEMBLY RELATED INFORMATION

Substrate Potential:

Tie Substrate to VREF GND

ADDITIONAL INFORMATION:

Worst Case Current Density:

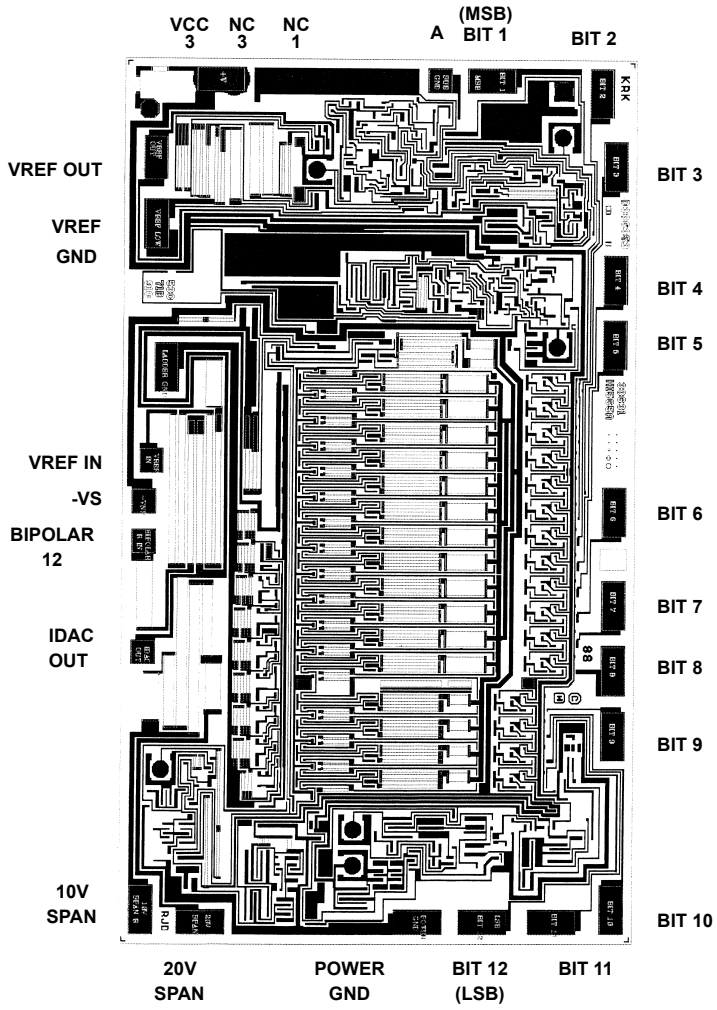
2.0×10^5 A/cm^2

Transistor Count:

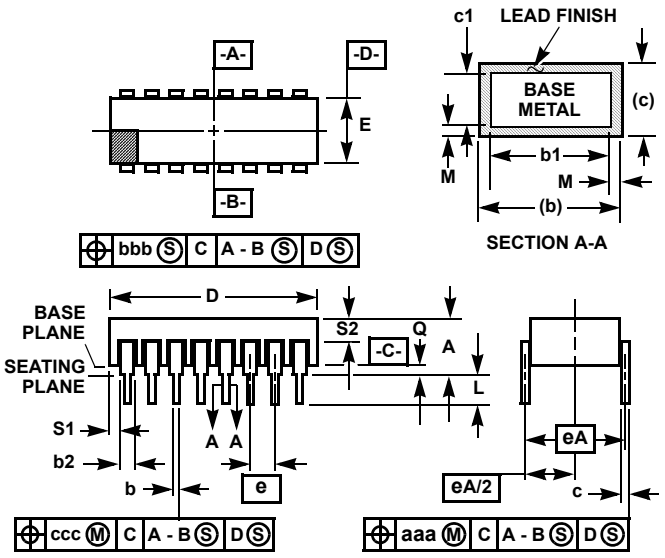
200

Metallization Mask Layout

HS-565BRH, HS-565BEH



Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

D24.6 MIL-STD-1835 CDIP2-T24 (D-3, CONFIGURATION C)
24 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.290	-	32.77	-
E	0.500	0.610	12.70	15.49	-
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.120	0.200	3.05	5.08	-
Q	0.015	0.075	0.38	1.91	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	24		24		8

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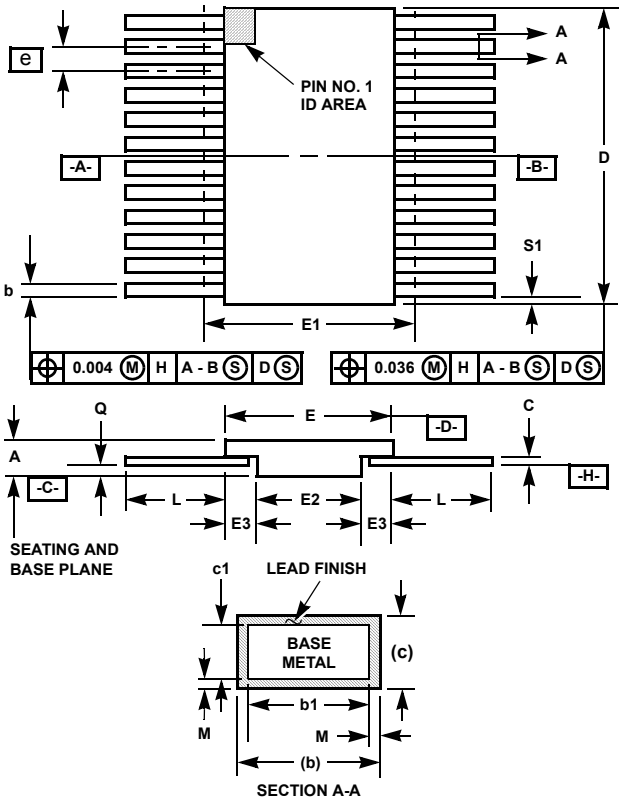
Ceramic Metal Seal Flatpack Packages (Flatpack)



K24.A MIL-STD-1835 CDFP4-F24 (F-6A, CONFIGURATION B)
24 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.640	-	16.26	3
E	0.350	0.420	9.14	10.67	-
E1	-	0.450	-	11.43	3
E2	0.180	-	4.57	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	24		24		-

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NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.