

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT138**

**3-to-8 line decoder/demultiplexer;  
inverting**

Product specification  
File under Integrated Circuits, IC06

September 1993

## 3-to-8 line decoder/demultiplexer; inverting

## 74HC/HCT138

## FEATURES

- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active LOW mutually exclusive outputs
- Output capability: standard
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT138 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT138 decoders accept three binary weighted address inputs (A<sub>0</sub>, A<sub>1</sub>, A<sub>2</sub>) and when enabled, provide 8 mutually exclusive active LOW outputs ( $\bar{Y}_0$  to  $\bar{Y}_7$ ).

The "138" features three enable inputs: two active LOW ( $\bar{E}_1$  and  $\bar{E}_2$ ) and one active HIGH (E<sub>3</sub>). Every output will be HIGH unless  $\bar{E}_1$  and  $\bar{E}_2$  are LOW and E<sub>3</sub> is HIGH.

This multiple enable function allows easy parallel expansion of the "138" to a 1-of-32 (5 lines to 32 lines) decoder with just four "138" ICs and one inverter.

The "138" can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

The "138" is identical to the "238" but has inverting outputs.

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to $\bar{Y}_n$	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	12	17	ns
t <sub>PHL</sub> / t <sub>PLH</sub>	E <sub>3</sub> to $\bar{Y}_n$ $\bar{E}_n$ to $\bar{Y}_n$		14	19	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	67	67	pF

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> – 1.5 V

## ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	$A_0$ to $A_2$	address inputs
4, 5	$\bar{E}_1, \bar{E}_2$	enable inputs (active LOW)
6	$E_3$	enable input (active HIGH)
8	GND	ground (0 V)
15, 14, 13, 12, 11, 10, 9, 7	$\bar{Y}_0$ to $\bar{Y}_7$	outputs (active LOW)
16	$V_{CC}$	positive supply voltage

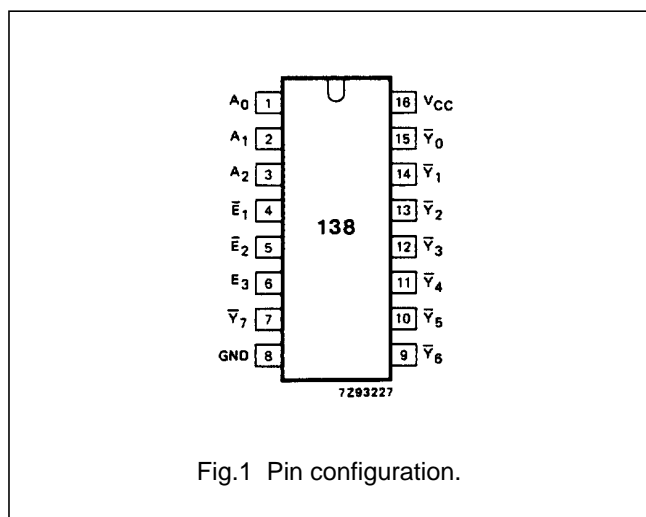


Fig.1 Pin configuration.

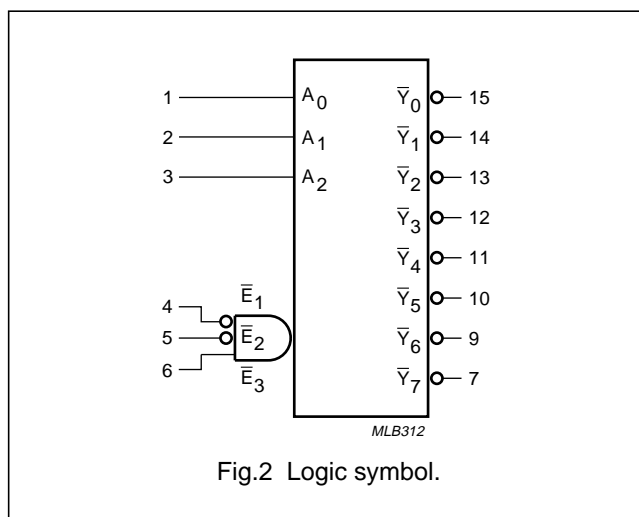


Fig.2 Logic symbol.

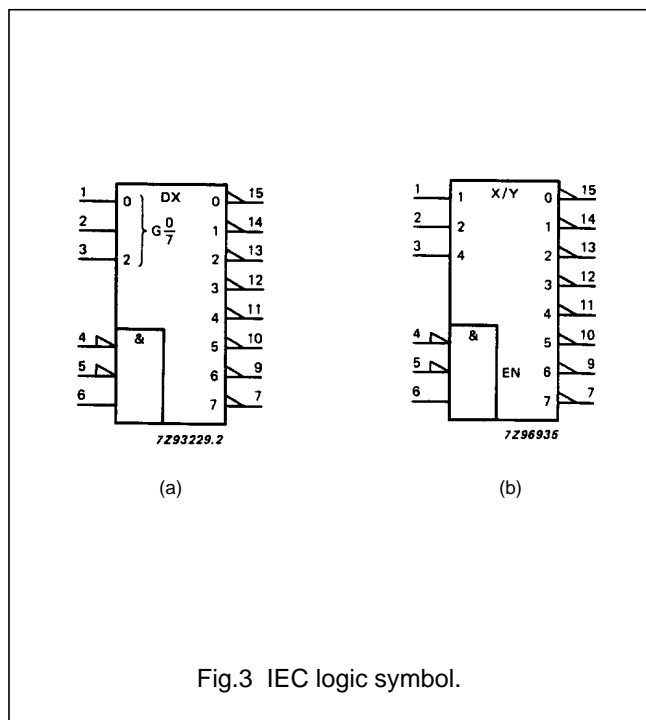


Fig.3 IEC logic symbol.

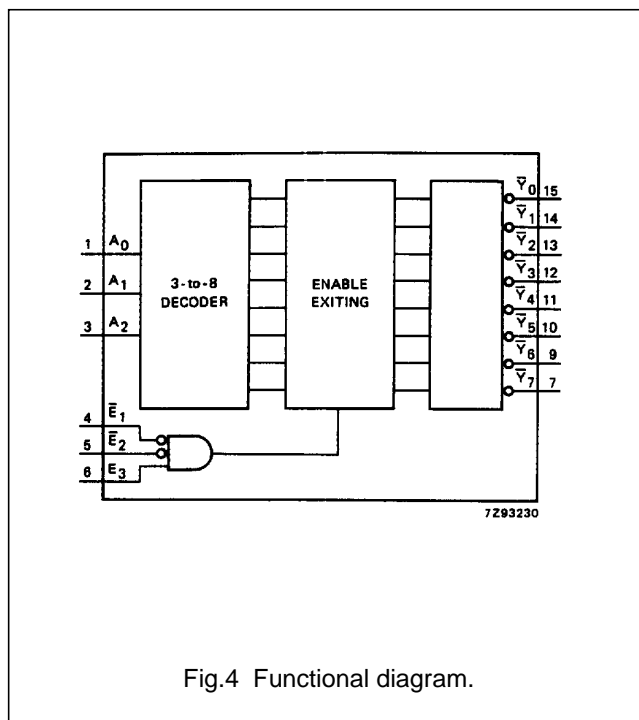


Fig.4 Functional diagram.

3-to-8 line decoder/demultiplexer; inverting

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FUNCTION TABLE

INPUTS						OUTPUTS							
$\bar{E}_1$	$\bar{E}_2$	$E_3$	$A_0$	$A_1$	$A_2$	$\bar{Y}_0$	$\bar{Y}_1$	$\bar{Y}_2$	$\bar{Y}_3$	$\bar{Y}_4$	$\bar{Y}_5$	$\bar{Y}_6$	$\bar{Y}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

Notes

- H = HIGH voltage level  
L = LOW voltage level  
X = don't care

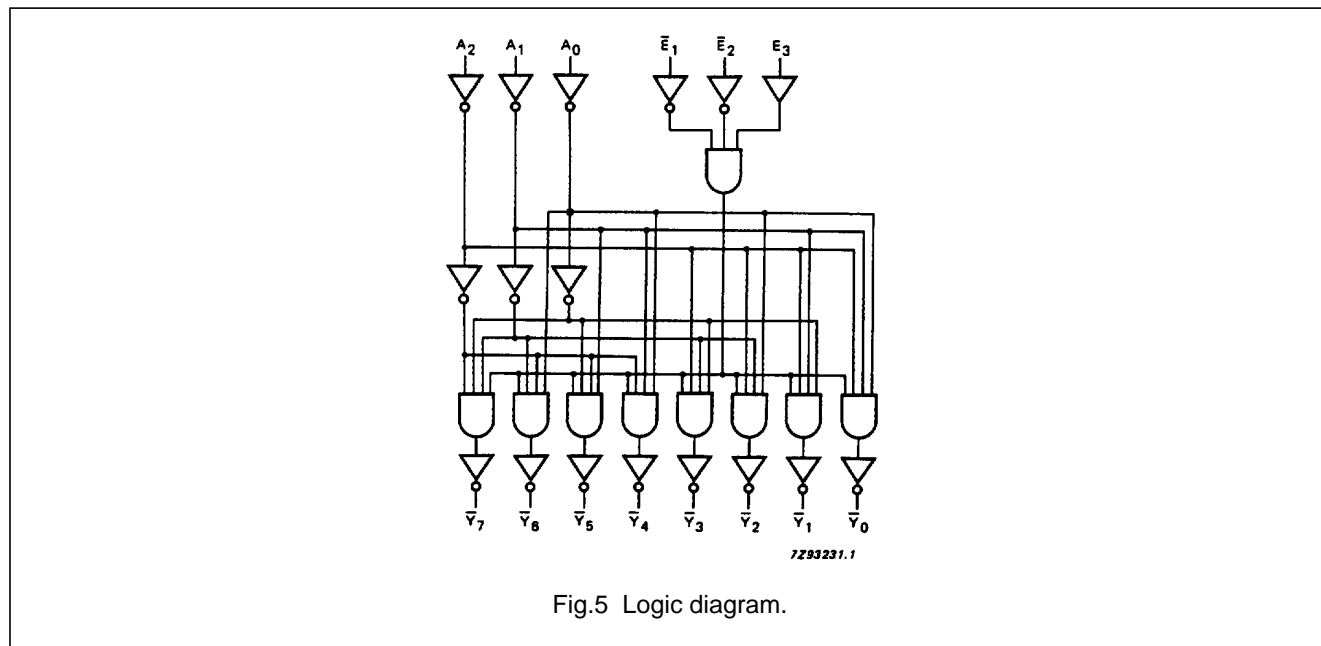


Fig.5 Logic diagram.

## 3-to-8 line decoder/demultiplexer; inverting

## 74HC/HCT138

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to $\bar{Y}_n$		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay E <sub>3</sub> to $\bar{Y}_n$		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\bar{E}_n$ to $\bar{Y}_n$		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

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## 74HC/HCT138

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A <sub>n</sub>	1.50
$\bar{E}_n$	1.25
E <sub>3</sub>	1.00

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to $\bar{Y}_n$		20	35		44		53	ns	4.5	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay E <sub>3</sub> to $\bar{Y}_n$		18	40		50		60	ns	4.5	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\bar{E}_n$ to $\bar{Y}_n$		19	40		50		60	ns	4.5	Fig.7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

3-to-8 line decoder/demultiplexer; inverting

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AC WAVEFORMS

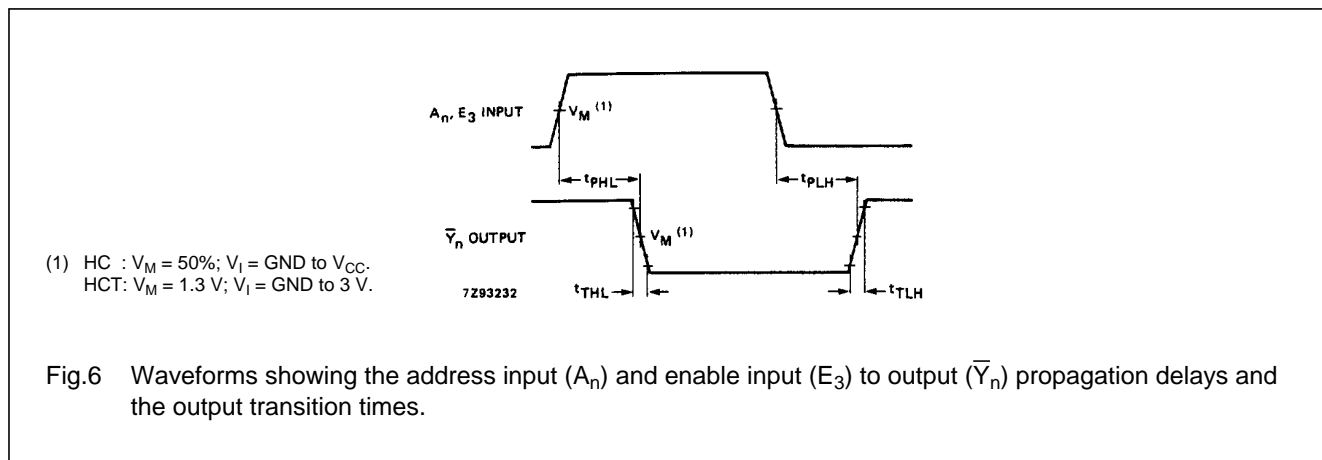


Fig.6 Waveforms showing the address input ( $A_n$ ) and enable input ( $E_3$ ) to output ( $\bar{Y}_n$ ) propagation delays and the output transition times.

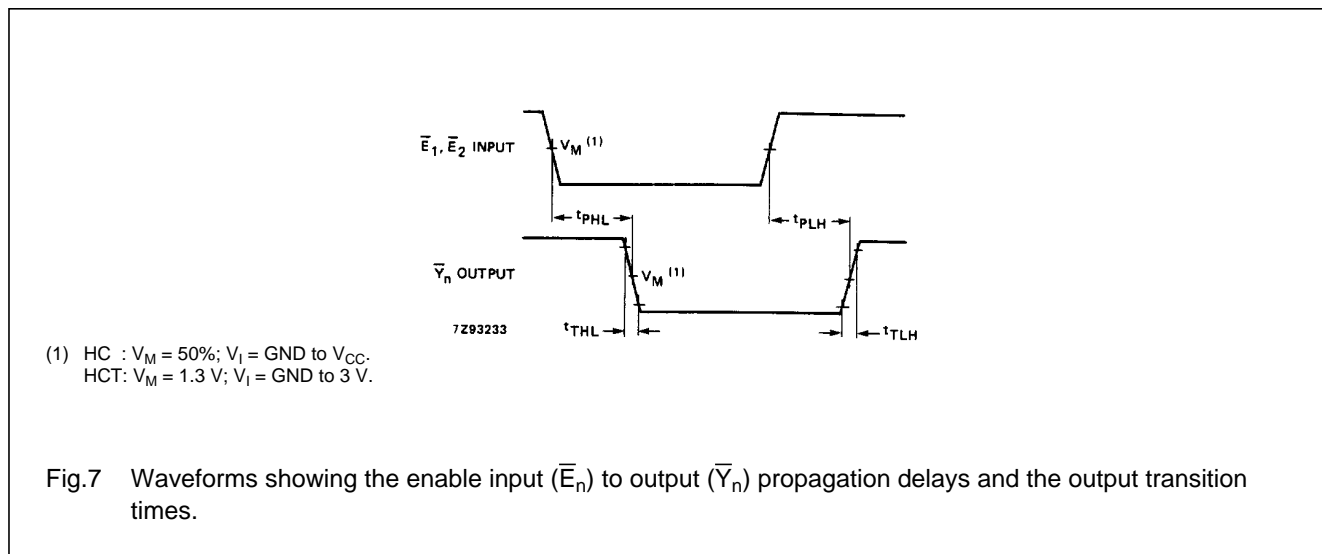


Fig.7 Waveforms showing the enable input ( $\bar{E}_n$ ) to output ( $\bar{Y}_n$ ) propagation delays and the output transition times.

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".

Product Information

# 74HC/HCT138; 3-to-8 line decoder/demultiplexer; inverting

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## General description

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The '138' features three enable inputs: two active LOW ( $E_1$  and  $E_2$ ) and one active HIGH ( $E_3$ ). Every output will be HIGH unless  $E_1$  and  $E_2$  are LOW and  $E_3$  is HIGH.

This multiple enable function allows easy parallel expansion of the '138' to a 1-of-32 (5 lines to 32 lines) decoder with just four '138' ICs and one inverter.

The '138' can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

The '138' is identical to the '238' but has inverting outputs.

## Features

- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active LOW mutually exclusive outputs
- Output capability: standard
- $I_{CC}$  category: MSI

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## Datasheet



<u>Datasheet title</u>	<u>Publication release date</u>	<u>Datasheet status</u>	<u>Page count</u>	<u>File size (kB)</u>	<u>Datasheet</u>
74HC/HCT138; 3-to-8 line decoder/demultiplexer; inverting	01-Sep-93	Product specification	7	47	<a href="#">PDF</a> <a href="#">Download</a>

### Additional datasheet info












To complete the device datasheet with package and family information, also download the following PDF files. The "Logic Package Information" document is required to determine in which package(s) this device is available.

Document	Description
1 <a href="#">PDF</a> <a href="#">HCT_FAMILY_SPECIFICATIONS</a>	HC/T Family Specifications, The IC06 74HC/HCT/HCMOS Logic Family Specifications
2 <a href="#">PDF</a> <a href="#">HCT_PACKAGE_INFO</a>	HC/T Package Info, The IC06 74HC/HCT/HCMOS Logic Package Information
3 <a href="#">PDF</a> <a href="#">HCT_PACKAGE_OUTLINES</a>	HC/T Package Outlines, The IC06 74HC/HCT/HCMOS Logic Package Outlines

## Parametrics

Type number	Package	Description	Propagation Delay(ns)	Voltage	No. of Pins	Power Dissipation Considerations	Logic Switching Levels	Output Drive Capability
74HC138BQ	SOT763	3-to-8 Line Decoder/Demultiplexer; Inverting	12@5V	2.0-6.0 V	16	Low Power or Battery Applications	CMOS	+/- 5.2 mA
74HC138D	<a href="#">SOT109-1</a> (SO16) 	3-to-8 Line Decoder/Demultiplexer; Inverting	12@5V	2.0-6.0 V	16	Low Power or Battery Applications	CMOS	+/- 5.2 mA
74HC138DB	<a href="#">SOT338-1</a> (SSOP16)	3-to-8 Line Decoder/Demultiplexer; Inverting	12@5V	2.0-6.0 V	16	Low Power or Battery Applications	CMOS	+/- 5.2 mA
74HC138N	<a href="#">SOT38-4</a> (DIP16)	3-to-8 Line Decoder/Demultiplexer; Inverting	12@5V	2.0-6.0 V	16	Low Power or Battery Applications	CMOS	+/- 5.2 mA
74HC138PW	<a href="#">SOT403-1</a> (TSSOP16)	3-to-8 Line Decoder/Demultiplexer; Inverting	12@5V	2.0-6.0 V	16	Low Power or Battery Applications	CMOS	+/- 5.2 mA
74HCT138D	<a href="#">SOT109-1</a> (SO16) 	3-to-8 Line Decoder/Demultiplexer; Inverting; TTL Enabled	17	4.5-5.5 V	16	Low Power	TTL	+/- 4 mA
74HCT138DB	<a href="#">SOT338-1</a> (SSOP16)	3-to-8 Line Decoder/Demultiplexer; Inverting; TTL Enabled	17	4.5-5.5V	16	Low Power	TTL	+/- 4 mA
74HCT138N	<a href="#">SOT38-4</a> (DIP16)	3-to-8 Line Decoder/Demultiplexer; Inverting; TTL Enabled	17	4.5-5.5V	16	Low Power	TTL	+/- 4 mA
74HCT138PW	<a href="#">SOT403-1</a> (TSSOP16)	3-to-8 Line Decoder/Demultiplexer; Inverting; TTL Enabled	17	4.5-5.5V	16	Low Power	TTL	+/- 4 mA

## Products, packages, availability and ordering

<u>Type number</u>	<u>North American type number</u>	<u>Ordering code (12NC)</u>	<u>Marking/Packing</u> <a href="#">PDF IC packing info</a>	<u>Package</u>	<u>Product status</u>	<u>Buy online</u>
74HC138BQ		9352 737 78115	Standard Marking * Reel Pack, SMD, 7"	<a href="#">SOT763</a>	Full production	-
74HC138D	74HC138D	9337 134 00652	Standard Marking * Tube, CECC	<a href="#">SOT109-1 (SO16)</a> 	Full production	<a href="#">BUY ONLINE</a> 
	74HC138D-T	9337 134 00653	Standard Marking * Reel Pack, SMD, 13", CECC	<a href="#">SOT109-1 (SO16)</a> 	Full production	<a href="#">BUY ONLINE</a> 
74HC138DB	74HC138DB	9351 744 10112	Standard Marking * Tube	<a href="#">SOT338-1 (SSOP16)</a>	Full production	<a href="#">BUY ONLINE</a> 
	74HC138DB-T	9351 744 10118	Standard Marking * Reel Pack, SMD, 13"	<a href="#">SOT338-1 (SSOP16)</a>	Full production	<a href="#">BUY ONLINE</a> 
74HC138N	74HC138N	9336 692 90652	Standard Marking * Tube, CECC	<a href="#">SOT38-4 (DIP16)</a>	Full production	<a href="#">BUY ONLINE</a> 
74HC138PW	74HC138PW	9351 743 80112	Standard Marking * Tube	<a href="#">SOT403-1 (TSSOP16)</a>	Full production	<a href="#">BUY ONLINE</a> 
	74HC138PW-T	9351 743 80118	Standard Marking * Reel Pack, SMD, 13"	<a href="#">SOT403-1 (TSSOP16)</a>	Full production	<a href="#">BUY ONLINE</a> 
74HCT138BQ		9352 744 71115	Standard Marking * Reel Pack, SMD, 7"	<a href="#">SOT763</a>	Full production	-
74HCT138D	74HCT138D	9337 134 10652	Standard Marking * Tube, CECC	<a href="#">SOT109-1 (SO16)</a> 	Full production	<a href="#">BUY ONLINE</a> 
	74HCT138D-T	9337 134 10653	Standard Marking * Reel Pack, SMD, 13", CECC	<a href="#">SOT109-1 (SO16)</a> 	Full production	<a href="#">BUY ONLINE</a> 
74HCT138DB	74HCT138DB	9351 744 20112	Standard Marking * Tube	<a href="#">SOT338-1 (SSOP16)</a>	Full production	<a href="#">BUY ONLINE</a> 
	74HCT138DB-T	9351 744 20118	Standard Marking * Reel Pack, SMD, 13"	<a href="#">SOT338-1 (SSOP16)</a>	Full production	<a href="#">BUY ONLINE</a> 
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74HCT138PW	74HCT138PW	9351 873 20112	Standard Marking * Tube	<a href="#">SOT403-1 (TSSOP16)</a>	Full production	<a href="#">BUY ONLINE</a> 
	74HCT138PW-T	9351 873 20118	Standard Marking * Reel Pack, SMD, 13"	<a href="#">SOT403-1 (TSSOP16)</a>	Full production	<a href="#">BUY ONLINE</a> 

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[→ MORE 74HC/HCT138](#) links to the similar products page containing an overview of products that are similar in function or related to the type number(s) as listed on this page. The similar products page includes products from the same catalog tree(s), relevant selection guides and products from the same functional category.

## Support & tools

[→ PDF HC/T Family Specifications, The IC06 74HC/HCT/HCMOS Logic Family Specifications](#)(date 1998-03-01)

[→ PDF HC/T User Guide](#)(date 1997-11-01)

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