SDLS011

SN54LS112A, SN54S112, SN74LS112A, SN74S112A
DUAL J-K NEGATIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH PRESET AND CLEAR
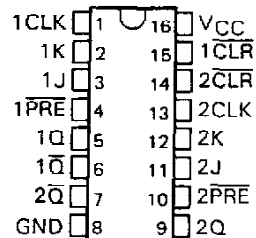
D2661, APRIL 1982—REVISED MARCH 1988

- **Fully Buffered to Offer Maximum Isolation from External Disturbance**

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs**

- **Dependable Texas Instruments Quality and Reliability**
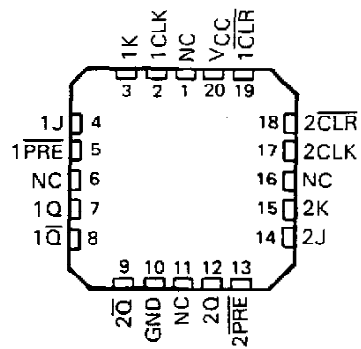
description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset and clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54LS112A and SN54S112 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS112A and SN74S112A are characterized for operation from 0°C to 70°C.

SN54LS112A, SN54S112 . . . J OR W PACKAGE
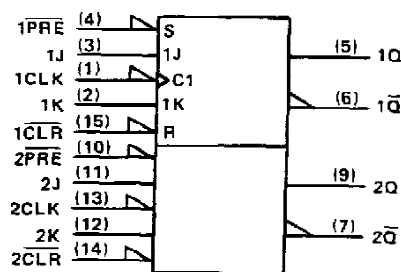SN74LS112A, SN74S112A . . . D OR N PACKAGE
(TOP VIEW)

1CLK	1	16	V_{CC}
1K	2	15	1$\overline{CLR}$
1J	3	14	2$\overline{CLR}$
1$\overline{PRE}$	4	13	2CLK
1Q	5	12	2K
1$\overline{Q}$	6	11	2J
2Q	7	10	2$\overline{PRE}$
GND	8	9	2$\overline{Q}$

SN54LS112A, SN54S112 . . . FK PACKAGE
(TOP VIEW)

	1K	1CLK	NC	V_{CC}	1$\overline{CLR}$	
	3	2	1	20	19	
1J	4					18	2$\overline{CLR}$
1$\overline{PRE}$	5					17	2CLK
NC	6					16	NC
1Q	7					15	2K
1$\overline{Q}$	8					14	2J
	9	10	11	12	13	
	2$\overline{Q}$	GND	NC	2Q	2$\overline{PRE}$	

NC—No internal connection

logic symbol[‡]

1$\overline{PRE}$	(4)	S
1J	(3)	1J
1CLK	(1)	C1
1K	(2)	1K
1$\overline{CLR}$	(15)	R
2$\overline{PRE}$	(10)	
2J	(11)	
2CLK	(13)	
2K	(12)	
2$\overline{CLR}$	(14)	

(5)	1Q
(6)	1$\overline{Q}$
(9)	2Q
(7)	2$\overline{Q}$

[‡]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

FUNCTION TABLE (each flip-flop)

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H[†]	H[†]
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

[†] The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at preset and clear are near V_{IL} minimum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

TEXAS INSTRUMENTS

logic diagrams (positive logic)
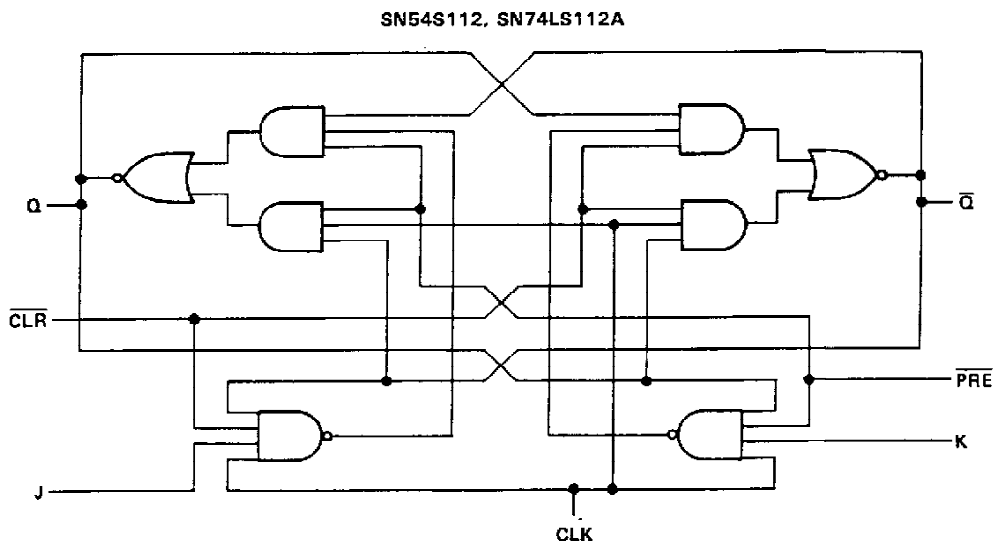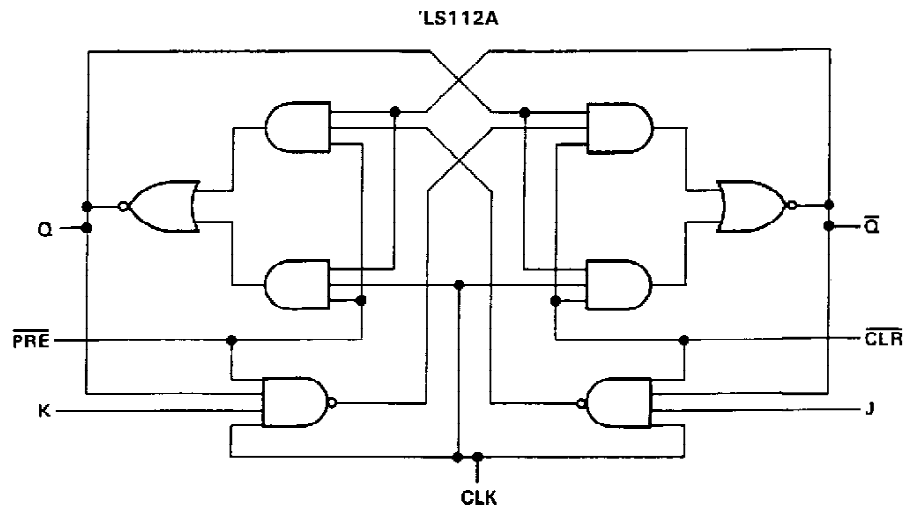
'LS112A

SN54S112, SN74LS112A

schematics of inputs and outputs

'LS112A

I_{IL} MAX	R_{eq} NOM
−0.4 mA	30 kΩ
−0.8 mA	8.25 kΩ

SN54S112, SN74S112A

I_{IL} MAX	R_{eq} NOM
−1.6 mA	4 kΩ
−4 mA	1.4 kΩ
−7 mA	900 Ω

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V

Input voltage: 'LS112A . . . . 7 V

               SN54LS112, SN74LS112A . . . . 5.5 V

Operating free-air temperature range: SN54' . . . . −55°C to 125°C

                                  SN74' . . . . 0°C to 70°C

Storage temperature range . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54LS112A			SN74LS112A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		30	0		30	MHz
t_w	Pulse duration	CLK high	20			20			ns
		$\overline{PRE}$ or $\overline{CLR}$ low	25			25			
t_{su}	Set up time-before CLK↓	Data high or low	20			20			ns
		$\overline{CLR}$ inactive	25			25			
		$\overline{PRE}$ inactive	20			20			
t_h	Hold time-data after CLK↓		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]	SN54LS112A			SN74LS112A			UNIT
			MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX, I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V, I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V, I_{OL} = 8 mA					0.35	0.5	
I_I	J or K	V_{CC} = MAX, V_I = 7 V			0.1			0.1	mA
	$\overline{CLR}$ or $\overline{PRE}$				0.3			0.3	
	CLK				0.4			0.4	
I_{IH}	J or K	V_{CC} = MAX, V_I = 2.7 V			20			20	µA
	$\overline{CLR}$ or $\overline{PRE}$				60			60	
	CLK				80			80	
I_{IL}	J or K	V_{CC} = MAX, V_I = 0.4 V			−0.4			−0.4	mA
	All other				−0.8			−0.8	
I_{OS}[§]		V_{CC} = MAX, see Note 2	−20		−100	−20		−100	mA
I_{CC} (Total)		V_{CC} = MAX, see Note 3		4	6		4	6	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

NOTES: 2. For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the '54 family and the '74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

3. With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}			R_L = 2 kΩ,	C_L = 15 pF	30	45		MHz
t_{PLH}	$\overline{CLR}$, $\overline{PRE}$ or CLK	Q or $\overline{Q}$				15	20	ns
t_{PHL}						15	20	ns

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

			SN54S112			SN74S112A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1			−1	mA
I_{OL}	Low-level output current				20			20	mA
t_w	Pulse duration	CLK high	6			6			ns
		CLK low	6.5			6.5			
		$\overline{PRE}$ or $\overline{CLR}$ low	8			8			
t_{su}	Set up time-before CLK↓	Data high or low	7			7			ns
t_h	Hold time-data after CLK↓		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]			SN54S112			SN74S112A			UNIT
					MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX, I_{OH} = −1 mA			2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA					0.5			0.5	V
I_I		V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	J or K	V_{CC} = MAX,	V_I = 2.7 V				50			50	µA
	All other						100			100	
I_{IL}	J or K	V_{CC} = MAX,	V_I = 0.5 V				−1.6			−1.6	mA
	$\overline{CLR}$[§]						−7			−7	
	$\overline{PRE}$[§]						−7			−7	
	CLK						−4			−4	
I_{OS}[¶]		V_{CC} = MAX			−40		−100	−40		−100	mA
I_{CC}[#]		V_{CC} = MAX,	see Note 3			15	25		15	25	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
[‡] All typical values are at V_{CC} = 5 V, T_A = 25 °C.
[§] Clear is tested with preset high and preset is tested with clear high.
[¶] Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.
[#] Values are average per flip-flop.
NOTE 3: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				80	125		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	R_L = 280 Ω, C_L = 15 pF		4	7	ns
t_{PHL}	$\overline{PRE}$ or $\overline{CLR}$ (CLK high)	$\overline{Q}$ or Q			5	7	ns
	$\overline{PRE}$ or $\overline{CLR}$ (CLK low)				5	7	
t_{PLH}	CLK	Q or $\overline{Q}$			4	7	ns
t_{PHL}					5	7	ns

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

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PRODUCT SUPPORT: TRAINING

SN74S112A, Dual J-K Negative-Edge-Triggered Flip-Flops With Clear And Preset
DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN74S112A
Voltage Nodes (V)	5
Vcc range (V)	4.75 to 5.25
Input Level	TTL
Output Level	TTL
Output Drive (mA)	-1/20
Output	2S
No. of Bits	2
th (ns)	0
tpd max (ns)	7
tsu (ns)	7

FEATURES   ▲Back to Top

- Fully Buffered to Offer Maximum Isolation from External Disturbance
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

DESCRIPTION   ▲Back to Top

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset and clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54LS112A and SN54S112 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LS112A and SN74S112A are characterized for operation from 0°C to 70°C.

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DATASHEET   ▲Back to Top
Full datasheet in Acrobat PDF: sn74s112a.pdf (300 KB) (Updated: 03/01/1988)

View Application Notes for Digital Logic

- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- Live Insertion (SDYA012 - Updated: 10/01/1996)

View Related Documentation for Digital Logic

- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- Logic Selection Guide Second Half 2002 (Rev. R) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- Military Semiconductors Selection Guide 2002 (Rev. B) (SGYC003B, 1648 KB - Updated: 04/22/2002)

PRICING/AVAILABILITY/PKG ▲Back to Top

	DEVICE INFORMATION							TI INVENTORY STATUS AS OF 3:00 PM GMT, 26 Sep 2002			REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE|PINS	TEMP (ºC)	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY		IN STOCK	IN PROGRESS QTY|DATE	LEAD TIME	DISTRIBUTOR COMPANY|REGION	IN STOCK	PURCHASE
SN74S112AD	OBSOLETE	SOP (D) | 16	0 TO 70	View Contents	1KU |			N/A*		Not Available			
SN74S112ADR	ACTIVE	SOP (D) | 16	0 TO 70	View Contents	1KU | 0.43	2500		N/A*	>10k | 10 Oct	5 WKS			
SN74S112AN	ACTIVE	PDIP (N) | 16	0 TO 70	View Contents	1KU | 0.43	25		N/A*	40 | 23 Sep	5 WKS	Avnet | AMERICA	150	BUY NOW
									1250 | 24 Sep				
									3724 | 04 Oct				
									>10k | 09 Oct				
									633 | 16 Oct				
SN74S112AN3	OBSOLETE	PDIP (N) | 16	0 TO 70	View Contents	1KU |			N/A*		Not Available			
SN74S112ANSR	ACTIVE	SOP (NS) | 16		View Contents	1KU | 0.43	2000		N/A*	705 | 23 Sep	5 WKS			
									2000 | 03 Oct				
									4949 | 04 Oct				
									2302 | 11 Oct				
									>10k | 18 Oct				

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PRODUCT SUPPORT: TRAINING

SN74LS112A, Dual J-K Negative-Edge-Triggered Flip-Flops With Clear And Preset
DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54LS112A	SN74LS112A
Voltage Nodes (V)	5	5
Vcc range (V)	4.5 to 5.5	4.75 to 5.25
Input Level	TTL	TTL
Output Level	TTL	TTL
Output Drive (mA)		-0.4/8
Output	2S	2S
No. of Bits	2	2
th (ns)		0
tpd max (ns)		20
tsu (ns)		20

| **FEATURES** | ▲Back to Top |

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| **DESCRIPTION** | ▲Back to Top |

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| **DATASHEET** | ▲Back to Top |

Full datasheet in Acrobat PDF: <u>sn74ls112a.pdf</u> (300 KB) (Updated: 03/01/1988)

APPLICATION NOTES

View Application Notes for <u>Digital Logic</u>

- <u>Designing With Logic (Rev. C)</u> (SDYA009C - Updated: 06/01/1997)
- <u>Designing with the SN54/74LS123 (Rev. A)</u> (SDLA006A - Updated: 03/01/1997)
- <u>Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits</u> (SZZA026 - Updated: 06/20/2001)
- <u>Input and Output Characteristics of Digital Integrated Circuits</u> (SDYA010 - Updated: 10/01/1996)
- <u>Live Insertion</u> (SDYA012 - Updated: 10/01/1996)

RELATED DOCUMENTS

View Related Documentation for <u>Digital Logic</u>

- <u>Logic Reference Guide</u> (SCYB004, 1032 KB - Updated: 10/23/2001)
- <u>Logic Selection Guide Second Half 2002 (Rev. R)</u> (SDYU001R, 4274 KB - Updated: 07/19/2002)
- <u>Military Semiconductors Selection Guide 2002 (Rev. B)</u> (SGYC003B, 1648 KB - Updated: 04/22/2002)

PRICING/AVAILABILITY/PKG

	DEVICE INFORMATION							TI INVENTORY STATUS AS OF 3:00 PM GMT, 26 Sep 2002			REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE|PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY		IN STOCK	IN PROGRESS QTY|DATE	LEAD TIME	DISTRIBUTOR COMPANY|REGION	IN STOCK	PURCHASE
SN74LS112AD	ACTIVE	SOP (D) | 16	0 TO 70	View Contents	1KU | 0.42	40		N/A*	7640 | 19 Sep	4 WKS	Avnet | AMERICA	>1k	BUY NOW
									1114 | 03 Oct				
									>10k | 10 Oct				
SN74LS112ADR	ACTIVE	SOP (D) | 16	0 TO 70	View Contents	1KU | 0.45	2500		N/A*	1112 | 03 Oct	4 WKS			
									>10k | 10 Oct				
SN74LS112AN	ACTIVE	PDIP (N) | 16	0 TO 70	View Contents	1KU | 0.42	25		N/A*	2000 | 30 Sep	4 WKS	Avnet | AMERICA	>1k	BUY NOW
									>10k | 02 Oct		DigiKey | AMERICA	375	BUY NOW
									>10k | 04 Oct				
SN74LS112AN3	OBSOLETE	PDIP (N) | 16	0 TO 70	View Contents	1KU |			N/A*		Not Available			
SN74LS112ANSR	ACTIVE	SOP (NS) | 16		View Contents	1KU | 0.42	2000		N/A*	>10k | 04 Oct	4 WKS			

Table Data Updated on: 9/26/2002