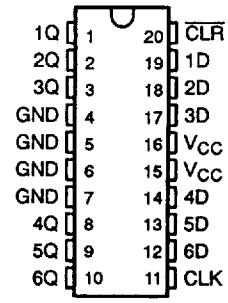
D3434, MARCH 1990 – REVISED APRIL 1993

- **Applications Include: Buffer/Storage Registers, Shift Registers, Pattern Generators**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin $V_{CC}$ and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

**DW OR N PACKAGE**
**(TOP VIEW)**




## description

This device contains six D-type flip-flops and is positive-edge-triggered with a direct clear input. Information at the D inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

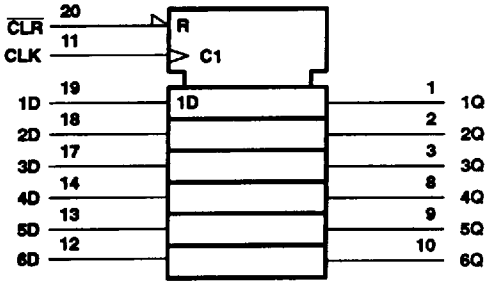
The 74AC11174 is characterized for operation from – 40°C to 85°C.

**FUNCTION TABLE**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{CLR}$ | CLK | D | Q |
| L | X | X | L |
| H | ↑ | H | H |
| H | ↑ | L | L |
| H | L | X | $Q_0$ |

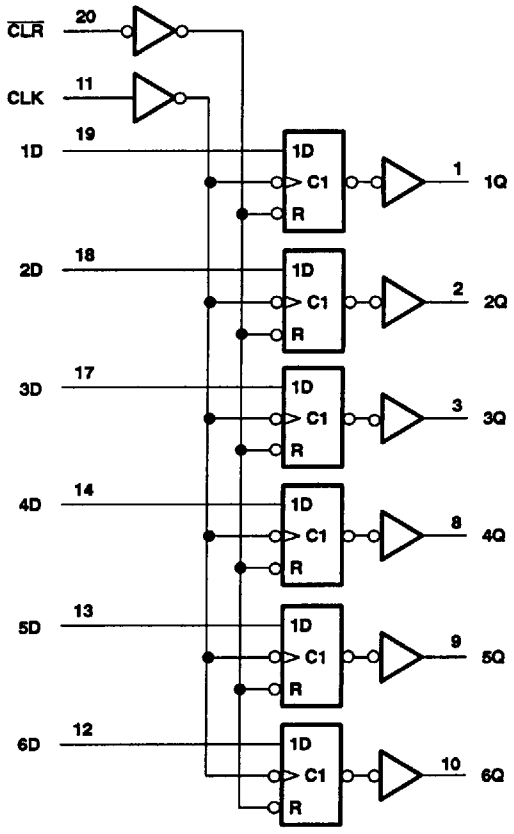
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

| | |
|---|---|
| Supply voltage range, $V_{CC}$ | −0.5 V to 7 V |
| Input voltage range, $V_I$ (see Note 1) | −0.5 V to $V_{CC}$ + 0.5 V |
| Output voltage range, $V_O$ (see Note 1) | −0.5 V to $V_{CC}$ + 0.5 V |
| Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{CC}$) | ±20 mA |
| Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) | ±50 mA |
| Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) | ±50 mA |
| Continuous current through $V_{CC}$ or GND | ±150 mA |
| Storage temperature range | −65°C to 150°C |

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

## recommended operating conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 3 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 3 V | 2.1 | | | V |
| | | $V_{CC}$ = 4.5 V | 3.15 | | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 3 V | | | 0.9 | V |
| | | $V_{CC}$ = 4.5 V | | | 1.35 | |
| | | $V_{CC}$ = 5.5 V | | | 1.65 | |
| $V_I$ | Input voltage | | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 3 V | | | −4 | mA |
| | | $V_{CC}$ = 4.5 V | | | −24 | |
| | | $V_{CC}$ = 5.5 V | | | −24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 3 V | | | 12 | mA |
| | | $V_{CC}$ = 4.5 V | | | 24 | |
| | | $V_{CC}$ = 5.5 V | | | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 0 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | −40 | | 85 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | TA = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | | |
| $V_{OH}$ | $I_{OH}$ = −50 μA | 3 V | 2.9 | | | 2.9 | | V |
| | | 4.5 V | 4.4 | | | 4.4 | | |
| | | 5.5 V | 5.4 | | | 5.4 | | |
| | $I_{OH}$ = −4 mA | 3 V | 2.58 | | | 2.48 | | |
| | $I_{OL}$ = −24 mA | 4.5 V | 3.94 | | | 3.8 | | |
| | | 5.5 V | 4.94 | | | 4.8 | | |
| | $I_{OH}$ = −75 mA† | 5.5 V | | | | 3.85 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 3 V | | | 0.1 | | 0.1 | V |
| | | 4.5 V | | | 0.1 | | 0.1 | |
| | | 5.5 V | | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 12 mA | 3 V | | | 0.36 | | 0.44 | |
| | $I_{OL}$ = 24 mA | 4.5 V | | | 0.36 | | 0.44 | |
| | | 5.5 V | | | 0.36 | | 0.44 | |
| | $I_{OL}$ = 75 mA† | 5.5 V | | | | | 1.65 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 8 | | 80 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | | | | pF |

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

**timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| | | | $T_A$ = 25°C | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | | | |
| $f_{clock}$ | Clock frequency | | 0 | 80 | 0 | 80 | MHz |
| $t_w$ | Pulse duration | $\overline{CLR}$ low | 4.5 | | 4.5 | | ns |
| | | CLK high or low | 6 | | 6 | | |
| $t_{su}$ | Setup time before CLK↑ | Data | 7 | | 7 | | ns |
| | | $\overline{CLR}$ inactive | 1.5 | | 1.5 | | |
| $t_h$ | Hold time after CLK↑ | | 0 | | 0 | | ns |

**timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| | | | $T_A$ = 25°C | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | | | |
| $f_{clock}$ | Clock frequency | | 0 | 100 | 0 | 100 | MHz |
| $t_w$ | Pulse duration | $\overline{CLR}$ low | 4 | | 4 | | ns |
| | | CLK high or low | 5 | | 5 | | |
| $t_{su}$ | Setup time before CLK↑ | Data | 4.5 | | 4.5 | | ns |
| | | $\overline{CLR}$ inactive | 1.5 | | 1.5 | | |
| $t_h$ | Hold time after CLK↑ | | 0 | | 0 | | ns |

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | 80 | 105 | | 80 | | MHz |
| $t_{PHL}$ | $\overline{CLR}$ | Any Q | 3.9 | 10 | 13.5 | 3.9 | 14.8 | ns |
| $t_{PLH}$ | CLK | Any Q | 2.4 | 7.5 | 9.2 | 2.4 | 10.8 | ns |
| $t_{PHL}$ | | | 3.4 | 9.6 | 12.7 | 3.4 | 14 | |

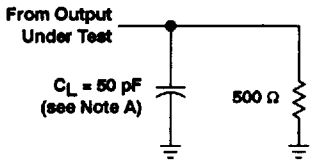
**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | 100 | 125 | | 100 | | MHz |
| $t_{PHL}$ | $\overline{CLR}$ | Any Q | 2.9 | 6.5 | 9.8 | 2.9 | 10.7 | ns |
| $t_{PLH}$ | CLK | Any Q | 2.1 | 4.9 | 6.8 | 2.1 | 7.6 | ns |
| $t_{PHL}$ | | | 2.7 | 6.2 | 9.2 | 2.7 | 10.1 | |

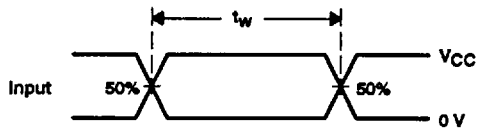
**operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C**

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | $C_L$ = 50 pF, f = 1 MHz | 29 | pF |

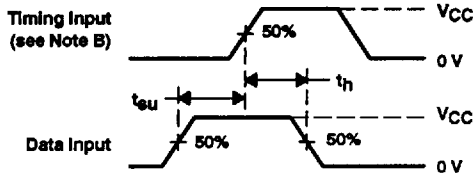
## PARAMETER MEASUREMENT INFORMATION



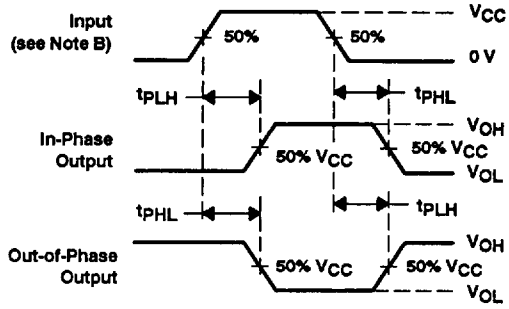

LOAD CIRCUIT




VOLTAGE WAVEFORMS




VOLTAGE WAVEFORMS




VOLTAGE WAVEFORMS

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**