DESCRIPTION

The HY62V256B-(I)/ HY62U256B-(I) is a high-speed, low power and 32,786 x 8-bits CMOS Static Random Access Memory fabricated using Hyundai's high performance CMOS process technology. It is suitable for use in low voltage operation and battery back-up application. This device has a data retention mode that guarantees data to remain valid at the minimum power supply voltage of 2.0 volt.

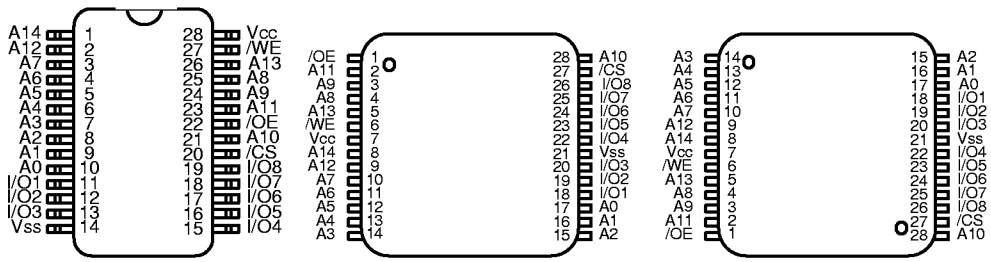
FEATURES

- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Low power consumption
- Battery backup(LL-part)
  - 2.0V(min.) data retention
- Standard pin configuration
  - 28 pin 330mil SOP
  - 28 pin 8x13.4 mm TSOP-I (Standard and Reversed)

Product No.	Voltage (V)	Speed (ns)	Operation Current(mA)	Standby Current(uA)	Temperature (¡)
HY62V256B	3.3	85/100/120	2	20	0~70(Normal)
HY62V256B-I	3.3	85/100/120	2	25	-40~85(E.T.)
HY62U256B	3.0	100/120/150	2	15	0~70(Normal)
HY62U256B-I	3.0	100/120/150	2	20	-40~85(E.T.)

Note 1. E.T. : Extended Temperature, Normal : Normal Temperature
2. Current value is max.

PIN CONNECTION

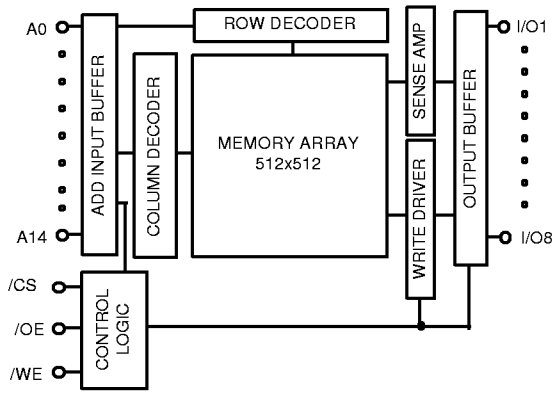


SOP TSOP-I(Standard) TSOP-I(Reversed)

PIN DESCRIPTION

Pin Name	Pin Function
/CS	Chip Select
/WE	Write Enable
/OE	Output Enable
A0 ~ A14	Address Inputs
I/O1 ~ I/O8	Data Input/Output
Vcc	Power(+3.3V or 3.0V)
Vss	Ground

BLOCK DIAGRAM



ORDERING INFORMATION

Part No.	Speed	Temp.	Package
HY62V256BLLJ	85/100/120		SOP
HY62V256BLLT1	85/100/120		TSOP-I Standard
HY62V256BLLR1	85/100/120		TSOP-I Reversed
HY62V256BLLJ-I	85/100/120	E.T.	SOP
HY62V256BLLT1-I	85/100/120	E.T.	TSOP-I Standard
HY62V256BLLR1-I	85/100/120	E.T.	TSOP-I Reversed
HY62U256BLLJ	100/120/150		SOP
HY62U256BLLT1	100/120/150		TSOP-I Standard
HY62U256BLLR1	100/120/150		TSOP-I Reversed
HY62U256BLLJ-I	100/120/150	E.T.	SOP
HY62U256BLLT1-I	100/120/150	E.T.	TSOP-I Standard
HY62U256BLLR1-I	100/120/150	E.T.	TSOP-I Reversed

ABSOLUTE MAXIMUM RATING (1)

Symbol	Parameter	Rating	Unit	Remark
Vcc, VIN, VOUT	Power Supply, Input/Output Voltage	-0.5 to 4.6	V	
TA	Operating Temperature	0 to 70	¡	HY62V256B
				HY62U256B
		-40 to 85	¡	HY62V256B-I
				HY62U256B-I
TSTG	Storage Temperature	-65 to 150	¡	
PD	Power Dissipation	1.0	W	
IOUT	Data Output Current	50	mA	
TSOLDER	Lead Soldering Temperature & Time	260•10	¡ •sec	

Note
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

TA=0°C to 70°C (Normal)/ -40°C to 85°C(E.T.)

Symbol	Parameter	Product	Min.	Type	Max.	Unit
Vcc	Power Supply Voltage	HY62V256B-(I)	3.0	3.3	3.6	V
		HY62U256B-(I)	2.7	3.0	3.3	V
VSS	Ground		0	0	0	V
VIH	Input High Voltage		2.2	-	Vcc+0.3	V
VIL	Input Low Voltage		-0.5(1)	-	0.4	V

Note
1. VIL = -3.0V for pulse width less than 30ns

TRUTH TABLE

/CS	/WE	/OE	MODE	I/O OPERATION
H	X	X	Standby	High-Z
L	H	H	Output Disabled	High-Z
L	H	L	Read	Data Out
L	L	X	Write	Data In

Note
1. H=V_{IH}, L=V_{IL}, X=Don't Care

DC CHARACTERISTICS

Vcc = 3.3V ¡ 10%/3.0V¡ 10%, T_A = 0¡ to 70¡ (Normal)/ -40¡ to 85¡ (E.T.) unless otherwise specified.

Symbol	Parameter		Test Condition		Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current		Vss ¡´ V_{IN} ¡´ Vcc		-1	-	1	uA
I_{LO}	Output Leakage Current		Vss ¡´ V_{OUT} ¡´ Vcc, /CS = V_{IH} or /OE = V_{IH} or /WE = V_{IL}		-1	-	1	uA
Icc	Operating Power Supply Current		/CS = V_{IL}, V_{IN} = V_{IH} or V_{IL}, $I_{I/O}$ = 0mA		-	1	2	mA
I_{CC1}	Average Operating Current		/CS = V_{IL}, Min. Duty Cycle = 100%, $I_{I/O}$ = 0mA		-	15	30	mA
I_{SB}	TTL Standby Current (TTL Inputs)		/CS= V_{IH}		-	-	0.3	mA
I_{SB1}	CMOS Standby Current	HY62V256B	/CS ¡Ý Vcc - 0.2V	LL	-	1.5	20	uA
		HY62V256B-I		LL	-	1.5	25	uA
		HY62U256B		LL	-	1	15	uA
		HY62U256B-I		LL	-	1	20	uA
V_{OL}	Output Low Voltage		I_{OL} = 2.1mA		-	-	0.4	V
V_{OH}	Output High Voltage		I_{OH} = -1mA		2.2	-	-	V

Note : Typical values are at Vcc =3.3V/3.0V, T_A = 25¡

AC CHARACTERISTICS(I)

Vcc = 3.3V¡ 10%, TA = 0¡ to 70¡ (Normal)/ -40¡ to 85¡ (E.T.) unless otherwise specified.

#	Symbol	Parameter	-85		-10		-12		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
	READ CYCLE								
1	tRC	Read Cycle Time	85	-	100	-	120	-	ns
2	tAA	Address Access Time	-	85	-	100	-	120	ns
3	tACS	Chip Select Access Time	-	85	-	100	-	120	ns
4	tOE	Output Enable to Output Valid	-	45	-	50	-	60	ns
5	tCLZ	Chip Select to Output in Low Z	10	-	10	-	10	-	ns
6	tOLZ	Output Enable to Output in Low Z	5	-	5	-	5	-	ns
7	tCHZ	Chip Disable to Output in High Z	0	30	0	30	0	40	ns
8	tOHZ	Out Disable to Output in High Z	0	30	0	30	0	40	ns
9	tOH	Output Hold from Address Change	10	-	10	-	10	-	ns
	WRITE CYCLE								
10	tWC	Write Cycle Time	85	-	100	-	120	-	ns
11	tCW	Chip Selection to End of Write	70	-	80	-	100	-	ns
12	tAW	Address Valid to End of Write	70	-	80	-	100	-	ns
13	tAS	Address Set-up Time	0	-	0	-	0	-	ns
14	tWP	Write Pulse Width	55	-	60	-	85	-	ns
15	tWR	Write Recovery Time	0	-	0	-	0	-	ns
16	tWHZ	Write to Output in High Z	0	30	0	30	0	30	ns
17	tDW	Data to Write Time Overlap	40	-	45	-	50	-	ns
18	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
19	tOW	Output Active from End of Write	5	-	5	-	5	-	ns

AC CHARACTERISTICS(II)

Vcc = 3.0V¡ 10%, TA = 0¡ to 70¡ (Normal)/ -40¡ to 85¡ (E.T.) unless otherwise specified.

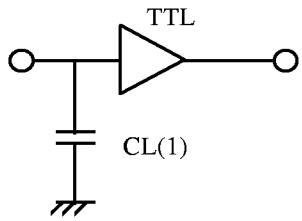
#	Symbol	Parameter	-10		-12		-15		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
	READ CYCLE								
1	tRC	Read Cycle Time	100	-	120	-	150	-	ns
2	tAA	Address Access Time	-	100	-	120	-	150	ns
3	tACS	Chip Select Access Time	-	100	-	120	-	150	ns
4	tOE	Output Enable to Output Valid	-	50	-	60	-	75	ns
5	tCLZ	Chip Select to Output in Low Z	20	-	20	-	20	-	ns
6	tOLZ	Output Enable to Output in Low Z	10	-	10	-	10	-	ns
7	tCHZ	Chip Disable to Output in High Z	0	30	0	40	0	50	ns
8	tOHZ	Out Disable to Output in High Z	0	30	0	40	0	50	ns
9	tOH	Output Hold from Address Change	20	-	20	-	20	-	ns
	WRITE CYCLE								
10	tWC	Write Cycle Time	100	-	120	-	150	-	ns
11	tCW	Chip Selection to End of Write	80	-	100	-	120	-	ns
12	tAW	Address Valid to End of Write	80	-	100	-	120	-	ns
13	tAS	Address Set-up Time	0	-	0	-	0	-	ns
14	tWP	Write Pulse Width	75	-	85	-	100	-	ns
15	tWR	Write Recovery Time	0	-	0	-	0	-	ns
16	tWHZ	Write to Output in High Z	0	35	0	40	0	50	ns
17	tDW	Data to Write Time Overlap	45	-	50	-	60	-	ns
18	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
19	tOW	Output Active from End of Write	10	-	10	-	20	-	ns

AC TEST CONDITIONS

T_A = 0¡ to 70¡ (Normal) / -40¡ to 85¡ (E.T.) unless otherwise specified

PARAMETER	VALUE
Input Pulse Level	0.4V to 2.2V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 100pF + 1TTL Load

AC TEST LOADS



Note : Including jig and scope capacitance

CAPACITANCE

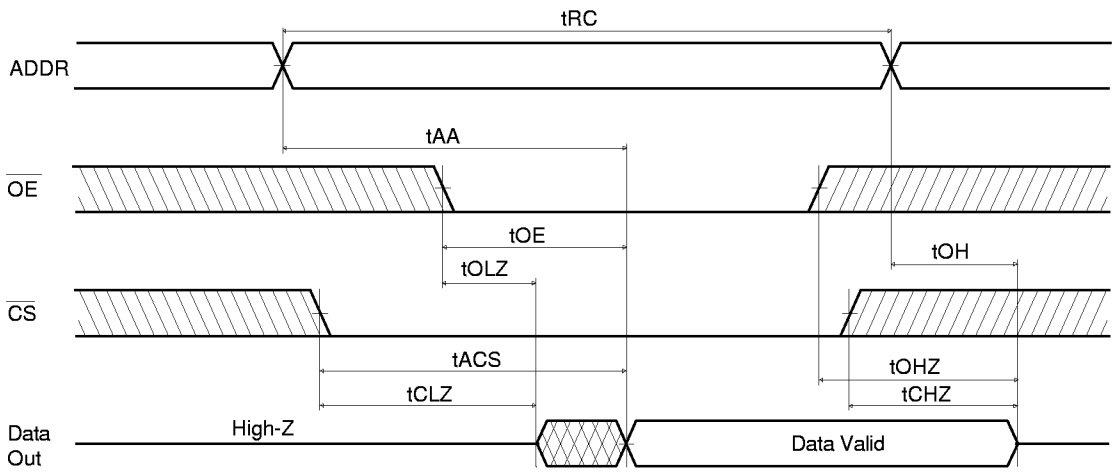
T_A = 25¡ , f = 1.0MHz

Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	Input /Output Capacitance	$V_{I/O}$ = 0V	8	pF

Note : These parameters are sampled and not 100% tested

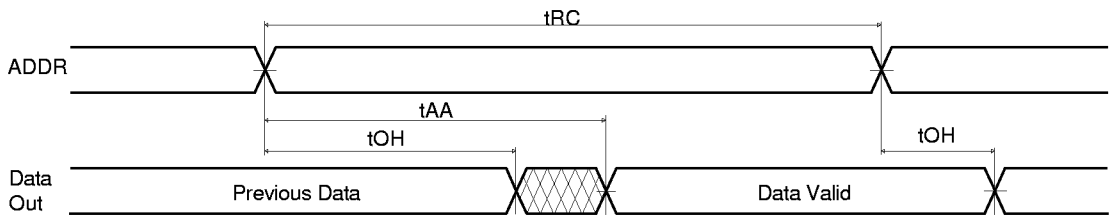
TIMING DIAGRAM

READ CYCLE 1



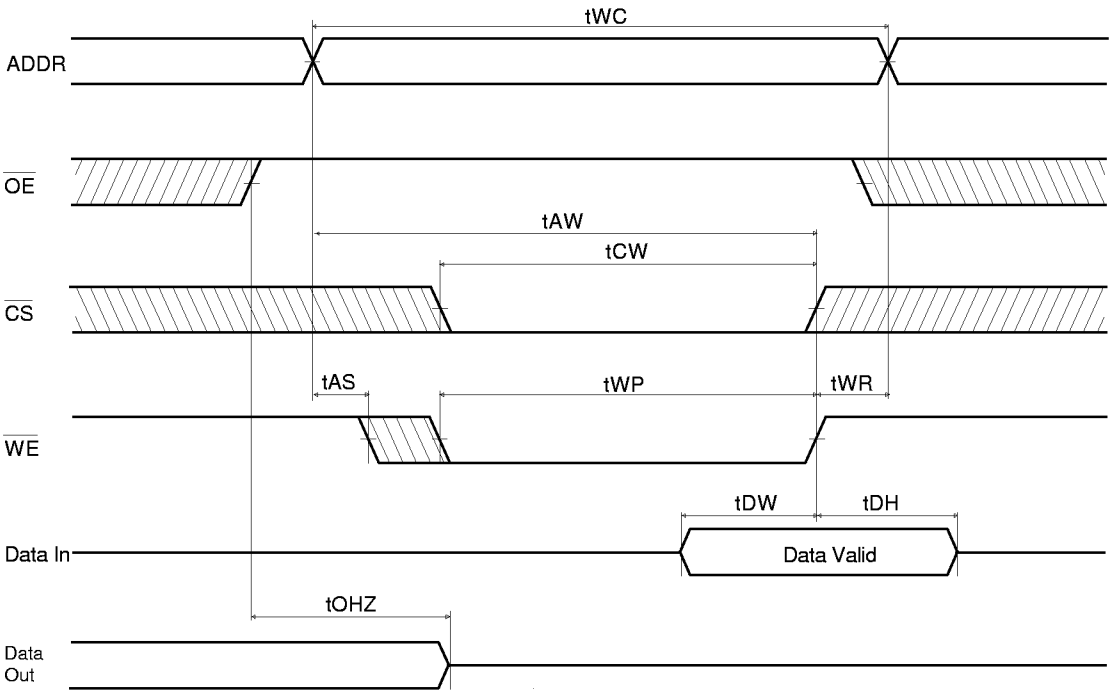
Note(READ CYCLE):
1. t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and arenot referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{CHZ} max. is less than t_{CLZ} min. both for a given device and from device to device.
3. /WE is high for the read cycle.

READ CYCLE 2

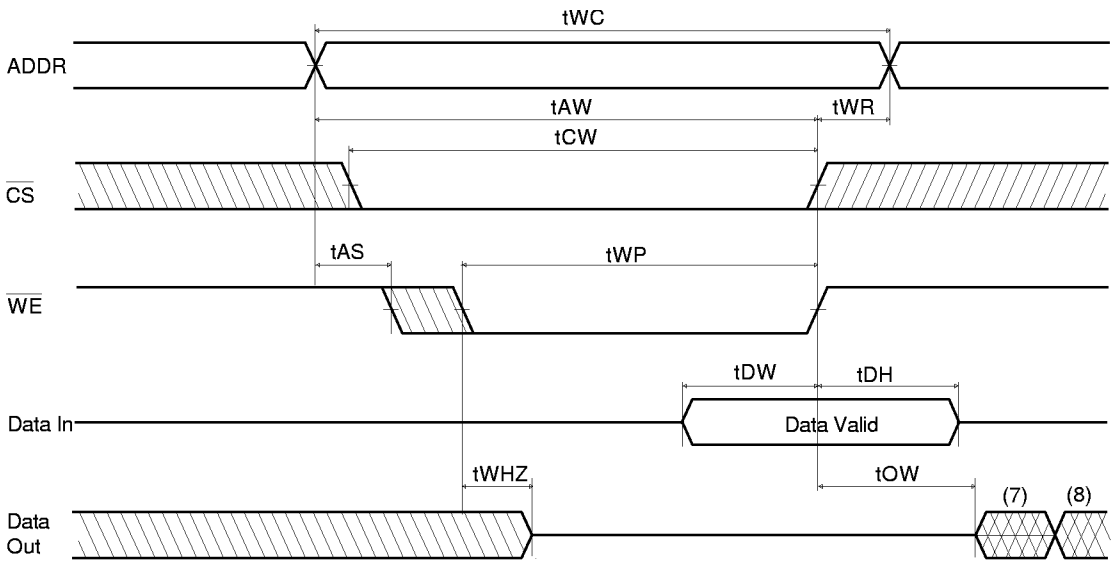


Note(READ CYCLE):
1. /WE is high for the read cycle.
2. Device is continuously selected /CS= V_{IL}.
3. /OE =V_{IL}.

WRITE CYCLE 1(/OE Clocked)



WRITE CYCLE 2 (/OE Low Fixed)



Notes(WRITE CYCLE):

1. A write occurs during the overlap of a low /CS and a low /WE. A write begins at the latest transition among /CS going low and /WE going low: A write ends at the earliest transition among /CS going high and /WE going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of /CS going low to the end of write .
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends as /CS, or /WE going high.
5. If /OE and /WE are in the read mode during this period, and the I/O pins are in the output low-Z state, input of opposite phase of the output must not be applied because bus contention can occur.
6. If /CS goes low simultaneously with /WE going low, or after /WE going low, the outputs remain in high impedance state.
7. D_{OUT} is the same phase of the latest written data in this write cycle.
8. D_{OUT} is the read data of the new address.

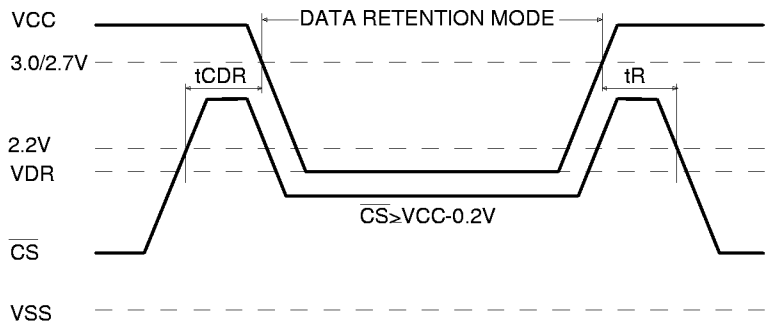
DATA RETENTION CHARACTERISTIC

TA=0°C to 70°C (Normal)/ -40°C to 85°C(E.T.)

Symbol	Parameter		Test Condition	Min	Typ	Max	Unit
V_{DR}	Vcc for Data Retention		CS¡ÃVcc-0.2V, Vss¡ÂVIN¡ÂVcc	2.0	-	-	V
I_{CCDR}	Data Retention Current	HY62V256B	Vcc=3.0V, /CS¡ÃVcc - 0.2V, Vss¡ÂVIN¡ÂVcc	-	1	15	uA
		HY62V256B-I		-	1	20	uA
		HY62U256B		-	1	15	uA
		HY62U256B-I		-	1	20	uA
tCDR	Chip Deselect to Data Retention Time		See Data Retention	0	-	-	ns
tR	Operating Recovery Time		Timing Diagram	tRC(2)	-	-	ns

Notes
1. Typical values are under the condition of T_A = 25¡Ì
2. tRC is read cycle time.

DATA RETENTION TIMING DIAGRAM



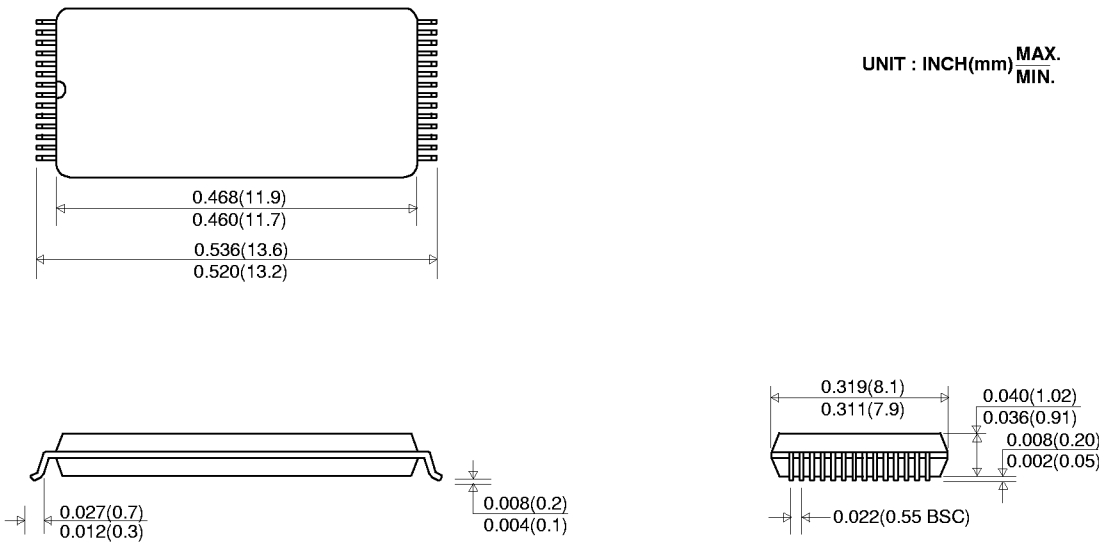
Note :
1. 3.0V : HY62V256B and HY62V25B-I
   2.7V : HY62U256B and HY62U256B-I

RELIABILITY SPEC.

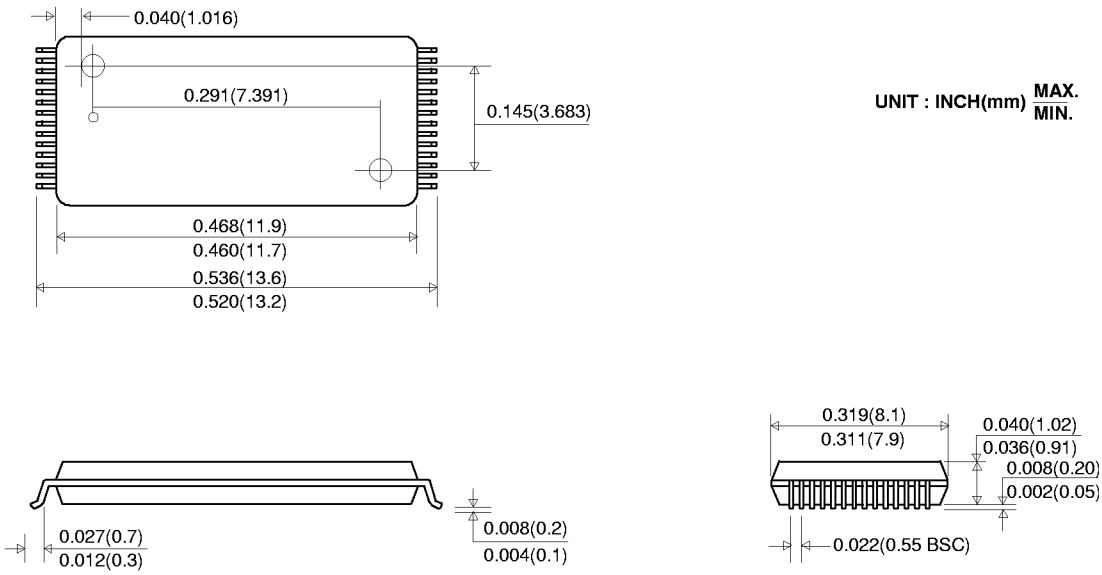
TEST MODE		TEST SPEC.
ESD	HBM	¡Ã 2000V
	MM	¡Ã 250V
LATCH - UP		¡Â -100mA
		¡Ã100mA

PACKAGE INFORMATION

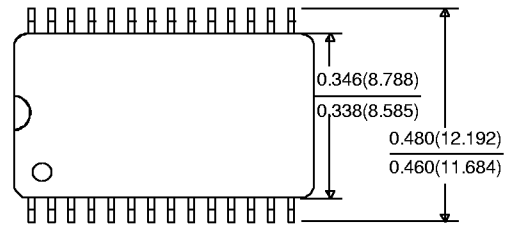
28pin 8x13.4mm Thin Small Outline Package Standard(T1)



28pin 8x13.4mm Thin Small Outline Package Reversed(R1)



28pin 330mil Small Outline Package(J)



UNIT : INCH(mm) MAX / MIN.